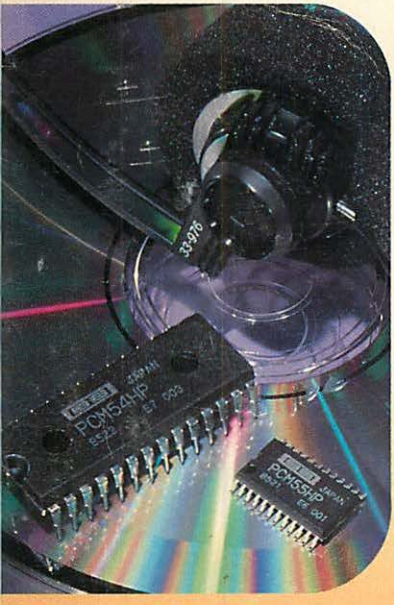
The Handbook of Linear IC Applications



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The Handbook of Linear IC Applications

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SWOP AMP® Burr-Brown Corp.

ANALOG ICs DIVIDE ACCURATELY TO CONQUER COMPUTATION PROBLEMS

Housed in dual-in-line packages, the hybrids can multiply, divide, or take the square root

Although analog dividers are basic building blocks in a wide variety of applications, until recently they remained bulky, very limited in operating range, and prohibitively expensive. Within the past two years, though, they have profited from the kinds of technological and design advances that have characterized the progress of integrated circuits in other areas.

Now, dedicated analog dividers are available in dual-in-line packages, and their low price—typically less than $30—has gone hand-in-hand with performance that has improved by orders of magnitude. Burr-Brown Corporation, for instance, makes a hybrid precision divider, the DIV100, with a guaranteed maximum error of less than 0.25% over a 40/1 denominator voltage. With optional external trims, the error may be significantly better over its 40/1 denominator range.

WHAT IS AN ANALOG DIVIDER?

Analog dividers are widely used in such applications as ratiometric measurements, percentage computations, transducer and bridge linearization, automatic level- and gain-control systems, voltage-controlled amplifiers, and analog simulations. They may be thought of as black boxes having two inputs and one output and the transfer function given by the equation:

$$V_o = K(N/D)$$

where:

V_o = output voltage
K = a scale factor constant
N = numerator input
D = denominator input

For most commercial packaged dividers, K is internally set at 10. Since the divisor can never pass through zero, D is always unipolar. Because N can be bipolar, the divider will operate in two of the four quadrants, as shown in Figure 1; it is therefore called a two-quadrant divider. Dividers that are designed for operation with N of one polarity are called one-quadrant dividers. At this point, no commercial four-quadrant divider exists, because it is impractical, though not impossible, to design one that would accept bipolar denominator voltages with a dead zone around zero.

There are two limiting conditions for every divider. First, the absolute value of N must be smaller than that of D to prevent the output from saturating beyond 10 volts. Second, a lower limit, D_{min} is always specified for the denominator below which the divider will exhibit unacceptably large errors. These two conditions define the operating region of a divider (the shaded area in Figure 1). For one-quadrant dividers, the operating region is either the top or the bottom half of the operating region of a two-quadrant divider.

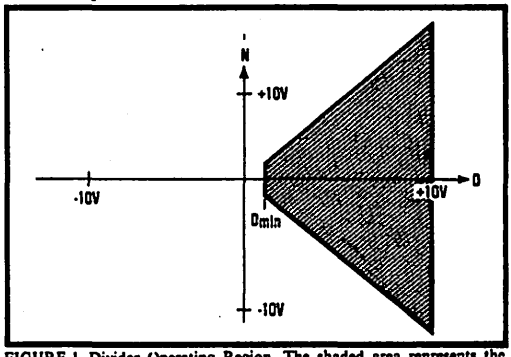

FIGURE 1. Divider Operating Region. The shaded area represents the operating region of a two-quadrant divider. A one-quadrant divider will perform in either the top or bottom half of the shaded area. Below D_{min}, the denominator exhibits unacceptably large errors.

PERFORMING DIVISION WITH MULTIPLIERS

The oldest and perhaps still the most common method of performing analog division is to connect a multiplier in a feedback loop of an operational amplifier (Figure 2a). An extra op amp is not needed with commercial packaged multipliers, since their output op amps can be employed through external pin connections.

Figure 2b shows a 4214 transconductance multiplier connected as a differential divider. One limitation of the multiplier-inverted divider (MID) is its limited divisor range. The divider error that limits the ranges can be estimated by:

$$\epsilon_d \doteq 10\,(\epsilon_m/D)$$

where ϵ_m is the multiplier error specified by the manufacturer and D is the denominator voltage. With a 0.5% transconductance multiplier, the divider error will go as high as 5% when D goes down from 10V to 1V. Hence, for practical purposes, these dividers are accurate only over a 10/1 denominator range.

The divider error can be reduced by shifting the level and preamplifying the divisor input and then shifting back at the output stage. In Figure 3, with K defined by the ratio R_2/R_1, the divider error given by $\epsilon_d \doteq 10\epsilon_m/D$ will be

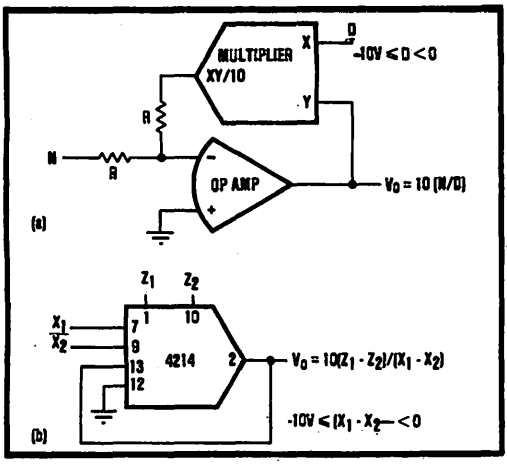

FIGURE 2. Economizing Space. An analog divider can be constructed by connecting an analog multiplier in the feedback loop of an op amp (a). Packaged multipliers (b) do not require an external op amp to be pin-programmed for performing division.

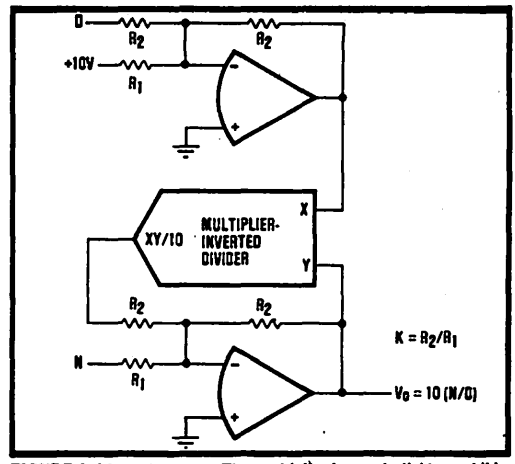

FIGURE 3. More Accurate. The multiplier-inverted divider exhibits improved accuracy when connected in the manner shown. The error equation is given approximately by $e_d = 10\epsilon_m$ (KD), where K is the ratio of R_2 to R_1 and can be used to optimize the divisor's range.

reduced by a factor of K. However, the divisor input is thus limited to -20/K volts. When K = 2, the divisor will swing within the same range of 0 to -10V. In other words, the divider error can be cut in half without sacrificing the divisor's dynamic range. With K greater than 2, say, K = 10, the divisor is limited to the range of 0 to -2V.

ONE-QUADRANT DIVIDER

The well-known multifunction converter (MFC), through different external connections, can be used as a precision divider whose accuracy and dynamic range greatly exceed that of a multiplier-inverted divider. It is, however, good for one-quadrant operation only, whereas the MID is a two-quadrant divider.

The functional diagram of this converter is shown in Figure 4. Its transfer function is given by:

$$V_o = X(Y/Z)^m$$

where m is determined by two external resistors and can range from 0.2 to 5. The circuit can be analyzed by applying, to each of the four transistors used to achieve the logarithmic relationship Q_1 - Q_4, the Ebers-Moll equation:

$$V_{be} = (KT/q)\ln(I_c/I_s)$$

where:

V_{be} = base-to-emitter voltage
K = Boltzmann's constant (8.62×10^{-5} electron-volt/K)
T = absolute temperature
q = charge of an electron (1eV)
I_c = collector current
I_s = emitter saturation current

Solving the equation for each of the four transistors simultaneously yields the converter's simple transfer function. This procedure assumes that the four transistors are matched, so that I_s and T are the same for all four equations.

The multifunction converter is capable of operating over a 40/1 denominator range with an error of less than 0.25%. At low input-signal levels, the offset voltages and bias currents of the Y and Z op amps contribute most of the errors. By trimming them out with potentiometers R_2 and R_3, the maximum error can be reduced less than 0.25% over a 40/1 dynamic range. R_1 is used to trim out gain errors.

The DIV100 analog divider has been optimized as a log-antilog divider. It is specified to be the most accurate two-quadrant, self-contained divider available in IC form. It operates in principle very similarly to a multifunction converter, but has several additional features. For one, it contains an internal level-shifting circuit for two-quadrant operation. For another, it is laser-trimmed to hold total error to less than 0.25% over a 40/1 dynamic range. In addition, both linearity compensation and an on-board temperature-compensated reference are provided.

PRECISE FOR TWO QUADRANTS

The divider's functional circuit diagram is shown in Figure 5a. Q_1 - Q_4 are the four logging transistors, which are always laid out on a monolithic chip along a thermal equilibrium line. Their geometries are specially designed for maximum conformity to a logarithmic output. In fact, log-conformity error is less than 0.05% over four decades of collector current from 100μA to 10nA. Thus, the divider can maintain its accuracy over many decades of denominator voltages.

The error sources at low input levels are mainly due to the offset voltages and bias currents of the numerator and denominator input op amps, and not to the logging transistors. Optional trims are usually provided by manufacturers in order to eliminate the offsets and bias currents that are inherent in all op amps.

As with the multifunction converter and the multiplier-inverted divider, the bandwidth of the log-antilog divider decreases almost linearly with divisor voltage level; for example, a 400kHz divider at a 10V divisor voltage will become a 4kHz divider at a 100mV divisor voltage. It is interesting to note that if it were possible to rearrange the

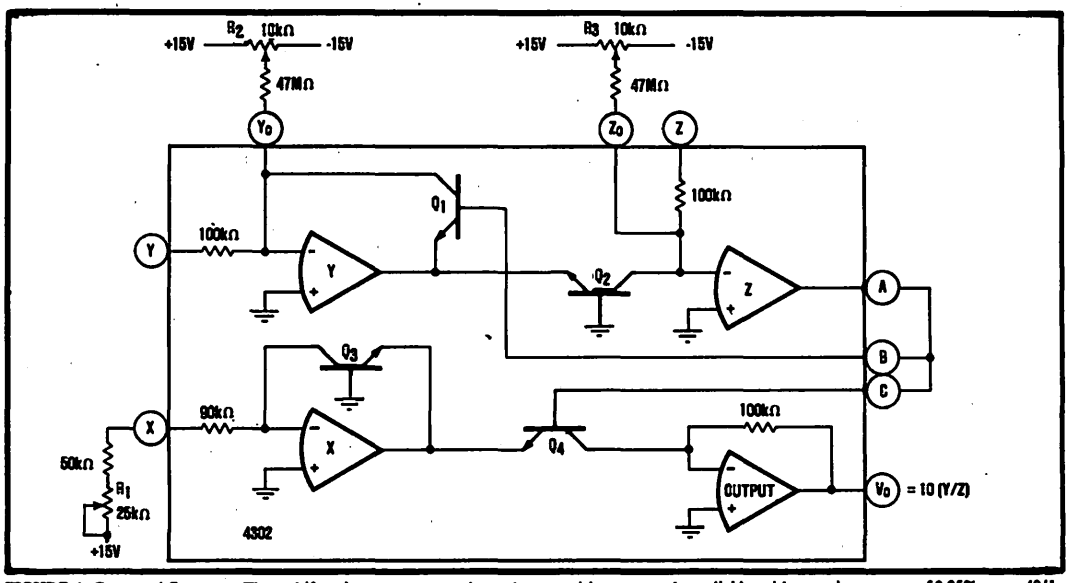

FIGURE 4. Converted Converter. The multifunction converter may be used as a precision one-quadrant divider with a maximum error of 0.25% over a 40/1 denominator range. The maximum error can be reduced by using potentiometer R_2 and R_3.

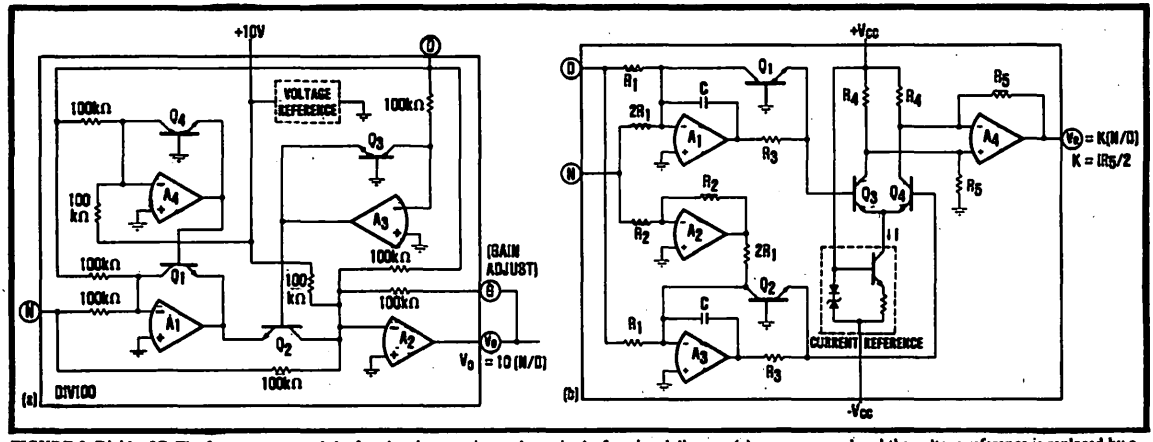

FIGURE 5. Divider IC. The four op amps and the four logging transistors shown in the functional diagram (a) are rearranged and the voltage reference is replaced by a current reference to form a log-antilog divider that maintains a constant-level bandwidth with decreasing divisor voltages (b).

four logging transistors and the four op amps and replace the voltage reference by a current reference, a log-antilog divider whose bandwidth remains constant at high level even with decreasing divisor voltages could be realized (Figure 5b).

Notice that the current through the output stage (Q_3, Q_4, and A_4) is determined by the reference current, I, and remains constant. If I is set high, the divider's bandwidth will stay fairly flat from a 10V divisor voltage down to 100mV and then start to drop gradually, at a much slower rate than the circuit in Figure 5a. Using 741-type op amps and setting I equal to 200μA, typical component values are:

$R_1 = 50k\Omega$ $R_4 = 10k\Omega$
$R_2 = 10k\Omega$ $R_5 = 100k\Omega$
$R_3 = 33k\Omega$ $C = 33pF$

As mentioned before, the offset voltages and bias currents of the op amps should be nulled out for low-signal operations. Unfortunately, with a reference current in place of a reference voltage, this divider circuit cannot be readily used as a three-input multiplier-divider to perform $V_o = XY/Z$.

SQUARE-ROOTERS

One application of a precision divider is computing the square root of an input signal, often required in process-control systems. If the divisor's input is connected to its output terminal, the divider's transfer function, that is, $V_o = 10N/D$, becomes:

$$V_o = 10\,(N/V_o) = (10N)^{1/2}$$

The output is now proportional to the square root of the input, N.

Square-rooters employing a log-antilog divider and a

multiplier-inverted divider are shown in Figures 6a and 6b, respectively. Since V_o is always unipolar, adding a diode at the output of the divider will help prevent the square-rooter from saturing to the opposite supply voltage, which is occasionally caused by power-supply transients. In Figure 6b, a 1MΩ output load may be necessary to turn on the diode, because the input impedances of the mid divider are so high (about 10MΩ) that, without the load, practically no current will flow through the diode.

The square-rooter's accuracy is strictly dependent upon the accuracy of the divider employed. With a multiplier-inverted divider, the accuracy is poor at low input voltages. The error-versus-signal voltage can be estimated from:

$$V_o = (10V_{in} + 10\epsilon_m)^{1/2}$$

where V_o and V_{in} are the square-rooter's output and input voltages, respectively, and ϵ_m is the multiplier error specified by the manufacturer. For example, for a 0.5% multiplier, ϵ_m = 50mV maximum, and therefore the square-rooter's error would be 25mV maximum at V_{in} = 10V, but would be 109mV maximum at V_{in} = 500mV.

Figure 6c compares the typical error curves of square-rooters built with a multiplier-inverted divider and those made with a log-antilog divider. Typical errors would normally be much lower than in the graph. As can be seen, if small-signal accuracy is critical, a precision divider like the log-antilog type should be used.

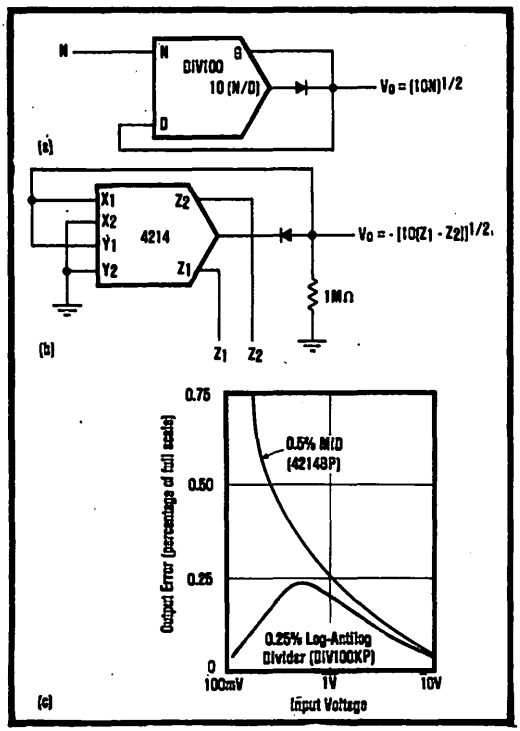

FIGURE 6. Taking the Square Root. Implementing either the multiplier-inverted divider (a) or the log-antilog divider (b) for finding the square root is a matter of the degree of accuracy wanted. Typical error curves for the two types are shown in the graph (c).

With an external voltage reference, a multi-function converter may also be used to build a square-rooter. There are two ways to implement this function. The straightforward method is to set m = 1/2 with two matched resistors and connect X and Z to a 10V reference (Figure 7a). Then the output voltage becomes.

$$V_o = 10(Y/10)^{1/2} = (10Y)^{1/2}$$

Alternatively, m can be set to 1 as in Figure 7b and the X input connected to a +10V reference. By shorting Z to the output, V_o, the transfer function becomes:

$$V_o = 10(Y/V_o) = (10Y)^{1/2}$$

The accuracy of this square-rooter is about equal to that of a log-antilog divider.

LINEARIZING THE BRIDGE

The familiar Wheatstone bridge is widely used in measuring the resistance of sensors like strain gauges, pressure transducers, thermistors, and servo motors. Unfortunately, the output of the bridge is a nonlinear function of the input variable, the change in the resistance being measured. As illustrated in Figure 8a, the output voltage, V_o, is related to the input variable, δ, by:

$$V_o = V_x\delta/(1 + \delta)$$

where $2V_x$ is the bridge supply voltage.

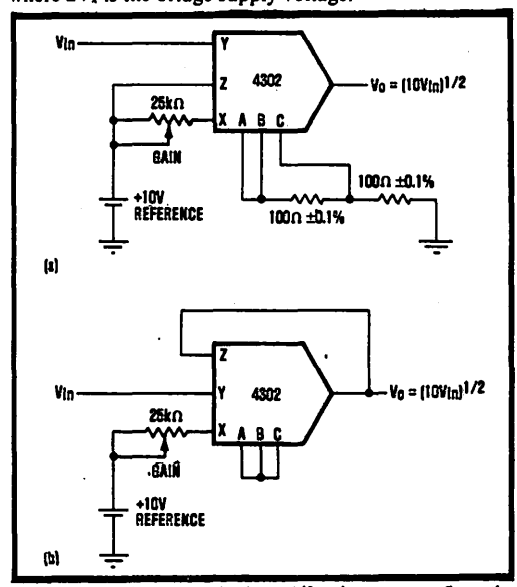

FIGURE 7. Another Approach. the multifunction converter (here, the 4302) may also be used as a square-rooter. To implement the transfer function, $V_O = X(YZ)^m$, M can be equal to 1/2 (a) or to 1 (b), with the other connections appropriately made.

Because direct measurement and manipulation of nonlinear data is often undesirable, a circuit is needed to first linearize the bridge function. The simplest method of linearization uses an op amp. Connecting the variable-resistance arm in the feedback loop (Figure 8b) causes the output of the op amp, V_o, to vary linearly with the variable, δ. Thus, $V_o = -V_x\delta$. However, some inexpensive

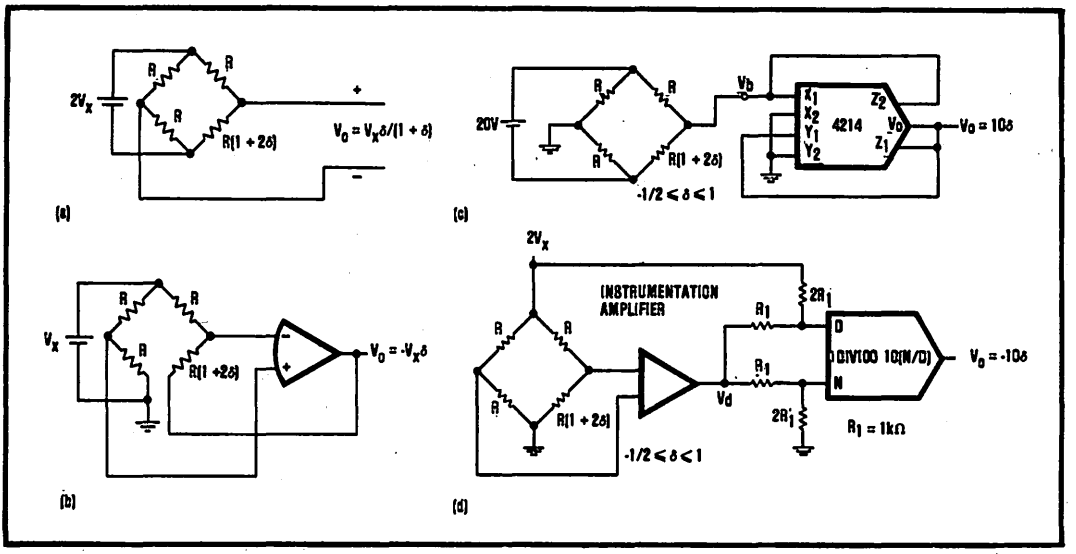

FIGURE 8. Linearizing Bridges. the Wheatstone bridge has a nonlinear output dependent on the input variable (a). It may be linearized by using an op amp in a feedback loop ((b), a multiplier-inverted divider (c), or an MID with an instrumentation amplifier (d).

bridges are packaged in four-terminal boxes and therefore will not work with this method, which requires five terminals.

A low-cost multiplier-inverted divider with differential Z inputs can, however, implement the inverse of the bridge function and linearize it. In Figure 8c, the output voltage of the bridge, V_b, is given by:

$$V_b = 10\delta/(1 + \delta)$$

and the multiplier-inverted divider provides the transfer function, $V_o = 10V_b/(10 - V_b)$. The series connection of these two nonlinear circuits results in a linear function, that is, $V_o = 10\delta$.

If the bridge supply voltage is single-ended, rather than floating as in Figure 8c, an instrumentation amplifier is needed to convert the two output terminals of the bridge to a single output. The amplifier can also be used effectively to compensate for bridge voltage variations. By inverting the signal such that $V_d = -V_x\delta/(1 + \delta)$ and using four resistors to sum the bridge voltage with, and divide it by, V_d (Figure 8d), the divider's denominator and numerator voltage become:

$$D = [2R_{iD}/(3R_{iD} + 2R_i)](V_x + V_d)$$
$$N = [2R_{iN}/(3R_{iN} + 2R_i)]V_d$$

respectively, where R_{iD} is the input impedance of the divider's denominator input and R_{iN} is that of the numerator input.

The cleverness of this circuit becomes clear when D and N are substituted into the divider's simple transfer function, $V_o = 10N/D$. The bridge voltage, $2V_x$, and the input impedance, R_i (= R_{iN} = R_{iD}), cancel out, resulting in $V_o = -10\delta$. Therefore, the output is independent of the bridge supply voltage. When R_i is much smaller than R_i, the circuit is insensitive to the value of R_i.

CONTROLLING THE GAIN AUTOMATICALLY

To compensate for amplitude fluctuations of any given signal, nothing less than a well-designed automatic-gain-control circuit will do. A good AGC circuit is one that can keep the output constant over a wide dynamic range of input signal levels (tracking range). Analog dividers are excellent candidates for such applications.

The tracking range of an AGC is directly related to the denominator's operating range of the divider employed. For example, if a divider has a divisor operating range from 10V down to 100mV, the AGC circuit associated with it will track AC signals over a 40dB range.

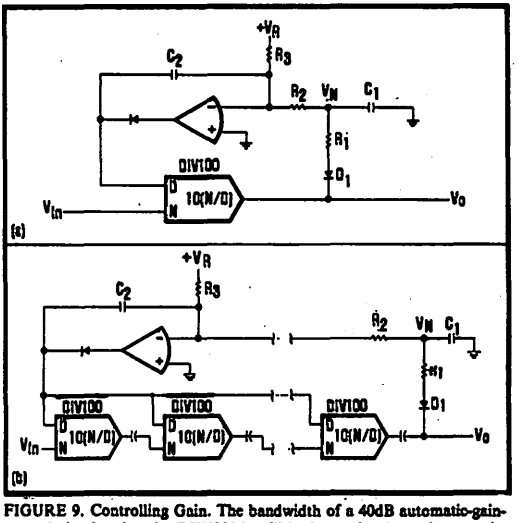

FIGURE 9. Controlling Gain. The bandwidth of a 40dB automatic-gain-control circuit using the DIV100(a), will be increasing by n times, or its tracking range by n times, by cascading n dividers in the feedback loop shown in (b). The 400kHz bandwidth, however, cannot be exceeded.

Figure 9a shows an AGC circuit using a two-quadrant log-antilog divider. The divider serves as a voltage-controlled amplifier whose output increases with a

decrease in divisor voltage. Diode D_1 rectifies the output voltage, V_o. Low-pass filter R_1 - C_1 produces a negative voltage, V_n, proportional to the negative peak of V_o. The integrator, comparing V_n with a positive reference voltage, V_R, determines the divisor voltage of the divider.

Automatic gain control is achieved thus: as the input signal, V_{in}, increases, V_o tends to increase, pushing V_N further negative. This increases the integrator's output voltage, which is connected to supply the divisor's input. As the divisor voltage goes up, it will pull V_o back down until it reaches an equilibrium.

Typical values for audio applications are:

$R_1 = R_2/10 = R_3/10 = 1k\Omega$

$C_1 = 10C_2 = 10\mu F$

$V_R = 0.3V$

These values will provide a 2V peak-to-peak output amplitude, which can be reset by adjusting either R_3 or V_R. For subaudio frequencies, an increase in the values of both C_1 and C_2 is necessary.

The upper frequency limit is determined by the bandwidth of the divider, and the bandwidth of most dividers decreases with decreases in divisor voltage. This means that the bandwidth of the AGC will decrease with input signal voltages.

As an example, with a divider's 3dB bandwidth specified for 400kHz at a 10V divisor voltage, the bandwidth will be, as a rule of thumb, 40kHz at a 1V divisor voltage and 4kHz at a 100mV divisor voltage. With these specifications, a 40dB AGC circuit will operate over a 40dB signal range only up to 4kHz and over a 20dB range up to 40kHz. Although it can function up to 400kHz, the circuit will have no practical tracking range at those frequencies.

The bandwidth of the AGC circuit can be expanded by cascading two or more dividers in the feedback loop (Figure 9b). For the 40dB example, each of the dividers operates actually over 40/n dB, where n is the number of dividers cascaded. The bandwidth of the AGC circuit will thus be increased by n times, but will, of course, never exceed the divider's maximum bandwidth of 400kHz. The cascading technique will also increase the tracking range of the AGC circuit by n times; that is, two 40dB dividers will yield an 80dB AGC circuit. AC coupling at the output of each divider is recommended to eliminate unwanted divider offset voltages.

TAKING RATIOS

For ratiometric applications, a divider naturally comes to mind. Percentage measurement:

$$V_o = 100(V_2 - V_1)/V_1$$

is just another version of ratiometric measurement, but it requires a divider with differential numerator inputs and adjustable gain (from the nominal 10 to 100). With low-cost IC dividers, it is practical to provide direct readout in percentages of such parameters as efficiency, distortion, gain/loss, error, and so on.

Figure 10 shows a percentage measurement circuit employing a differential multiplier-inverted divider. The circuit, which provides 1V = 1%, is capable of measuring ±10% deviations. Wider deviations can be measured by decreasing the ratio of R_2/R_1, and narrower variations by increasing the ratio. If the dynamic range of V_1 is too wide for a multiplier-inverted divider to handle, a log-antilog divider may be employed, but an extra operational amplifier will be needed to take the difference V_2 - V_1.

The percentage circuit can also be used to sort components by first converting the component's parameter into a voltage and comparing it with a reference. A comparator at the output of the percentage circuit may then be set to separate units beyond a specified limit.

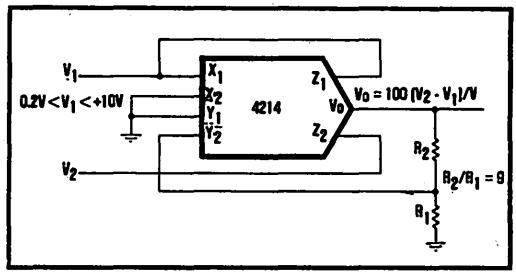

FIGURE 10. A Natural Application. Direct readouts in percentage or such parameters as efficiency, distortion, gain/loss, and error are easily obtained by connecting a 4214 in a configuration that provides an output of 1V = 1% with deviations measured up to ±10%.

References:

1. Y.J. Wong and W.E. Ott, "Function Circuits: Design and Applications," McGraw-Hill, New York, 1976.
2. J.G. Graeme, "Designing with Operation Amplifiers: Applications Alternatives," McGraw-Hill, New York, 1977.

CREATE COMPLEX NONLINEAR TRANSFER FUNCTIONS WITH A MULTIFUNCTION CONVERTER

A multifunction circuit is an uncommitted analog circuit that will perform a variety of functions as programmed by external pin connections. Its basic transfer function is:

$$E_{out} = V_y\left(\frac{V_z}{V_x}\right)^m$$

The multifunction circuit has three independent inputs that may be any value between 0 and +10V. The exponent m can vary between 0.2 and 5.

As you can see, the multifunction circuit is an extremely versatile analog circuit. The operations that it will perform include:

$$(V_y)(V_z), \frac{V_z}{V_x}, V_z^2, \sqrt{V_z}, V_z^m, V_y\sqrt{V_z/V_x}, \sqrt[n]{V_z}$$

and many others. With a few external components, the possibilities are almost endless: sine, cosine, arctangent, vector magnitude, true RMS, log.

In the multiply mode (with V_X = constant and m = 1), the multifunction circuit is very accurate, with typical errors of 0.25% of full scale.

Multifunction circuits are designed to be used in analog signal conditioning circuitry. It is of course used in many of the myriad applications for multipliers where one quadrant operation is satisfactory. In fact, if a high accuracy, one-quadrant multiplier is needed, a multifunction is probably the most cost effective solution. If one or more of the inputs must be bipolar, a conventional four-quadrant multiplier may be called for. Other applications include analog processing of data as an input to data acquisition systems or just data compression in purely analog systems. This includes functions such as RMS to DC conversion and logging circuits. The multifunction circuit is truly a universal computational element.

CIRCUIT OPERATION

The multifunction circuit works on a logging circuit principle. Figure 1 shows the block diagram of a multifunction circuit.

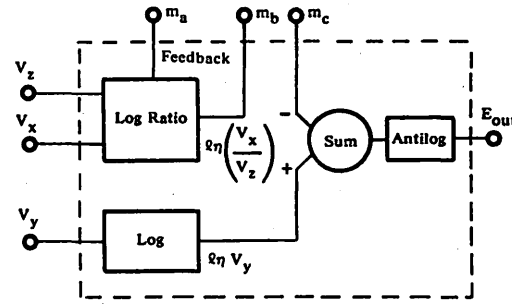

FIGURE 1. Multifunction Circuit Block Diagram.

The log ratio circuit performs the function $\log\left(\frac{V_X}{V_Z}\right)$ which is equal to $\log V_X - \log V_Z$. This output at pin m_b is transferred to the negative summing input, m_c, with some gain m. Thus the output of the summer is $-m(\log V_X - \log V_Z) + \log V_y = \log V_y + m(\log V_z - \log V_x)$. When this signal is processed by the antilog circuit, $E_{out} = \text{antilog}\left(\log V_y + m \log\left(\frac{V_z}{V_x}\right)\right) = V_y\left(\frac{V_z}{V_x}\right)^m$, the amount of the log ratio output (at pin m_b) that is applied as feedback to pin m_a determines the exponent.

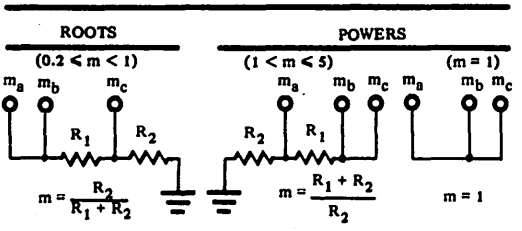

FIGURE 2. Exponent Selection for Multifunction Circuit.

Resistors R_1 and R_2 from a voltage divider. For m less than one, the log ratio output is simply attenuated by R_1 and R_2. For m greater than one, R_1 and R_2 determine the gain of the log ratio amp.

A typical log amp uses a transistor in the feedback loop of an op amp to create the log response. These log amps require a relatively complex circuit to compensate for the temperature drift of the logging transistor. In the multifunction converter, the outputs of the log ratio and log amplifiers are not temperature compensated but the antilog circuit being the inverse of the log function provides a first order temperature compensation of the log amplifiers. The circuit of Figure 3 shows the basic design of the multifunction.

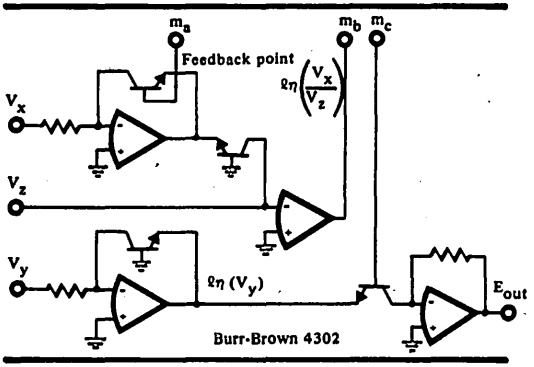

FIGURE 3. Multifunction Simplified Circuit.

The logarithmic response of these amplifiers is based on the Ebers-Moll equation for junction transistors:

$$I_c = I_s\left(e^{\frac{q\,V_{be}}{KT}} - 1\right)$$

where, I_s = constant term characteristic of each transistor
V_{be} = base to emitter voltage
I_c = collector current
q = electron charge = 1.602×10^{-19}C
K = Boltzmann's constant = 1.380×10^{-23}J/K°K
T = absolute temperature (25°C ≈ 300°K)

$\frac{KT}{q}$ @ 300°K = 26 mV, V_{be} corresponding to a diode drop is approximately 600 mV.

Therefore $e^{\frac{qV_{be}}{KT}} = e^{\frac{600mV}{26mV}} = e^{23} \gg 1$ at room temperature.

Therefore $e^{\frac{q\,V_{be}}{KT}} - 1 \approx e^{\frac{q\,V_{be}}{KT}}$

$$I_c = I_s\, e^{\frac{q\,V_{be}}{KT}}$$

$$\ell n I_c = \ell n I_s + \frac{qV_{be}}{KT}$$

$$V_{be} = \left(\frac{KT}{q}\right)\ell n I_c - \left(\frac{KT}{q}\right)\ell n I_s$$

Thus, you can see that the base to emitter voltage of a junction transistor is proportional to the log of the collector current. It is also proportional to the absolute temperature of the junction. This is the reason for the temperature drift of uncompensated log amps mentioned previously. Fortunately in the multifunction circuit the antilog circuitry has an equal and opposite drift to provide cancellation and respectable temperature stability. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. Adjacent layout of these transistors in a monolithic circuit as is done with some multifunction circuits provides the best and most repeatable results.

DIVISION

One of the most useful configurations of the multifunction circuit is in the DIVIDE mode. When m = 1 the log ratio amplifier and the antilog converter perform as a divider. Division by logging techniques produces errors that are virtually constant with input voltages. This contrasts dramatically with conventional dividers implemented by a multiplier in the feedback loop of an op amp. Conventional dividers have a very limited denominator range because at low denominator voltages the op amp approaches the open loop state with the attendant drifts and errors of open loop op amps. On the other hand, division by the multifunction circuit can accept denominator ranges of 100:1 with errors of less than 0.5%. A disadvantage of division by multifunction circuit is that the operation is only in one quadrant whereas conventional techniques yield division in two quadrants.

TRUE RMS TO DC CONVERSION

The true RMS value of an AC signal is defined as the square root of the average of the square of the input (see Figure 4). Many circuits to obtain quasi-RMS values are linear averaging circuits that are only accurate when measuring pure sinewaves. A true RMS converter on the other hand will measure accurately square waves, pulse trains, distorted sinewaves, noise, any electrical signal. A conventional technique of computing RMS values, shown in Figure 4, explicitly performs the functions called for.

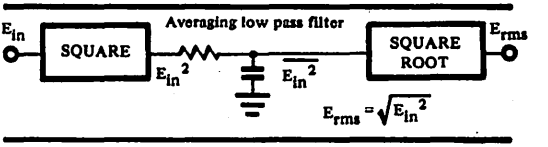

FIGURE 4. Conventional Computing RMS Converter.

A multifunction circuit can be used to implicitly perform the true RMS computation. The circuit is shown in Figure 5.

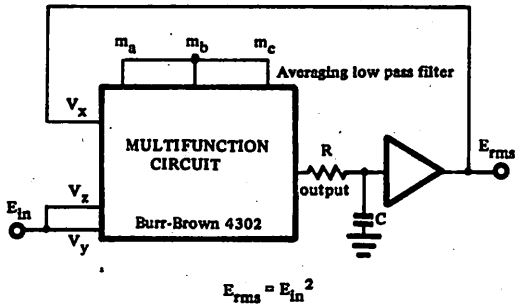

FIGURE 5. RMS to DC Converter Using Multifunction Circuit.

The implicit solution yields an output of

$$E_{rms} = \frac{E_{in}^2}{E_{rms}} \text{ solving for } E_{rms}:$$

$$E_{rms} = \sqrt{E_{in}^2}$$

The averaging time constant is determined by the choice of R & C in the lowpass filter. This time constant determines the lowest frequency of E_{in} that the unit will convert to DC. Of course, the unit will respond correctly to a DC input voltage.

EXPONENTIATION

As mentioned earlier, the exponent m may be continuously varied from 0.2 to 5. This parameter allows use of the multifunction in linearization circuits that require correction factors such as V_z^m or $(\frac{1}{V_x})^m$. Figure 6 shows the transfer characteristics when using the multifunction in the V_z^m mode.

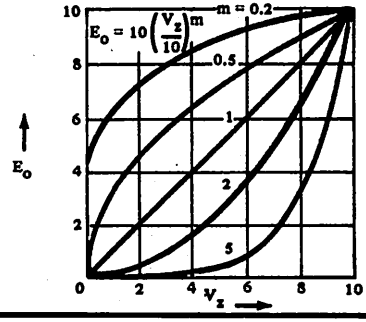

FIGURE 6. Exponentiator Transfer Characteristics.

This mode will obviously allow the use of squaring and square root linearization factors.

The transfer characteristic for $\left(\frac{1}{V_x}\right)^m$ is shown in Figure 6a.

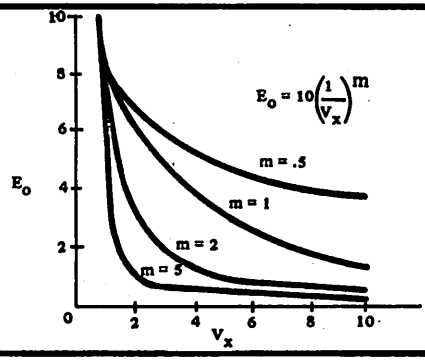

FIGURE 6a. Exponentiator Transfer Characteristics for $(\frac{1}{V_x})^m$.

This too can be a useful circuit if linearizations with negative slope are required. These two examples illustrate just some of the multitude of transfer functions that can be obtained with the multifunction circuit. If more than one of the three inputs are used as variables the possibilities are endless.

The ability of the exponent, m, to assume nonintegral values contributes to the versatility of the multifunction circuit. A nonintegral exponent can be very helpful in linearizing transducer transfer functions. The multifunction circuit provides a much smoother linearization than a diode breakpoint generator (piecewise linear method) because it has no discontinuities.

TRIGONOMETRIC FUNCTIONS

The nonintegral exponent is also very useful in approximating trigonometric functions such as sine, cosine and arc tangent. A Taylor's series expansion of an arbitrary function is

$$f(x) = f(0) + xf'(0) + \frac{x^2}{2!}f''(0) + \text{''' } + \frac{x^{n-1}}{(n-1)!}f^{n-1}(0).$$

For sine, cosine and arc tangent this is:

$$\sin x = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} + \ldots$$

$$\cos x = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \frac{x^6}{6!} + \ldots$$

$$\tan^{-1} x = \frac{\pi}{2} - \frac{1}{x} + \frac{1}{3x^3} - \frac{1}{5x^5} \ldots \text{ for } x > 1$$

If these power series expansions are altered using nonintegral exponents and modified coefficients, more accurate approximations can be achieved for a given number of terms. This mathematical approach to a true power series can be computer generated to produce a minimum error from true conformance to the ideal function. Figure 7 contrasts the error of a typical Taylor Series approximation to the error of a generalized power series expansion using nonintegral exponents.

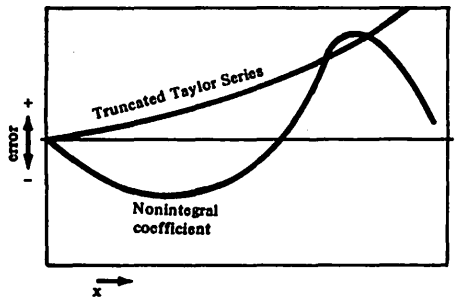

FIGURE 7. Truncated Series Expansion Comparison.

A nonintegral expansion distributes the error more or less evenly over the applicable range of x values. Taylor Series expansion produces small errors for small values of x but increases the error for larger values. It is for this reason that a nonintegral two term expansion can have theoretical accuracies 5 times better than a two term Taylor Series expansion. The trigonometric equations (for x in radians) are

	Theoretical Error
$\sin x = x - \frac{x^{2.827}}{6.28}$	$\pm 0.23\%\ 0 \leqslant x \leqslant \frac{\pi}{2}$
$\cos x = 1 + 0.2325\,x - \frac{x^{1.504}}{1.445}$	$\pm 0.75\%\ 0 \leqslant x \leqslant \frac{\pi}{2}$
$\tan^{-1} x = \frac{x^{1.2125}}{1 + x^{1.2125}}\ (90^{0})$	$\pm 0.75\%\ 0 \leqslant x \leqslant \frac{\pi}{2}$

The connections to produce these functions are shown in Figure 8. It shows among others, the connections for the arc tangent of a ratio. This is particularly well suited for conversion from rectangular to polar coordinates where

$$E_\theta = \tan^{-1}\left(\frac{E_y}{E_x}\right)$$

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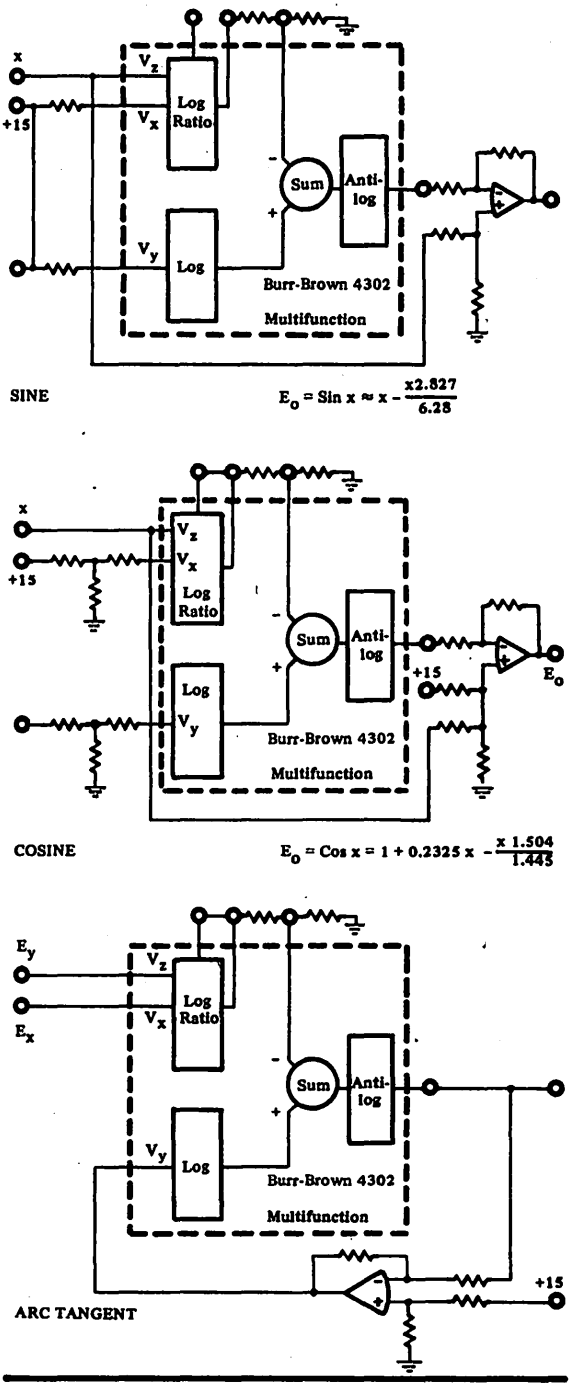

FIGURE 8. Connections for trigonometric functions using multifunction.

VECTOR COMPUTATION

The multifunction circuit will perform the square root of the sum of squares. This function is the companion to the arc tangent of a ratio for the converison of rectangular to polar coordinates. This function can be obtained implicitly as the following mathematical manipulation shows.

Desired Function: $V_O = \sqrt{V_1^2 + V_2^2}$

$$V_O^2 = V_1^2 + V_2^2$$

$$V_O^2 - V_2^2 = V_1^2$$

$$(V_O - V_2)(V_O + V_2) = V_1^2$$

$$V_O + V_2 = \frac{V_1^2}{V_O - V_2}$$

$$V_O = \frac{V_1^2}{V_O - V_2} - V_2 \quad \left(\equiv \sqrt{V_1^2 + V_2^2}\right)$$

This final equation is in a form suitable for the multifunction circuit to process. This circuit can be implemented as shown in the simplified diagram of Figure 9.

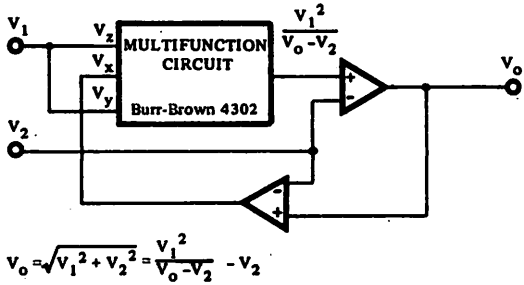

FIGURE 9. Vector Magnitude Function.

LOG AMP

The multifunction will perform as a log amp with these typical specifications:

Input Range: Voltage (4 decades) + 1 mV to +10 mV
Current (5 decades) +10 nA to +0.1 mA

Accuracy: ±1% of full scale
Accuracy Drift: ±0.4%/°C

As mentioned previously, the temperature stability is not compensated in this mode of operation. If operated in a ±10°C band, the accuracy will typically be ±5%. The V_Z input and m_b output should be used.

BIPOLAR OPERATION

The multifunction circuit can be adapted as shown in Figure 10 to bipolar input operation rather than its normal unipolar operation.

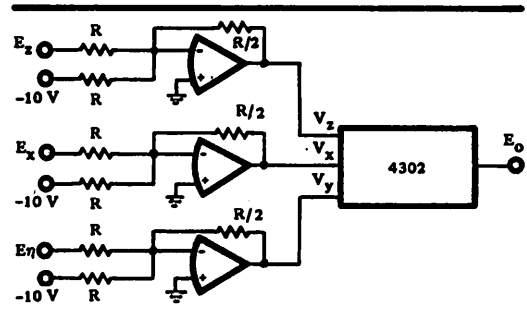

FIGURE 10. Bipolar Operation for Multifunction Circuit.

In that figure,

$$V_Z = \frac{1}{2}(-E_Z + 10),\ V_X = \frac{1}{2}(-E_X + 10),\ V_Y = \frac{1}{2}(-E_Y + 10).$$

$$E_O = V_Y\left(\frac{V_Z}{V_X}\right)^m = \frac{1}{2}(-E_Y + 10)\left[\frac{\frac{1}{2}(-E_Z + 10)}{\frac{1}{2}(-E_X + 10)}\right]^m$$

$$E_O = (10 - E_Y)\left[\frac{10 - E_Z}{10 - E_X}\right]^m$$

E_Y, E_X, E_Z can now be any value between +10 V and -10 V. As an example, a four-quadrant multiplier such that $V_O = \frac{E_Z E_Y}{10}$ can be implemented. (E_Z and E_Y anywhere between +10 V and -10V.)

$$E_O = (10 - E_Y)\left(\frac{10 - E_Z}{10 - E_X}\right)^m$$

With E_X grounded and m = 1, we have

$$E_O(10 - E_Y)\left(\frac{10 - E_Z}{10}\right) = \frac{100 - 10E_Y - 10E_Z + E_Y E_Z}{10}$$

$$E_O = \frac{E_Z E_Y}{10} + 10 - E_Y - E_Z$$

$$V_O = \frac{E_Z E_Y}{10} = E_O - 10 + E_Y + E_Z$$

This can be implemented by adding an additional op amp at the output of the circuits shown in Figure 10. This op amp circuit would simply implement the above equation (see Figure 11).

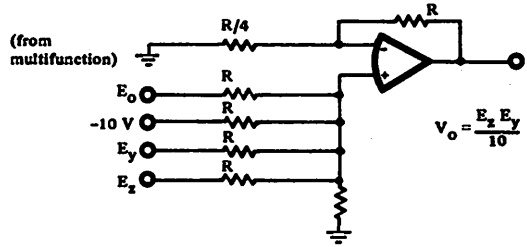

FIGURE 11. Additional Circuitry of Obtain Four-Quadrant Multiplier.

MOLD CIRCUIT RESPONSE WITH A MULTIFUNCTION CONVERTER

For generating nonlinear responses the multifunction converter excels through its noninteger exponent capability. When combined with operational amplifiers in a number of ways, this analog signal processor can develop an expanded variety of nonlinear transfer functions. Several of these functions permit correction of the frequently encountered bow and "S" shaped nonlinearities. Selection of circuit parameters for this application can be done with a BASIC program.

Historically, nonlinear transfer responses were created using piecewise-linear approximation.[1] Circuits creating such responses approximated a nonlinear function with a series of linear segments. Typically, a great number of such segments were required to make the generated response accurately fit the desired function.

Later the analog multiplier made possible nonlinear responses through power series approximation.[2] Given the moderately comprehensible number of exponents that integer values set for such series, mathematicians paved the way for this approach. Complexity in electronic realization remained relatively high, however, as this approach requires one multiplier per power term in the series. Intuitively, we can imagine a power series approximation requiring far fewer terms if noninteger exponents were used, as access to the infinite set of numbers between integer values magnifies our degrees of freedom. This is precisely the power offered by the multifunction converter—*noninteger exponents*. While finding such exponents can be intimidating to the mathematician, computers and curve fitting can do the selecting. Specifically, the multifunction converter is a specialized multiplier/divider, like the Burr-Brown Model 4302, and produces a response of

$$e_o = y\left(\frac{z}{x}\right)^m$$

where x, y, and z are input signals. Exponent m can be set to any number, integer or noninteger, within a practical range of 0.2 to 5. To generate its transfer function the multifunction converter relies on the uniquely predictable exponential current/voltage relationship of the semiconductor junction. With this relationship, log and antilog operations are performed as in Figure 1. By reducing the x, y, and z signals to their logarithms, multiplication and division are simplified to addition and subtraction. Also, power and root functions then result from amplification or attenuation of logarithmic signals, as represented by gain block m. Antilog reconversion of the resulting combined and scaled signal completes the multifunction operation to give product, quotient, and exponent. For various sample exponents the converter circuit alone produces the nonlinear curves of Figure 2. Between those shown there are, of course, innumerable other possibilities achievable with noninteger exponents.

In addition to stand alone operation a multifunction converter can be combined with op amp circuitry to expand

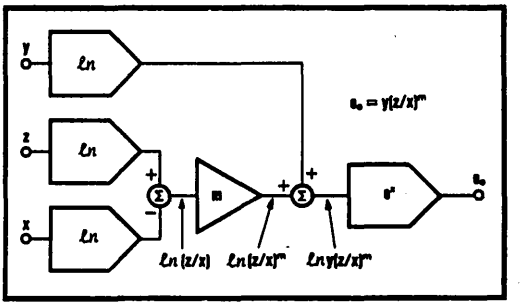

FIGURE 1. Introduction of gain m to logarithmic signals in a log/antilog multiplier/divider results in the exponent of the multifunction converter response.

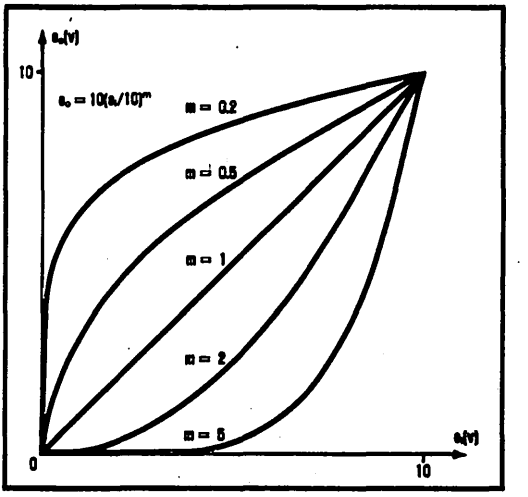

FIGURE 2. Transfer response curves of the multifunction converter provide continually increasing slopes for m > 1 (power functions) and continually decreasing slopes for m < 1 (root functions).

the variety of nonlinear responses available. The response of the basic circuit can be restructured through use of summation, feedback, or signal control of exponent. With the circuit of Figure 3a the input signal is summed with the converter output providing two terms of a power series approximation. For the element values shown, response curves like those of Figure 3b are created. Such downard bowing curves are useful in nonlinearity correction of responses that have an upward bow. When processed through this circuit, upward and downward bows tend to cancel, giving a more linear end result.

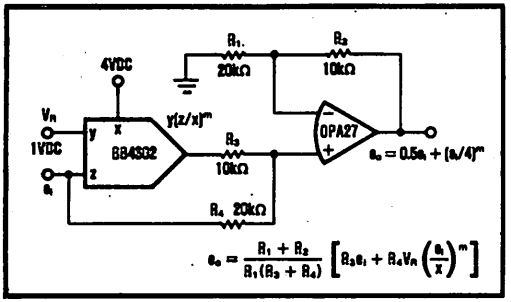

FIGURE 3a. Summation adds a second term to a response approximation.

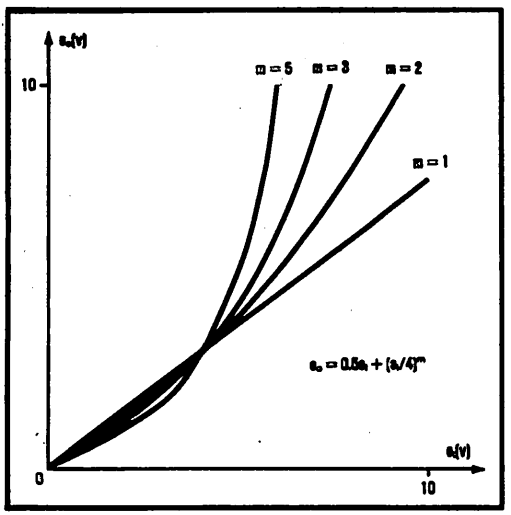

FIGURE 3b. Refined control of nonlinear response results with the circuit of Figure 3a.

To compensate a downward bow, the complement to Figure 3b is needed. Making the second term of the approximation series negative is one way to achieve this, so subtraction rather than summation is used. Figure 4a provides this by combining a difference amplifier with the converter. With the specific circuit scaling shown, curves can be derived like those of Figure 4b. Note that the bow becomes so great that some curves represent double-valued functions.

Another common nonlinearity is "S" shaped; alternately deviating to one side and then to the other of a straight

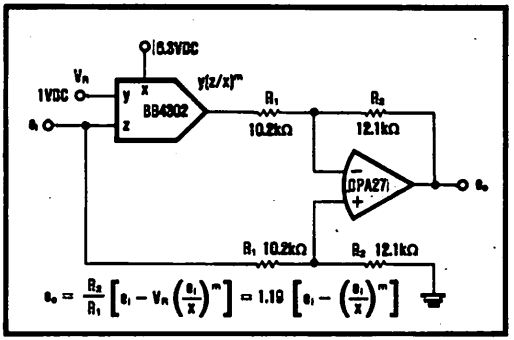

FIGURE 4a. Addition of a difference amplifier provides a negative second term to the response expression.

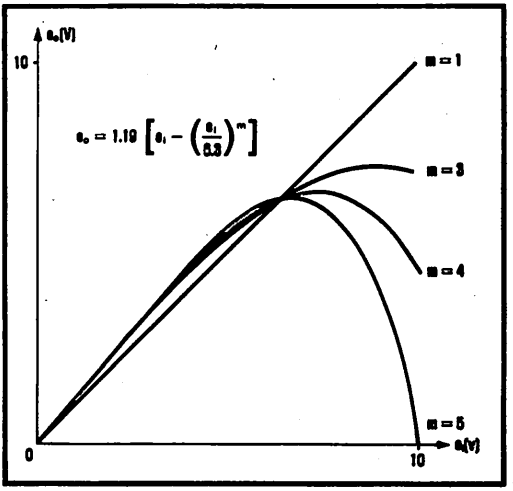

FIGURE 4b. With the power term subtracted, a downward bow develops in the response curves for Figure 4a.

line response. To derive appropriate correction curves, op amp feedback will be used with the multifunction converter. When a summing amplifier is connected from the output to one of the converter inputs as in Figure 5a, the transfer response has both numerator and denominator terms that are functions of e_i. Because of the feedback loop, the phase shifts of the converter and op amp combine to degrade frequency stability. Correcting for this is added phase compensation in the form of bypass of the op amp feedback, as this will create a single dominant pole in the loop.

This feedback connection results in response curves like those of Figure 5b. They exhibit the desired "S" shape for exponents greater than one and a companding type response for lower values. These responses provide linearity correction as a signal is processed through the circuit and encounters the nonlinear gain reflected by the response curve.

Another approach involves summation of a correction signal with the signal to be compensated. For that purpose a zero-based response, like the dashed line of Figure 5b, is required so that only the correction signal is generated. This is accomplished by rotating the curve

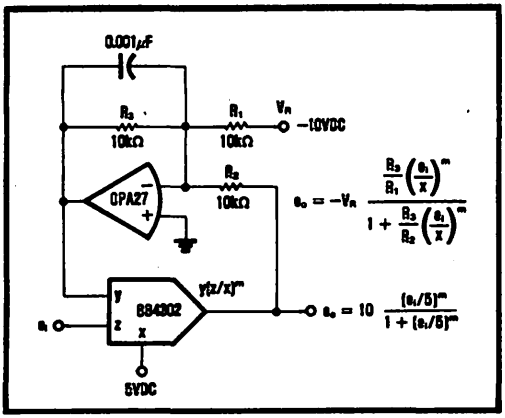

FIGURE 5a. Feedback around the converter adds a signal term to the denominator of the response.

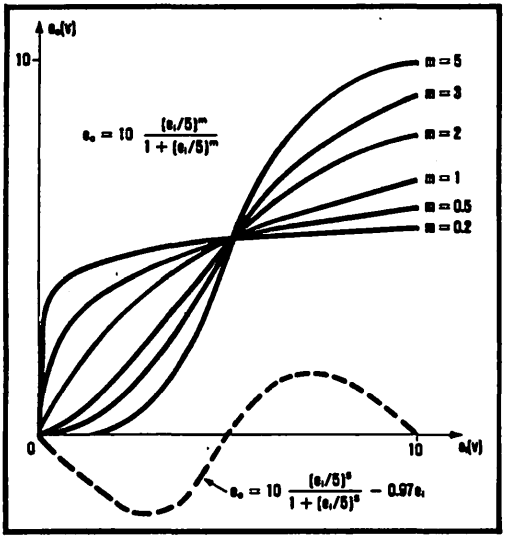

FIGURE 5b. With the circuit of Figure 5a either "S" shaped or companding responses are created.

down to the e_i axis through subtraction of an e_i term, as the dashed curve illustrates for the m = 5 case. A difference amplifier added to the circuitry will do this.

When the nonlinear response desired is the mirror image of the above, the "S" shape can be reversed by subtracting the response of Figure 5b from twice the input signal. The subtraction removes an "S" shape from an otherwise linear response to create the reverse nonlinearity. In Figure 6a this is done by combining a subtracting amplifier with the circuitry of Figure 5a. Sample response curves are shown in Figure 6b.

In the previous two circuits, an amplifier was connected in feedback around a multifunction converter. Reversing these functions, the converter becomes a feedback element in Figure 7a. As before, the feedback loop is phase-compensated with a capacitor across the op amp feedback. Now only the denominator of the response is a

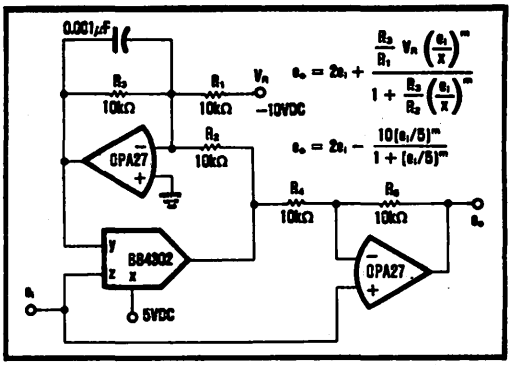

FIGURE 6a. Combining a subtracting amplifier with the configuration of Figure 5a will add a phase inversion to the nonlinear terms.

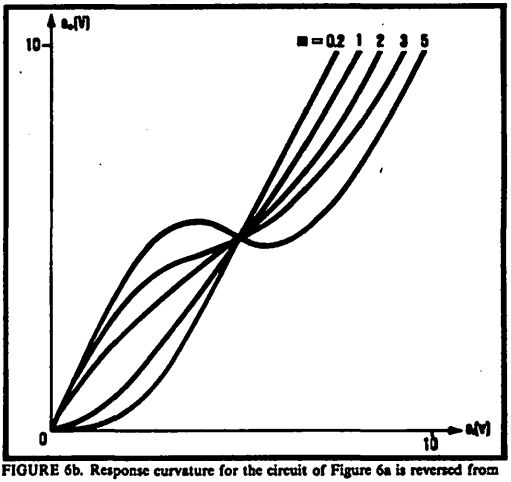

FIGURE 6b. Response curvature for the circuit of Figure 6a is reversed from that of Figure 5b.

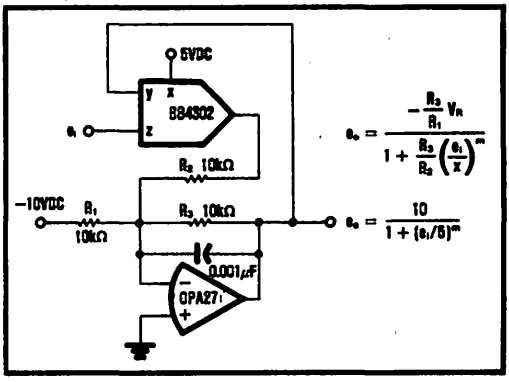

FIGURE 7a. Accepting the signal input, and in the feedback loop of an op amp, the converter generates a response function with only denominator signal dependence.

function of e_i and the results are the curves of Figure 7b. Some functions approximated by similar responses are the cosine function[3] and the Gaussian response.[4] Although offset from the origin, these responses are otherwise again the mirror images of those of Figure 5b and provide the opposite "S" shape for m > 1. It is necessary to include the offset in generating these curves because

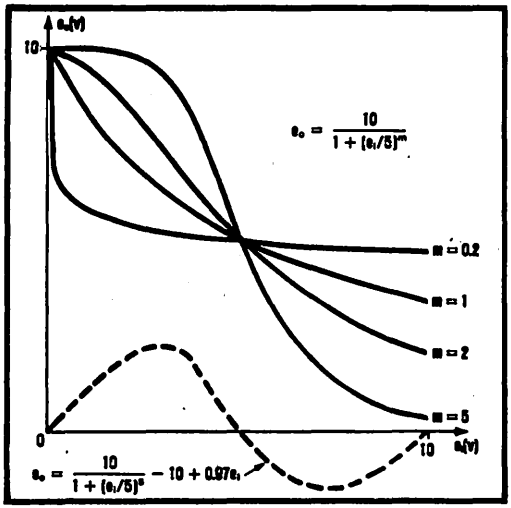

FIGURE 7b. Offset mirror images of Figure 5b result from the connection of Figure 6a.

the multifunction converter has only one response quadrant of operation ($e_i \geq 0$, $e_o \geq 0$). However, with a difference amplifier that offset can be removed, and if appropriate the response can be rotated, as described before. For the m = 5 case the result of these operations is plotted with a dashed line.

So far, the applications considered have all used fixed values for exponents. Even greater versatility is possible through signal control of the exponent, which can be seen from Figure 1. This only requires voltage control over the gain level m. Such gain control is another function performed by an analog multiplier, which the multifunction converter becomes with an exponent of one. Exploring this possibility, the input signal is made to control the exponent in Figure 7a. Gain control results from intercepting the logarithmic signal at the exponent set points and multiplying it with the input signal. Depending on whether the set points controlled are those for power or root functions, the exponent will be proportional to e_i or its reciprocal resulting in curves like those of Figure 8b. Numerous other options for voltage control of exponent exist if alternate signal connections, summation, and feedback are considered.

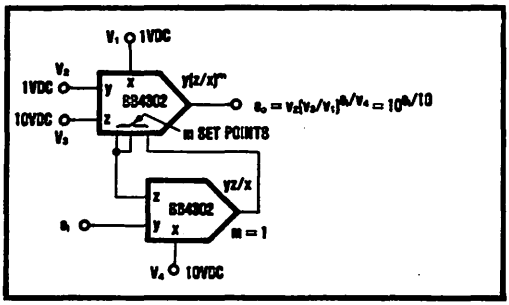

FIGURE 8a. By virtue of its logarithmic operation, the exponent of the multifunction converter is controlled by a gain level, and that can be made signal dependent.

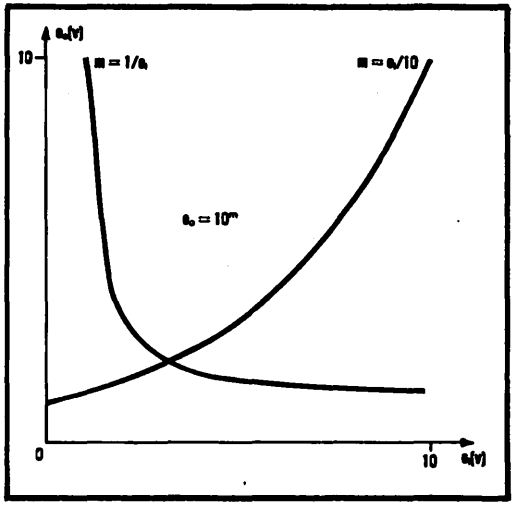

FIGURE 8b. Two possibilities derived with signal-controlled exponents.

Whichever of the preceding nonlinear response circuits is used, the response must be tailored to the application. For a specific case, an exponent and the scale factors for each term of the response equation must be chosen. This is a manageable task for a computer using iterative techniques to analyze the data. A BASIC program which performs this task is listed in Figure 9. It will select parameters for most of the circuits previously discussed in a manner that minimizes the residual nonlinearity as a percentage of full scale. Any one of four response equations can be designated and they are identified below with their corresponding circuit.

I.D. #	Response	Circuit
1	$e_o = b\left(\frac{e_i}{c}\right)^m$	Figure 1
2	$e_o = ae_i + b\left(\frac{e_i}{c}\right)^m$	Figures 3a and 4a
3	$e_o = \frac{a\left(\frac{e_i}{c}\right)^m}{1 + b\left(\frac{e_i}{c}\right)^m}$	Figure 5a
4	$e_o = 2e_i - \frac{a\left(\frac{e_i}{c}\right)^m}{1 + b\left(\frac{e_i}{c}\right)^m}$	Figure 6a

To use the program, first the type of compensation response must be chosen. This can generally be done by reviewing the example response curves presented earlier and finding a type whose nonlinearity is opposite that to be corrected. Each of the four equation types handled by the program passes through the origin. If the response to be linearized does not, it should first be mathematically offset so that the data to be analyzed has an output of zero for zero input. Following program execution, the offset can be restored by addition of a constant. Such an offset is achieved in the actual circuit by summing appropriate DC voltages with the input and output signals.

```
10 !  *** NONLIN.BAS ***   BCT AFTER JGG  3-20-84
20  INPUT "EQUATION NUMBER... (1,2,3 OR 4)";EQN
30  IF EQN < 1 OR EQN > 4 THEN GOTO 20
40      YIN(1) = .772              !  INPUT DATA FOR T TYPE
50      YIN(2) = 1.609             !  THERMOCOUPLE EXAMPLE
60      YIN(3) = 2.504
70      YIN(4) = 3.453
80      YIN(5) = 4.45
90      YIN(6) = 5.49
100     YIN(7) = 6.568
110     YIN(8) = 7.681
120     YIN(9) = 8.827
130     YIN(10) = 10               !  END INPUT DATA
140 INPUT "STARTING VALUE FOR B ";BSTART
150 INPUT "ENDING VALUE FOR B ";BEND
160 INPUT "STEP SIZE FOR B ";STP
170 INPUT "VALUE FOR C ";C
180 INPUT "GUESS FOR M ";MGUESS
190 FOR J = BSTART TO BEND STEP STP     !  LOOP TO FIND BEST START FOR B
200    B = J
210    M = MGUESS
220    PRINT "STARTING ITERATION AT B= ";B;
230    FAC = 1.2                   !  INITIALIZE ITERATION FACTOR
240    GOSUB 590
250    OLDERR = LSTERR
260    LSTERR = NEWERR
270   IF ABS(ABS(SMLERR)-ABS(NEWERR)) < .0001 THEN GOTO 350
280   IF ABS(OLDERR) > ABS(NEWERR) THEN GOTO 320
290    SMLERR = OLDERR
300    FAC = 1/FAC                 !  REVERSE DIRECTION OF ITERATION
310   GOTO 330
320  SMLERR = NEWERR
330   IF ITERB = 1 THEN B = FAC * B  ELSE M = FAC * M
340  GOTO 240
350  CNT = CNT + 1
360   ITERB = 0                             !  SET TO ITERATE M
370    IF CNT > 3 THEN ITERB = 1            !  SET TO ITERATE B
380   IF CNT < 6 THEN GOTO 280
390   IF FAC > .9997 AND FAC < 1.0003 THEN GOTO 450     !  THEN EXIT
400    PRINT "*";
410    FAC = SQR(FAC)                       !  REDUCE ITERATION SIZE
420    CNT = 1
430    ITERB = 0                            !  SET TO ITERATE M
440  GOTO 240
450     GOSUB 790
460   IF J = BSTART THEN GOTO 480          !  FIRST TIME THRU?
470   IF ABS(NEWERR) >= ABS(MINERR) THEN GOTO 520
480     MINERR = NEWERR       !  KEEP RESULTS OF BEST STARTING B VALUE
490     BMINST = J
500     MMIN = M
510     BMIN = B
520    PRINT "BEST ERR=";MINERR;"  WITH B STARTING AT";BMINST
530 NEXT J
540   M = MMIN
550   B = BMIN
560    GOSUB 590
570    GOSUB 790
580 GOTO 940
590 NEWERR = 0                          !  MAIN CALC. ROUTINE
600   FS = B*(YIN(10)/C)^M
610   ON EQN GOSUB 910,900,920,920
620   FOR I = 1 TO 10
630     ON EQN GOSUB 710,730,750,770
640      YOUT(I) = Y
650      DIFF(I) = YOUT(I)-I
660      IF ABS(NEWERR) > ABS(DIFF(I)) THEN GOTO 690
670        NEWERR = DIFF(I)
680        ERRLOC = I
690   NEXT I
700 RETURN
710  Y = B*(YIN(I)/C)^M                          !  EQN. TYPE 1
720 RETURN
730  Y = A*YIN(I)+B*(YIN(I)/C)^M                 !  EQN. TYPE 2
740 RETURN
750  Y = (A*(YIN(I)/C)^M)/(1+B*(YIN(I)/C)^M)     !  EQN. TYPE 3
760 RETURN
770  Y = 2*YIN(I)-(A*(YIN(I)/C)^M/(1+B*(YIN(I)/C)^M))   !  EQN. TYPE 4
780 RETURN
790 PRINT                                       !  OUTPUT ROUTINE
800    PRINT "A=";A,"B=";B,"C=";C,"M=";M
810    PRINT
```

```
820     PRINT " #","INPUT","CALC. OUT","ERROR"
830     FOR I = 1 TO 10
840       PRINT I,YIN(I),YOUT(I),DIFF(I);
850       IF I = ERRLOC THEN PRINT " <== MAX ERROR";
860       PRINT
870     NEXT I
880      PRINT
890 RETURN
900  A = 1-(FS/YIN(10))          !  "A" FOR EQN. TYPE 2
910 RETURN                       !  NO "A" REQUIRED FOR EQN. TYPE 1
920  A=B*(((FS+1)*YIN(10))/FS)   !  "A" FOR EQN. TYPES 3 & 4
930 RETURN
940 END
```

FIGURE 9. This BASIC program computes the required constants to linearize a given set of data points in lines 40 through 130. The data shown corresponds to the example in Figure 10.

The program seeks a solution by iterating both m and b using an iteration factor which is gradually reduced as a minima in error is approached. Since the program may converge on more than one minima, the starting value for b can be stepped through a range of values. The starting b value producing the best solution is saved and repeated in the final pass, and execution halts with the results. The error indicated in the final display is the deviation from the desired straight line response.

The program prompts for all required inputs. A starting, ending, and step value for b is chosen. Parameter c is chosen by the user in order to ensure accuracy-preserving larger values in the multifunction converter denominator. Full scale inputs of 10V lead to greatest accuracy, making c = 10 an appropriate choice. An initial guess is supplied for the constant m.

The input voltage data is written into lines 40 through 130 of the program to facilitate easy rerunning. The data in the listing is for the example given in Figure 10. These lines should be changed to your input data points after trying the sample data. Depending on the nature of the data analyzed, convergence may be smooth and fast, or perhaps somewhat difficult to achieve. In any event, some human intervention may be required to select the best range and step size for b and initial guess for m. A few runs from different starting points will help verify that a good solution has been achieved.

As an example, consider the task of linearizing the response for a type T thermocouple. Shown in Figure 10 is the thermocouple output voltage e_T for ten equally spaced temperature increments away from zero. It is assumed that a preamp would be used to boost this output to e_A and that its gain is set for a 10V full scale output. Examination of the data points reveals a downward bow so linearization can be achieved by processing the signal through a response having an upward bow, like that found in Figure 4b. So the appropriate compensation circuit is of the Figure 4a type, and the parameter finding program is set for a type 2 equation. Running the program finds the compensating transfer response to be

$$e_o = 1.621\, e_A - 6.214 \left(\frac{e_A}{10}\right)^{1.27}$$

Residual nonlinearity calculated by the program would be 12mV or 0.12% of the 10V full scale, as compared to the initial 5.5% nonlinearity. This reduced level of error is compatible with the accuracy attainable in practice with the multifunction converter.

T (°C)	e_T (mV)	e_A (V)*	e_o (V)**	Error (mV)
40	1.611	.772	1.011	11
80	3.357	1.609	1.998	−2
120	5.227	2.504	2.989	−11
160	7.207	3.453	3.988	−12
200	9.286	4.450	4.991	−9
240	11.456	5.490	5.998	−2
280	13.707	6.568	7.003	3
320	16.030	7.681	8.006	6
360	18.420	8.827	9.005	5
400	20.869	10.000	9.996	−4

*$e_A = 479.2\, e_T$ **$e_o = 1.621 e_A - 6.214(e_A/10)^{1.27}$

FIGURE 10. For a type T thermocouple the program of Figure 9 selects a linearity correction equation that would provide a 46:1 improvement.

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3. J. Graeme, *Designing With Operational Amplifiers*, McGraw-Hill, 1977.
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10MHz ANALOG MULTIPLIER CARRIES OUTPUT AMP, BREAKS BANDWIDTH BARRIER

A transconductance multiplier chip, the first one fitted with an output amplifier, alleviates design worries in high-bandwidth communication circuits.

No monolithic solution has ever existed for wideband analog multiplication. Beyond a 1MHz bandwidth, multiplier chips usually need external amplifiers and biasing, and many cannot deliver their promised accuracy and performance without external trimming components. Those burdens have largely kept single-chip multipliers out of communication applications. Mixer circuits, for example, have instead relied on signal-diode rings, even though those rings bring their own performance drawbacks, including poor low-frequency response and narrow frequency and power ranges.

With the arrival of the MPY634 multipliers, wideband analog multiplication need no longer be a multichip affair or imply performance compromises. Along with its 10MHz small-signal bandwidth, the four-quadrant chip has a laser-trimmed DC accuracy of 0.25%, an adjustable scale factor, and the ability to drive loads down to 2kΩ.

In addition, because it has three instead of two differential input pairs, the chip can divide, square, and find square roots. Those functions make it, in effect, a multifunction converter. As a result, adding just a few components creates any number of analog processors, including a voltage-controlled filter or a mixer.

The chip unites three voltage-to-current input converters, a transconductance core, a highly stable voltage reference, and a high-gain output amplifier (Figure 1). The three converters can be viewed as differential amplifiers with an extremely low transconductance, the benefits of which are a 10MΩ input impedance and a 20V/μs slew rate. Moreover, the converters' input voltages can be differential or single-ended; in the latter case, the second input can be used to nullify offsets.

HAVING THE DRIVE

The differential outputs of the converters drive the transconductance core, which actually performs the multiplication. The output of the core, a differential current, produces a voltage across a resistive load that feeds a high-gain, high-bandwidth amplifier. For multiplication, the output of the amplifier is fed back to converter Z; other mathematical operations are set up by different feedback connections.

Like any mathematical circuit, the multiplier is only as good as its linearity, accuracy, and stability. Here linearity and accuracy depend on the transconductance core, and more specifically, on how precisely the base-to-emitter voltages of its six transistors match. To maximize linearity, the transistors are diagonally coupled (cross-coupled) on the die and then laser-trimmed.

Maintaining a constant scale factor over temperature requires stable bias current in the core. A built-in bandgap reference keeps the scale factor's temperature coefficient within 30ppm/°C over a temperature range of −55°C to +125°C. Nevertheless, the scale factor can be adjusted over the range of 10V to 3V by connecting a resistor from the negative supply to the Scale Factor Adjust pin.

As with an op amp, the multiplier's open-loop equation offers insight into the chip's operation, as well as into its constraints. The open-loop equation is:

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right]$$

where V_{OUT} is the output voltage; A is the output amplifier's open-loop gain and is assumed to be infinite; X_N, Y_N, and Z_N are input voltages; and SF is the scale factor, which is nominally 10V.

For stability, feedback is applied to one or more inputs. (However, when feedback involves more than one input, designers must take care that the overall feedback does not become positive.) Since the gain is always positive, inputs that receive feedback become dependent on the output voltage. Thus, the behavior of the circuit can be predicted by substituting V_{OUT} (or its function) for the appropriate input voltage.

For example, in a basic multiplier with single-ended inputs and no offset, X_2, Y_2, and Z_2 all equal zero. Feedback enters directly through the Z_1 input. Because converter Z drives the output amplifier's inverting input, the feedback is negative and the output voltage is given by:

$$V_{OUT} = A\,(X_1Y_1/SF - V_{OUT})$$

When A approaches infinity the equation gives:

$$V_{OUT} = X_1Y_1/SF$$

Applying the feedback through a voltage divider increases the overall gain. For example, if a 10:1 attenuator makes

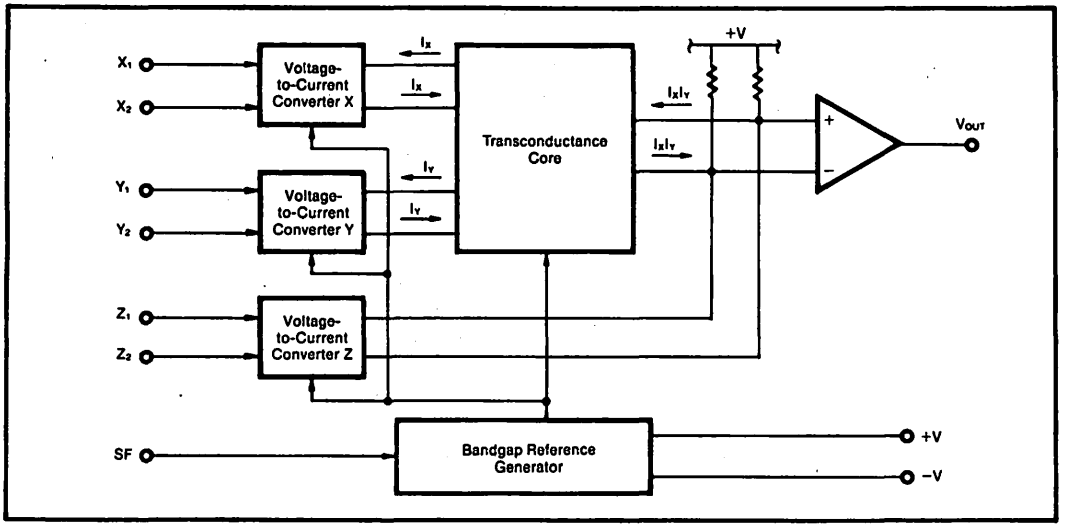


FIGURE 1. The MPY634 multiplier chip is the first to break the 1MHz barrier without the external wideband amplifier, making it a suitable alternative to diode mixers. It combines three voltage-to-current converters, a transconductance core, a voltage reference, and an output amplifier.

Applying the feedback through a voltage divider increases the overall gain. For example, if a 10:1 attenuator makes Z_1 equal $0.1V_{OUT}$, as gain becomes infinite the open-loop equation becomes:

$$V_{OUT} = 10X_1Y_1/SF$$

To make a divider circuit, single-ended inputs X_2, Y_1, and Z_2 are grounded. The feedback is applied to Y_2 so that it is negative for positive values of X_1. However, if X_1 is negative, then Y_2 is grounded and the feedback is applied to Y_1. In either case, the open-loop equation is:

$$V_{OUT} = A\left[\frac{(X_1)(-V_{OUT})}{SF} - Z_1\right]$$

As gain approaches infinity, V_{OUT} becomes Z_1/X_1SF.

The scope of the multiplier chip becomes apparent in a highly accurate voltage-controlled filter. Two multiplier chips, a universal active filter chip, four resistors, and six bypass capacitors team up to form a second-order filter with high-pass, low-pass, and bandpass outputs (Figure 2). The multipliers act like linear voltage-controlled resistors that set the filter's center frequency and thus the cutoff frequency of the high- and low-pass outputs. Although the active filter chip allows a compact implementation for bandwidths up to 200kHz and a Q of up to 500, the bandwidth can be extended to 1MHz by implementing the filter with discrete op amps instead.

Precision 1% resistors ensure accurate values for the full-scale center frequency and for Q. Two such resistors, between each multiplier's output and the filter chip, determine the full-scale frequency, which is the center frequency of the bandpass for a 10V control voltage. In operation, a control voltage drives both multipliers at once and must always be greater than 0V. If the voltage falls to zero or goes negative, the feedback around the filter chip is lost and the circuit becomes unstable.

With 0.1% resistors, the filter holds its full-scale frequency to 2% over a 10:1 range of control. Moreover, no external trimming adjustments are required, unless accuracy must be raised even further (in which case the input offsets can be nulled by trimming). The bandpass and cutoff frequencies drift no more than ±50ppm/°C over −55°C to +125°C. At a full-scale frequency of 25kHz, the wideband noise is typically less than 160μV. The output swing can go as high as 20V p-p, yielding a dynamic range of 96dB.

Limits on the slew rate of the amplifiers inside the universal active filter restrict the input amplitude and Q. First, since the filter's internal amplifiers handle a maximum slew rate of 6V/μs, the full power bandwidth (10Vpk) is 100kHz compared with the small-signal bandwidth of 200kHz. As a result, the input voltage should be limited to 20V p-p below 50kHz and 2V p-p between 50 and 100kHz. Above that, the maximum input voltage is determined by the formula $f_C/50{,}000$, where f_C is the filter's cutoff frequency. Second, a high Q can make internal voltages larger than the input swing. Thus the maximum Q is below 4kHz and $f_C/20{,}000$ above 4kHz.

The high performance of this voltage-controlled oscillator justifies the use of the multiplier and the universal active filter. Though a switched-capacitor filter and a voltage-controlled oscillator represent an easier and less costly alternative, the arrangement's 75dB dynamic range and 30kHz upper frequency fall far short of the multiplier-based configuration. Moreover, the switched-capacitor approach suffers from clock feedthrough and aliasing, which dictate additional filtering.

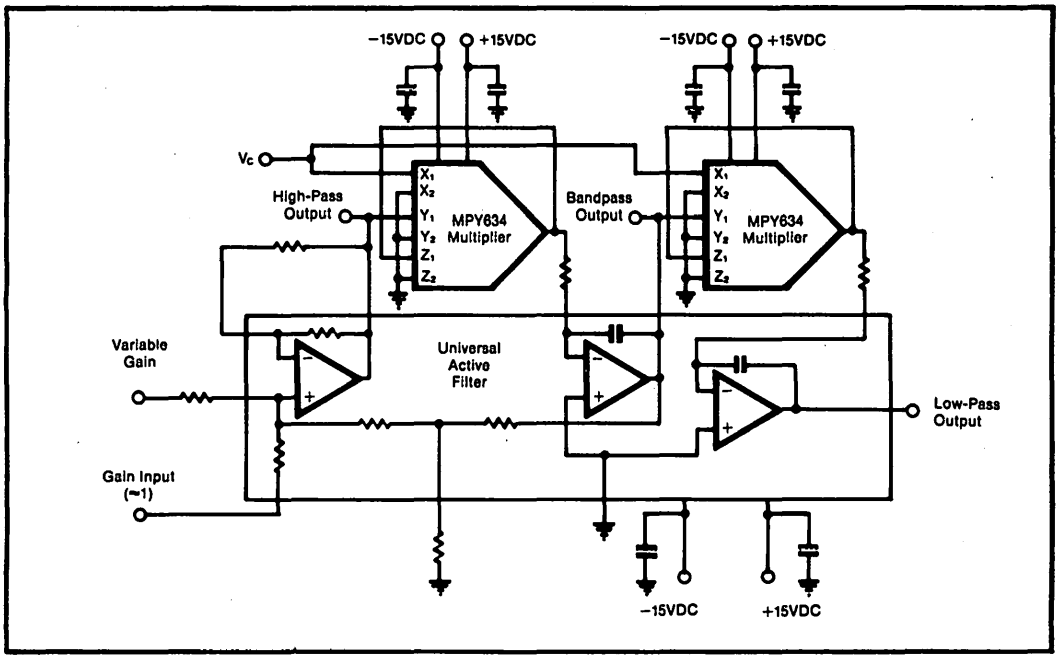


FIGURE 2. A voltage-controlled second-order filter revolves around two multiplier chips and a UAF21 universal active filter. The multipliers act as linear voltage-controlled resistors that vary the center and cutoff frequencies of the active filter chip. Bandwidths up to 200kHz and Q values up to 500 can be attained with just a handful of components.

Since this transconductance multiplier needs no external circuitry to attain its wide bandwidth, it is a particularly good choice for building low-cost mixer circuits (see "Strike up the Bandwidth"). Mixers form the heart of heterodyning, which is used for modulating and demodulating signal amplitude.

A ring-diode circuit, one of the most common types of mixers, performs well at high frequencies but suffers numerous limitations. For instance, since the diodes in the ring must be biased, transformers must be coupled at the mixer's input and sometimes at the output. Unfortunately, transformer coupling precludes low-frequency operation. The low-end frequency of most diode mixers is limited to several hundred kilohertz, preventing them from modulating rf signals directly with audio signals.

On the other hand, the transconductance mixer is directly coupled and thus can modulate audio signals directly onto an rf carrier. For example, the amplitude of a 10MHz carrier can be modulated simply by applying an audio signal to the X input of the multiplier chip and feeding the output of a 10MHz local oscillator to the Y input.

A ring-diode mixer also requires a resistive impedance, usually 50Ω, at its input and output ports. A reactive impedance can severely degrade performance. The transconductance mixer, in contrast, is relatively insensitive to I/O impedances. At low frequencies, its input impedance is 10MΩ and, at about 1MHz, that starts to drop off, falling to a low of 25kΩ at 10MHz. If required, a 50Ω resistor can be shunted across the input to match impedances. The output is insensitive to load impedances greater than 2kΩ and less than 1000pF.

Transconductance mixers exhibit better linearity than typical double-balanced diode mixers (see the table). The input voltage to diode mixers is applied directly to the diode junction, so that the region of linear operation is small. Any nonlinearity causes harmonic distortion and feedthrough, which adversely affect almost all specifications. In addition, it generates spurious carriers, intermodulation distortion, and increased feedthrough. Within the transconductance mixer, the input voltage is converted into a current before being applied to the core, affording a much wider range of linear operation.

One mixing application combines a 1kHz low-pass filter with a 5MHz local oscillator to create a bandpass filter with an extremely high Q of 5000—normally an impractical if not impossible achievement. In a passive network, reaching that Q would necessitate many poles, which are difficult and costly to tune. In addition, a typical active circuit version would require expensive op amps with high gain-bandwidth products.

The input signal is first multiplied by the local oscillator and then sent through the low-pass filter (Figure 3). Since the filter has a 1kHz bandwidth, it passes all incoming components between the local oscillator frequency and 1kHz above it. The filter's output is then reconverted into the original frequency by multiplying it by the local oscillator output. An image frequency is

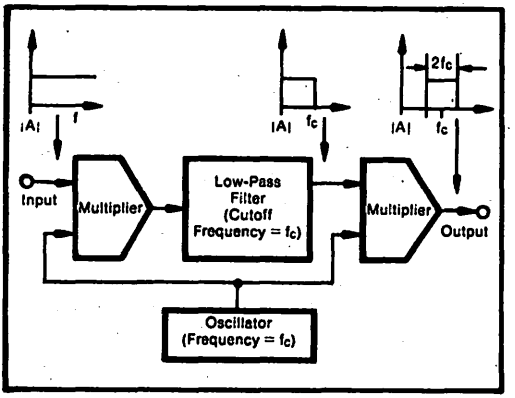


FIGURE 3. In a frequency-mixing circuit, one multiplier chip converts the input signal into DC, and another translates the DC signal back into the original frequency. With this technique, a 1kHz low-pass filter and a 5MHz local oscillator create a bandpass filter with an effective Q value of 5000 and a 5MHz center frequency.

created when the signal is reconverted. The circuit can also translate the center frequency of a bandpass filter, a useful feature when the required filter falls outside of the commonly available communications frequencies.

The mixer circuit can also be adopted for phase detectors; the designer need only connect a low-pass filter to the multiplier chip's output (Figure 4). The configuration follows the principle that the product of two signals of equal frequency contains a DC component, and that component is proportional to the cosine of the angle between the signals.

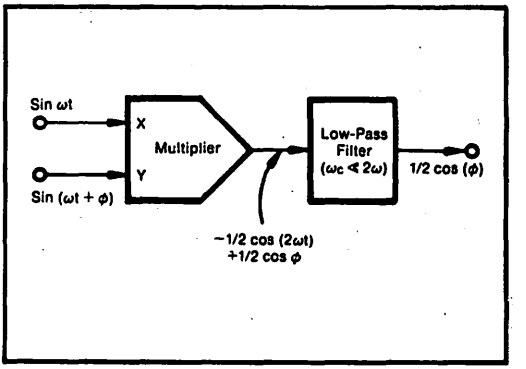


FIGURE 4. The multiplier chip works in a phase detector. When two signals of equal frequency are multiplied, the operation produces a DC component proportional to the cosine of the angle between them.

COMPARING DOUBLE-BALANCED MIXERS

Specification	Typical Double-Balanced Diode Mixer	Multiplier Chip	
		DC to 0.5MHz	0.5 to 10MHz
Carrier Feedthrough	25dB	60dB	40dB
Isolation: RF Input to Local Oscillator	40dB	60dB	40dB
Local Oscillator to Mixer	30dB	60dB	40dB
RF Input to Mixer	25dB	60dB	35dB
Third-Order Intermodulation Intercept	1V rms	50V rms	2V rms
Frequency Range	Several kHz to several GHz*	DC to 10MHz	DC to 10MHz

*The frequency range for any one mixer is usually about three decades.

STRIKE UP THE BANDWIDTH

The limited bandwidth of transconductance multipliers is customarily attributed to the output amplifier. Though the bandwidth of the MPY634 multiplier chip can be kept to 50MHz by the core transistors, the output amplifier slashes that figure to 1MHz. The drop is caused by interaction between the core's output resistance and the large Miller capacitance at the amplifier's input, creating a pole at about 1MHz.

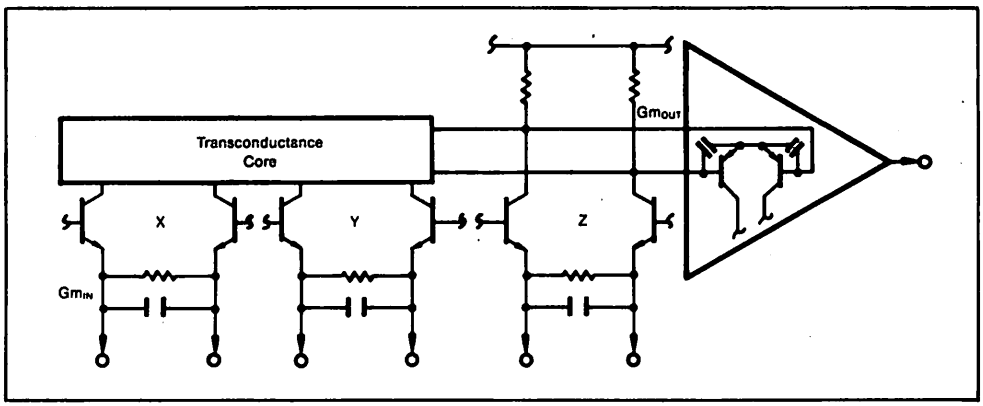
Designers have usually compensated for that interaction by making the output amplifier's −3dB cutoff frequency occur at or before the pole. However, the new chip shifts out that pole in frequency, so that the gain can be sustained far beyond 1MHz. Keeping the gain constant, however, mandates an unchanging ratio of transconductances in the output and input amplifier stages. To keep the ratio constant over a wide band, the input stage's transconductance, Gm_{IN}, must decrease at the same rate that the output transconductance, Gm_{OUT}, does for increasing frequency.

The gain of each input amplifier is the ratio of its load impedance to the transconductance of the input amplifier stage (see the figure). Also, the overall transconductance of the output stage is the output resistance of the core plus the input capacitance and transconductance of the output amplifier. This lumped value looks like a direct load to voltage-to-current converter Z and to the core. Since the core is transparent to converters X and Y, they see Gm_{OUT} as the direct load. Moreover, because Gm_{OUT} represents the load impedance for all the converters, the wideband gain is Gm_{OUT}/Gm_{IN}.

For Gm_{OUT}/Gm_{IN} to remain constant over a broad frequency range, the RC time constants of both transconductances must be within 100% of each other. Fortunately, with worst-case process and temperature variations, the match between the RC time constants can be held to within 20%.

In this multiplier chip, a reactive element of the input stage keeps the transconductance ratio constant. The element, a small nitride capacitor, parallels the normally high resistance Gm_{IN}. In fact, this purely resistive transconductance causes Gm_{OUT} to limit the bandwidth in the first place.

The resistive portions comprise thin-film resistors that can be matched to within 1%. The capacitive portion of Gm_{OUT} depends mainly on the quiescent current of the output amplifier's differential inputs. That current is laser-trimmed to a known value. Consequently, only the absolute tolerance of the added nitride capacitor determines the match between the capacitive portions of Gm_{OUT} and Gm_{IN}.



The substance of this application note appeared in article form in the January 9, 1986 issue of *Electronic Design*.

CURRENT TRANSMITTER IC CATERS TO HIGH-LEVEL SIGNALS AND TIGHT BUDGETS

When process control signals must travel far, a transmitter chip steps in, supplying the drive while alleviating cost and space worries.

In the past, designers of process-control systems have had to opt for either bulky modules or "home-brewed" circuits to transmit current to run remote actuators from high-level control signals over long distances. Unfortunately, modules add expense, and in-house circuitry not only sacrifices valuable board space but also gobbles up costly resistors having low temperature coefficients.

Integrated circuits present a new option. For example, in the industry-standard 4 to 20mA range, the XTR110 current transmitter can convert 0–5V or 0–10V inputs into a current output with an end-point accuracy of 0.2% and an overall nonlinearity of below 0.005%. This 16-pin DIP circuit operates with one inexpensive external transistor and incorporates an accurate 10V reference.

The characteristics of the transmitter chip suit it not only to process-control systems but to other demanding applications as well. For instance, when teamed with the transmitter chip, a test system can receive current signals from remote equipment over a pair of wires while maintaining an integrity of 12 bits. Indeed, the current signals can travel to a series of test stations in daisy-chain fashion, picking up only minimal, easily filtered noise along the way.

Other system designs may benefit from the fact that current-mode signals, unlike their voltage counterparts, need not return to a single ground; instead, they can terminate in a dirty ground (see "The Care and Feeding of Current Transmitters", page 5). Finally, bridge networks, in which a transducer serves as one arm, behave in a linear fashion if driven by current, but in a nonlinear manner if driven by voltage.

The current transmitter contains three basic functional blocks: a 10V bandgap reference and two operational amplifiers (Figure 1). The first op amp, A_1, drives an internal NPN transistor whose emitter is fed back into the op amp's inverting input. That unity-gain configuration makes the emitter's voltage match the voltage appearing at A_1's noninverting input—a value representing the summation of the three inputs V_{REF} In, V_{IN1}, and V_{IN2}.

A resistor from the emitter to ground sets the collector current of the NPN transistor, based on the expression:

$$I_C = (V_{REF}\,In/16 + V_{IN1}/4 + V_{IN2}/2) / R_{SPAN}$$

Here I_C is the collector current, and R_{SPAN} is a resistance connected from the Span Adjust pin to ground. The equation ignores base-current error, since the actual circuit uses a compound Darlington arrangement instead of the NPN transistor, thus nearly eliminating the effects of base current.

The second op amp, A_2, takes the collector current of the NPN transistor and mirrors it with a gain of 10. Then a 500Ω resistor converts that current into a voltage at the amplifier's noninverting input. The output of this op amp drives the gate of an external P-channel power MOSFET, whose source is connected to the inverting input and to a 50Ω resistor. That setup resembles the unity-gain configuration of A_1, except that it uses the positive supply instead of ground as a reference.

The MOSFET, which can be considered the output device of A_2, keeps the power dissipation away from the chip, and thus preserves its linearity and endpoint performance. A_2 maintains an equal voltage across the 50Ω resistor. Moreover, the 10:1 ratio of the resistors creates a drain current through the MOSFET that is ten times the collector current of the NPN transistor. With that drain current being the output variable, I_{OUT}, the system transfer function is the desired $I_{OUT} = 10\ I_C$.

The 10V reference within the current transmitter supplies the internal bias for the chip. However, it can also be used to offset the output current or to perform other reference chores with its extensive drive capability.

To establish the reference, the V_{REF} Force pin must be shorted to the V_{REF} Sense pin, thereby closing a feedback loop for the internal voltage regulator. If a system demands more than the reference's rated 10mA output, an external current-boosting NPN transistor can be used, with its collector connected to the positive supply, its base to V_{REF} Force, and its emitter (that is, its output) to V_{REF} Sense.

THE HEAT IS ON

Although the 4 to 20mA output of the current transmitter is not excessive, it can lead to a phenomenon known as resistor self-heating under measurement conditions. Since a resistor has a finite thermal resistance, the load resistor can be affected by its own heat. Its temperature coefficient forces the resistor's value to change: the higher the TC, the heavier the toll on transfer accuracy and linearity.

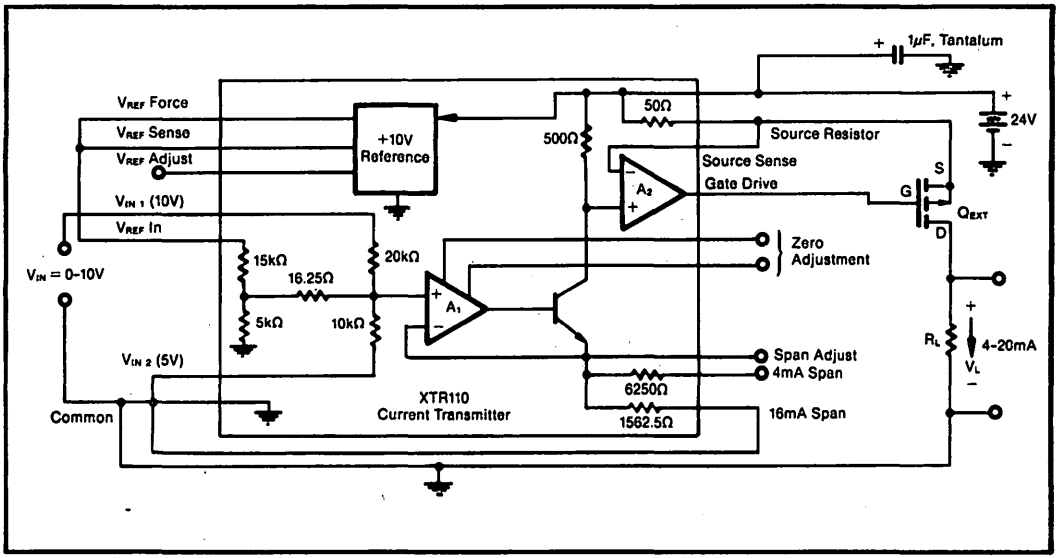


FIGURE 1. The XTR110 current transmitter contains three main functional blocks: a 10V reference circuit and two operational amplifiers. The extra transistor, which keeps power dissipation away from the chip, is the only external component needed for basic operation.

Take, for example, a typical 0.25W, 250Ω load resistor that has a thermal resistance of 320°C/W and a temperature coefficient of 50ppm/°C. As current varies from 4mA to 20mA, the resistor's value deviates by 0.15%. (In the calculation, the power difference between the two current levels multiplied by the thermal resistance is the change in the resistor's temperature. That change is factored with the temperature coefficient to produce the change in resistance.)

Even a change in resistance of just 0.15% could make a significant dent in the error budget for the system. So designers obviously should worry about more than the end-point change. Since the calculation of change in resistance depends on a current-squared term, the entire circuit departs from linear performance. In fact, change in resistance, considered as a function of current at values intermediate to the end points, reveals a curved transfer function that illustrates the nonlinearity error contributed solely by the resistor (Figure 2).

Thermal resistance contributes most to the error. To surmount that limitation, resistors with higher power ratings can be used, or the power can be spread over more resistors. Placing four 1kΩ resistors in parallel, for example, produces one-fourth the thermal resistance of a 250Ω resistor. Resistors with a temperature coefficient of 10ppm/°C or less—such as wire-wound and thin-film types—also improve the measured current transmission performance.

To accommodate some pressure transducers, an external 20Ω source resistor and a jumper wire can select a second output range—10mA to 50mA—for the current transmitter (point A in Figure 3). The circuit should be carefully laid out with the Source Sense feedback connection made as close to the external resistor as practical, thereby minimizing series parasitic resistance from the

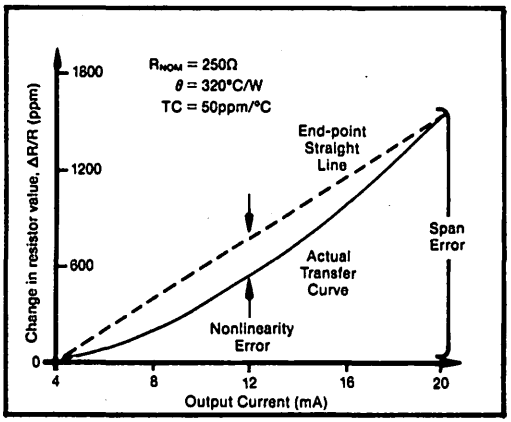


FIGURE 2. Resistor self-heating introduces a current-squared term into the error calculations for the current loop. As a result, the current transmitter could exhibit nonlinear behavior. Improved design practices, such as spreading the power across a parallel combination of larger resistors, can reduce this effect.

metal pattern on the printed circuit board. Although the metal traces exhibit little resistance, they can have a high temperature coefficient and consequently can influence span drift.

THE CLOSER YOU GET

Similarly, the supply side of the source resistor should be connected as close as possible to the $+V_{CC}$ pin of the current transmitter. The user can compensate for variations in the 20Ω resistor by trimming at the Span Adjust pin. Any parasitic resistance from the Source Sense pin to the MOSFET's source is outside the feedback loop and thus can be ignored. As a result, the transistor can be positioned in areas suitable for heat-sinking without affecting system performance.

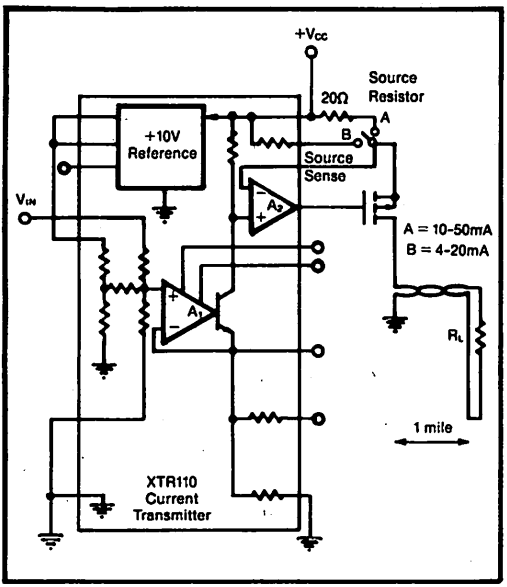


FIGURE 3. An external 20Ω resistor and a jumper (point A) can select a second output range of 10 to 50mA for the current transmitter.

If system design requirements can stand a slight drop in end-point accuracy and linearity, a garden-variety bipolar PNP transistor can replace the more expensive power MOSFETs. For instance, a TN2905 in a TO-92 package performs adequately, suffering only slight degradation in supply rejection and linearity.

The shift in the offset current can be calculated by dividing the nominal value (4mA) by the transistor's beta. For a beta of 250, the offset changes by 16μA, or 0.10% of the desired 4 to 20mA span. Of course, variations in beta also shift the span itself. Just how much can be found by dividing the nominal span (16mA) by beta—yielding a change in span of 64μA, or 0.40% of the nominal value.

An external resistor, R_{PAD}, can augment the internal 50Ω source-sensing resistor to correct the transistor's base-current loss (Figure 4). A 20kΩ trimming potentiometer or a carbon resistor suffices. Drawing on the fractional change in the current span (ΔSpan/Span) described above, the correction could be calculated as:

$$R_{PAD} = 50\ (\text{Beta} + 1)$$

These calculations assume that the transistor's current gain is fixed. But in practice, the beta varies as the transistor dissipates power and its junction temperature rises. The temperature change can be figured if the transistor's thermal resistance is known.

The transmitter chip runs from a 24V supply, and the current varies from 4 to 20mA. Because the transistor is in series with the 50Ω source resistor and the 250Ω load resistor, minimum and maximum power can be established at 91.2mW and 360.0mW, respectively. The thermal resistance, 200°C/W, elevates the junction temperature by 53.8°C.

The beta of a transistor has a typical temperature coefficient of 5000ppm/°C. By calculating the shift in span, beta becomes 317 and the shift, 50μA, or 0.31%. Note that the span shifts by almost 0.10% less than first determined but still could trouble an unsuspecting designer.

Here too, power does not vary linearly with current, because the resistive portion contributes a current-squared term. Although nonlinearity for this particular case degrades only 0.01% across the entire transfer curve, the design still must accommodate that additional deviation. Different transistors, of course, will produce different results.

Heat-sinking minimizes the effect of temperature on beta and allows the current transmitter to reach optimum performance. System designers also should remember that thermal effects become evident over a period of milliseconds rather than instantaneously.

Valve drivers and certain other actuators require that the current must not only be accurate but bipolar as well. The current transmitter—teamed with an external quad op amp, two power MOSFETs, a small-signal transistor, and a handful of resistors—can act as a current pump to meet this requirement (Figure 5). Basically, the transmitter chip serves as a variable current source in parallel with a fixed current sink, which is itself biased at half the full-scale source current and thus provides a constant offset.

In this pump circuit, a transconductance amplifier (A_4, Q_3, R_3, and R_5) translates the +10V reference input into a current. In turn, that current drives a current-mirror multiplier (A_3, Q_2, R_2, and R_4) which works as the current sink. In addition, A_5, R_9, and R_{10} can be used to adjust offset by forcing the current transmitter to source

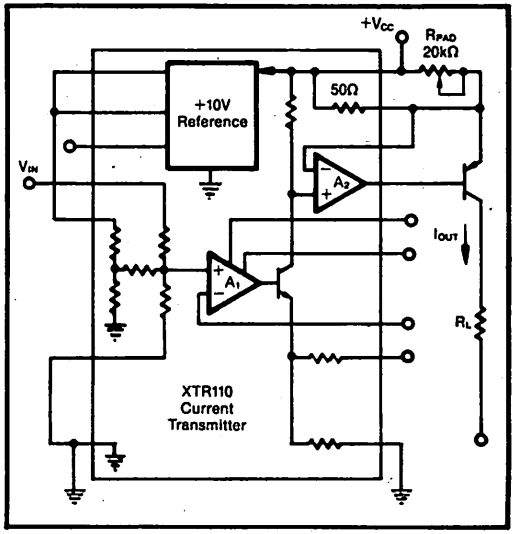


FIGURE 4. A fixed resistor or 20kΩ trimming potentiometer, R_{PAD}, corrects for variations in beta when a less costly PNP transistor is used instead of a MOSFET at the output of the current transmitter.

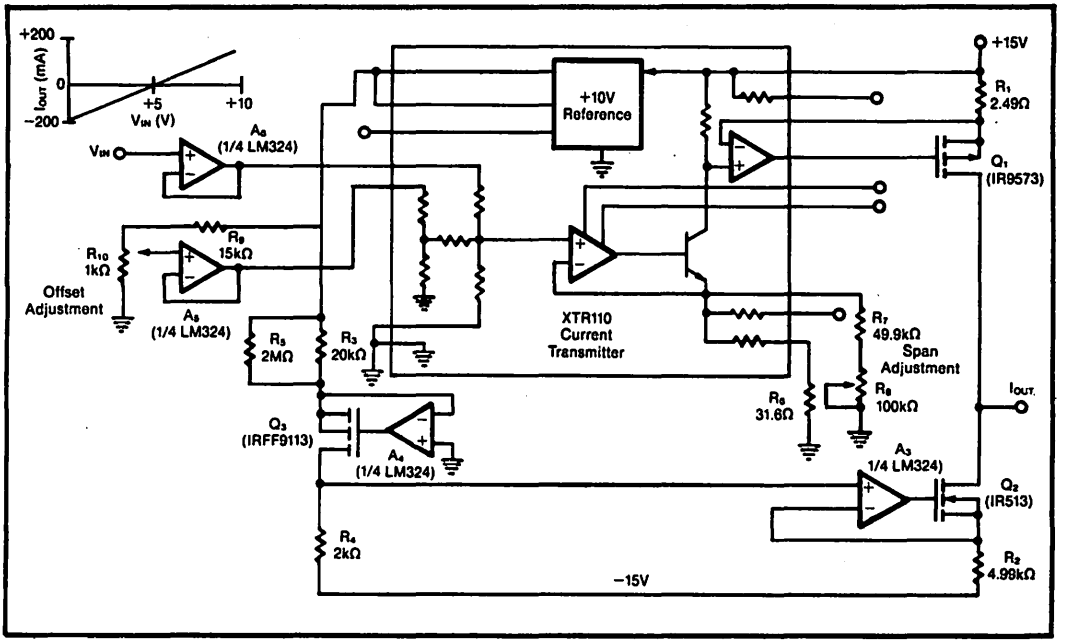


FIGURE 5. Alterations to the support circuitry to the current transmitter allow it to accommodate actuators that require a bipolar current. Resistors R_1 and R_2 feature low temperature coefficients and dissipate just 0.2W continuously; R_8 and R_{10}, two 10-turn potentiometers, afford great sensitivity.

some constant current from Q_1. Resistor R_5 in the transconductance amplifier should be selected to set the current sink a bit high in anticipation of the adjusted offset current sourced by T_1. If required, high-impedance buffer A_6 can be configured for gain.

The circuit includes both offset and span adjustment circuitry to compensate for the 1% tolerance of the resistors and the inherent offsets of the op amps. Span adjustment resistors R_6, R_7, and R_8 keep the span unchanged when the trim potentiometer is set at midscale.

The circuit can be modified if the desired transfer function has bipolar inputs of −5V to +5V. In that case, a divider circuit can be connected to the +10V reference to generate a +2.5V tap. A_6 can serve as a buffer off the tap, and its output can be connected to V_{IN2} instead of to V_{IN1}, which now accepts the input.

A POINT OF REFERENCE

The chip's +10V reference can also be used to calibrate data acquisition systems, sourcing 10mA over the specified temperature range. If more current is needed, V_{REF} Source and V_{REF} Sense allow a discrete NPN transistor to be connected for boosting the current.

However, a voltage reference need not be the only standard value used for biasing data acquisition systems. Frequently current can be applied just as easily for the system reference.

Many data acquisition units are built around a current-sinking servo loop (Figure 6). A control amplifier converts the voltage across the input resistor into a current, which is mirrored by the other transistors. The bases of those devices are connected to the amplifier's output. The collector currents of the transistors follow the ratio of their emitter areas and emitter resistors with respect to the control transistor and its resistor.

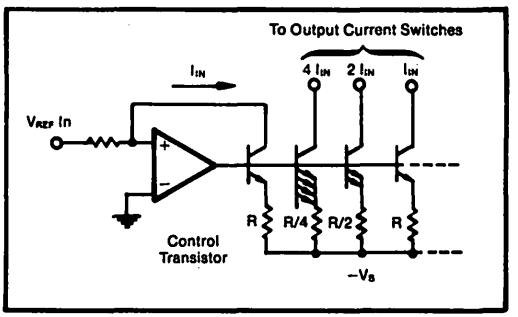


FIGURE 6. The current transmitter can supply a reference current for D/A converters that work on the principle of current replication and multiplication. The current flowing through the transistors depends on a ratio of emitter areas and emitter resistors.

Following that setup, a digital-to-analog converter would work on the principle of current replication and multiplication. In certain applications, as in driving CRT yokes, the absolute value of the D/A converter's output current is important. To drive a pair of 12-bit converters (Figure 7), the current transmitter's output connects to the slider of a balance trim potentiometer, ensuring that each converter has the same full-scale output current. If more than two converters must be scaled, the same principle can be extended by applying resistor current dividers to the paralleled converter reference inputs.

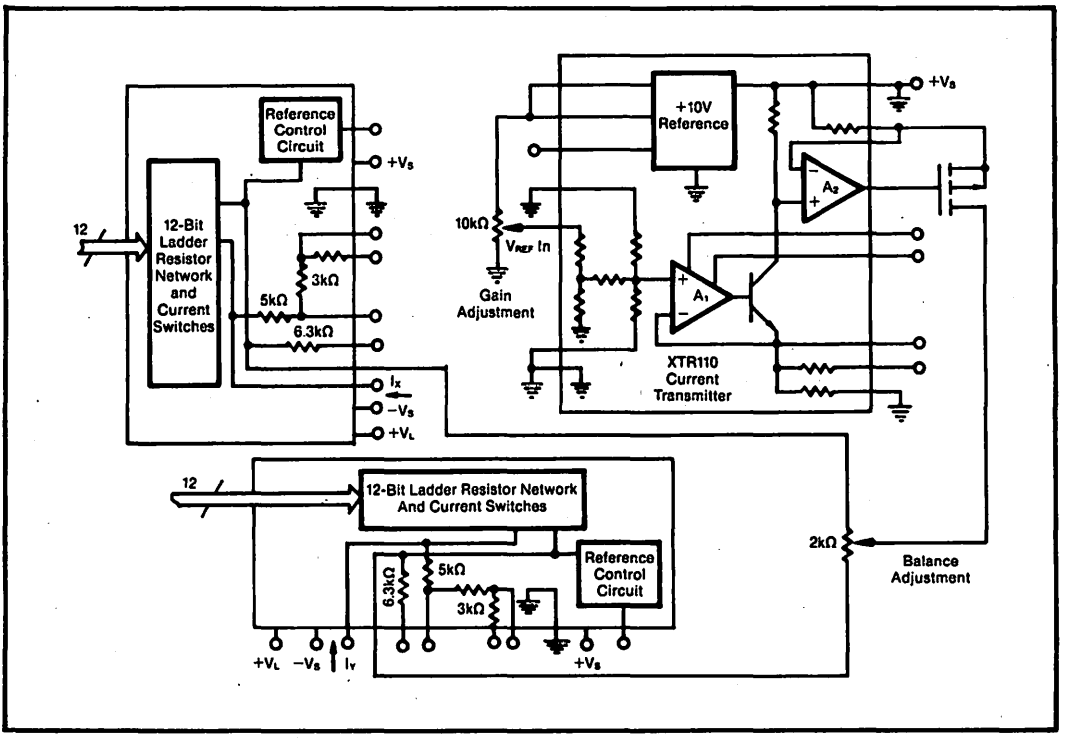


FIGURE 7. To drive a pair of 12-bit D/A converters, the current transmitter feeds its output through a 2kΩ potentiometer, which equalizes the two full-scale output currents.

Small variations in the current transmitter's output permit gain to be adjusted accurately, and large variations can be used for digital multiplication. If a system calls only for the converters' full-scale outputs to be set, a single potentiometer can adjust the current transmitter's output current. The potentiometer should be connected between the +10V reference and ground, with its slider to the V_{REF} In pin.

THE CARE AND FEEDING OF CURRENT TRANSMITTERS

Getting the most out of the XTR110 current transmitter is as simple as following a few basic rules. First and foremost, designers should pay close attention to the way that output current affects system ground, since the flow of current can modulate individual circuit grounds.

A floating ground may be of no consequence if all the signals of interest are relative to local ground. For example, if the signal from a resistance-temperature detector or a thermocouple is amplified at the same site as the current transmitter, no confusion exists over the integrity of the ground. On the other hand, if a host controller drives the current transmitter from many feet away, the designer must consider errors induced by the drop in ground. Any path that current takes from one point to another should have a return path as well; otherwise the transmitter chip could not draw current from the MOSFET, and no voltage would develop across the load resistor. Although that cautionary measure may seem self-evident, designers sometimes inadvertently overlook the return path if the load resistor already terminates in a local ground. In any case, the ground for the receiving circuitry should be connected—directly or indirectly—to the current transmitter's ground.

The voltage at the output of the current transmitter (that is, the drain of the MOSFET) is not critical. For example, the current could return to a negative supply without affecting the circuit's linearity or accuracy. The positive compliance voltage must be 2V lower than the current transmitter's positive supply, plus the IR drop from the drain-to-source on-resistance of the MOSFET. The breakdown voltage of the MOSFET determines the negative compliance voltage.

TWO-WIRE TRANSMITTER PROMOTES PAINLESS PROCESS CONTROL

Faced with low signal amplitudes and high electrical noise, control and data acquisition system designers need all the help they can get. Lending a hand is a small monolithic that resists noise and reduces cost.

Pity the process-control designer: he is charged with delivering miniscule signals reliably through hostile environments over long distances, and as always, he is asked to do it as simply and as cheaply as possible. Fortunately, these demands, though not trivial, can be met.

A crucial link in the chain of components that forms the solution is the signal transmitter. It influences the number of transmission lines, the transmission type, and ultimately, the system's overall noise immunity.

Among the better choices for this part is a current-mode two-wire signal transmitter that, as its name implies, connects the ends of a transmission system with a single pair of twisted wires. Both signal and power travel together, avoiding exotic, expensive transmission cable (see "The Transmission System Choices").

What's more, a recent two-wire transmitter implemented as a monolithic circuit represents a breakthrough in performance. The XTR101 gives designers a small, inexpensive signal conditioner that converts low level signals into a standard 4mA to 20mA output. Not only does it amplify small signals, but it also provides excitation for strain-gauge bridges, RTDs (resistance temperature detectors), and thermistors. And it does so with 12-bit accuracy between −40°C and +85°C, with loop voltages of 11.6VDC to 40VDC. The package is small enough (0.7" by 0.3" by 0.15") to fit inside many transducer packages.

Placing the XTR101 near the sensor reduces errors in a hostile electrical environment and also minimizes the need for expensive shielded sensor wire.

Finally, because a current level instead of a voltage level is used, the transmitted signal is unaffected by noise voltages or contact potentials. Current-mode transmission also eliminates crosstalk even when wires are bundled together, and high-signal-level transmission means inexpensive unshielded copper wire can be used. Also, by transmitting current instead of a voltage, the voltage drops caused by line resistance do not cause measurement errors. The 4mA minimum current, which is necessary to supply power to the XTR101 and power the two excitation 1mA current sources, has the added benefit that a broken line (0mA) can be distinguished from the minimum input signal of 4mA. Even current-induced errors are suppressed by using the simple twisted-wire pair.

In operation, amplifiers A_1 and A_2 act together as an instrumentation amplifier controlling a current source, A_3 and Q_1 (see Figure 1). An internal feedback loop, completed by an external resistor, sets the operating point. Input voltage e_1, applied to pin 3, appears at pin 5; and e_2, applied to pin 4, appears at pin 6. Thus the current in the spanning resistor, R_S, is $I_S = (e_2\text{-}e_1)/R_S = e_{in}/R_S$, where e_{in} is the input voltage differential. This current is added to internal current I_3; and the sum, I_1, controls I_2, which is set to be 19 times greater.

In a 4mA to 20mA current loop, the output current's lower limit of 4mA occurs when $e_{in} = e_2 - e_1 = 0V$. The components of the 4mA current are a 2mA quiescent current driving into pin 7 and 2mA drawn from both of the current sources.

The upper limit of the output current, 20mA, is set by properly selecting R_S, based on the upper limit of e_{in}. In this case, R_S is chosen to give a 16mA output current span, or $[(0.016mA/mV) + (40/R_S)]\ e_{in}(\text{full scale}) = 16mA$. Also, since the output current, I_{out} is unipolar, e_2 must always be larger than e_1; and to keep I_{out} at 20mA or less, e_{in} must be less than 1V when $R_S = \infty\Omega$ and proportionately less as R_S is reduced.

The majority of the 16mA current can be off-loaded to an external transistor as shown in Figure 1. In this way the self-heating of the XTR101 is dramatically reduced for a factor of 25 less self-induced thermal drift.

One purpose of the XTR101's self-contained dual current sources is to simplify temperature measurements. Consider one application in which a platinum RTD with a resistance of 100Ω at 0°C and 200Ω at 266°C is needed to transmit 4mA at 25°C and 20mA at 150°C (Figure 2). Here the RTD is excited with one of the 1mA current sources, while the other source is used for zero suppression, an input biasing technique.

USING THE CURRENT SOURCES

To start, feedback resistor R_S is picked so that the intended temperature span produces a full scale current

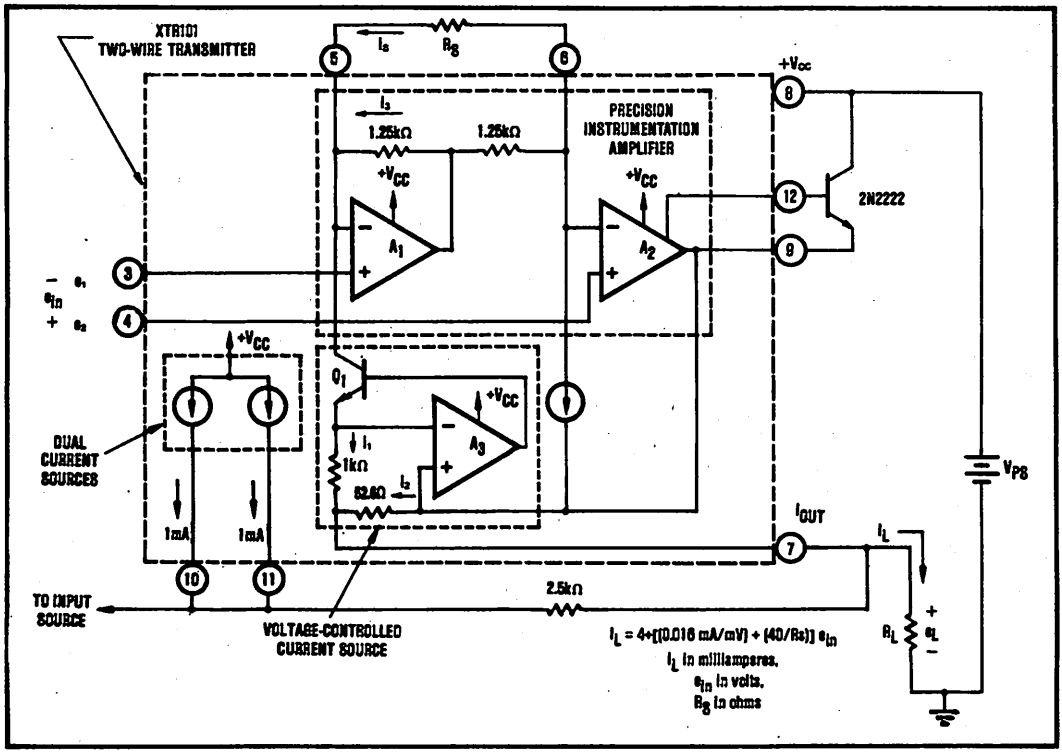


FIGURE 1. A two-wire transmitter in hybrid IC form, the XTR101 modulates the power supply current with changes in the input voltage, e_{in} (at pins 3 and 4). In addition, the circuit contains two 1mA current sources for powering transducers.

swing. First, the sensitivity of the RTD, $\Delta/R\Delta T$, is defined as 100Ω/266°C. Thus, when excited with a 1mA current source and exposed to a 25°C to 150°C temperature range, the span of e_{in}, will be

$$1mA \times (100\Omega/266°C) \times 125°C = 47mV$$

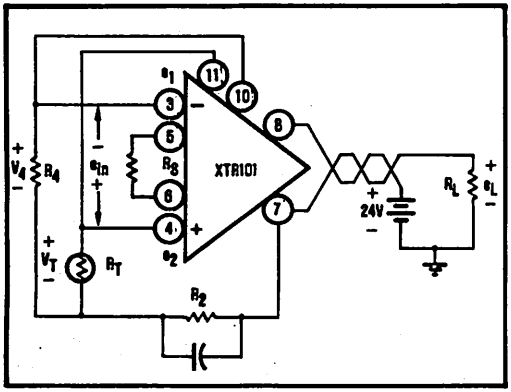


FIGURE 2. In applying the XTR101 in a temperature-measuring circuit, the operating point is fixed by the span resistance, R_S, a zero-suppression voltage across R_4, an input biasing voltage across R_2, and of course the resistance of the RTD.

The equation for R_S is obtained by differentiating the transfer function to obtain the change in the load current, I_L, divided by the change in e_{in}; in other words $\Delta I_L/\Delta e_{in}$, and then solving for R_S. That is:

$$R_S = \frac{40}{(\Delta I_{out}/\Delta e_{in}) - (0.16mA/mV)}$$

CHOOSING THE RESISTOR VALUES

With $\Delta I_{out} = 16mA$ and $e_{in} = 47mV$, R_S is 123.3Ω. This value of R_S sets the instrumentation amplifier's gain so that an RTD full scale input voltage change of 47mV produces a full scale output current change of 16mA. Next, R_4 is chosen to place the 16mA output span between 4mA and 20mA. For this case, when $e_{in} = 0$, $I_L = 4mA$. Analysis of the loop voltage from pin 4 to pin 3 yields $e_{in} = V_T - V_4$. Thus, when $e_{in} = 0$, $V_4 = V_T$, and V_T is given by

$$V_{T25} = 1mA \times \left[100 + \left(\frac{100\Omega}{266°C} \times 25°C\right)\right]$$
$$= 109.4mV$$

Since R_4 is excited by the second 1mA current source,

$$R_4 = 109.4mV/1mA$$
$$= 109.4\Omega$$

In applying the XTR101, it is both convenient and helpful to think of it is a single-supply instrumentation amplifier

where pin 7 is ground and pin 8 is V_{CC}. As with any single-supply amplifier, the input voltages must be biased with a common-mode voltage to keep the input transistors operating linearly. In the case of the XTR101, biasing requires that pins 3 and 4 be kept between 4V and 6V above pin 7. That is done by having both current sources flow through a resistor, R_2, located between pin 7 and the inputs. Making $R_2 = 2.5k\Omega$ produces a 5V drop. The input voltages, with respect to pin 7, are then

$e_1 = 5V + 0.1094V$
e_2 (min) $= 5V + 0.1094V$ (occurs at 25°C)
e_2 (max) $= 5V + 0.1564V$ (occurs at 150°C)

Thus the 4V to 6V requirement is met.

If it is necessary to place the RTD a significant distance from the transmitter, measurement errors due to the resistance of the cable connecting the RTD to the transmitter can result. In such a case, the dual current sources of the XTR101 and a three-wire RTD connection correct the problem (see Figure 3). Here, if $R_1 = R_2$ (meaning identical wire lengths), and $I_1 = I_2$, equal and opposite voltages (V_1 and V_2) are produced in series with the RTD voltage, canceling the line resistance error.

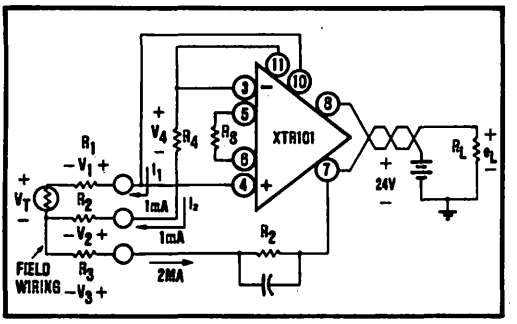


FIGURE 3. When a long line is needed to connect the RTD to the transmitter, errors that might be introduced by line length are reduced by using this three-wire connection to the transmitter. Here, line drops V_1 and V_2 cancel out, since they produce equal voltages on both sides of the RTD.

THERMOCOUPLE SIGNAL CONDITIONING

The XTR101 is well suited for thermocouples, the most popular temperature sensors. Its temperature range of −40°C to +85°C means that it can be placed close to the thermocouple, reducing the need for expensive thermocouple extension wire, as noted. With the dual current references, the function of thermocouple compensation, burnout indication, and zero suppression and elevation all are easily accomplished.

A typical thermocouple application might involve a process temperature range of 0°C to 1000°C. A type J thermocouple produces a voltage span of 58mV for that temperature range and the thermocouple's sensitivity is 52μV/°C at 25°C from standard thermocouple tables. To find R_S, the span-setting, or gain-setting, resistor, recall that

$$R_S = \frac{40}{(\Delta I_L/\Delta e_{in}) - (0.016mA/mV)}$$

Since I_L should span 16mA (4mA to 20mA) when e_{in} changes 58mV (for a 0°C to 1000°C temperature range), R_S is calculated to be 123.3Ω.

COLD JUNCTION COMPENSATION

Remember, thermocouples produce a voltage proportional to the difference in temperature between two junctions. In the example just discussed, one junction is at the process itself and the other at the reference point, where the thermocouple wire is connected to the signal transmitter. To produce an input voltage to the XTR101 that is proportional to the process temperature, it is necessary to create a voltage proportional to the temperature of the reference junction, whatever that may be. This technique of establishing a reference is called cold junction compensation.

A practical way to compensate the thermocouple circuit is to create a known voltage in the thermocouple loop that tracks the temperature of the reference junction. Two common methods are with semiconductor diodes and with RTDs. When the former is chosen (see Figure 4), the loop that forms e_{in} runs from pin 3 to pin 4 and so

$$e_{in} = V_{TC} + V_4 - V_6$$

where V_{TC} is the temperature-compensating voltage; V_6 is created from the diode voltage, V_D, which itself is a function of the diode temperature; and V_4 is in series with V_{TC}. A voltage divider consisting of R_5 and R_6 scales the diode voltage properly and places it in series with the thermocouple voltage loop.

To accomplish that task, the voltage divider must meet two criteria. First, it must make the gradient $\Delta V_6/\Delta T$ the same as the gradient of the thermocouple voltage (52μV/°C at 25°C—obtained from standard thermocouple tables). Second, the impedance level of the divider must be much larger than the diode impedance to prevent loading of the diode voltage.

For the first criterion,

$$\Delta V_{TC}/\Delta T = \Delta V_6/\Delta T$$
$$= \Delta V_D/\Delta T\,[R_6/(R_5 + R_6)]$$
$$52\mu V/°C = 2000\mu V/°C\,[R_6/(R_5 + R_6)]$$

For the second criterion, R_5 is chosen as 2kΩ and solving the last equation yields a value of 51Ω for R_6.

The purpose of V_4 is to set the process temperature corresponding to 4mA of output current, that is, to determine which V_{TC} will produce an e_{in} of 0. For convenience, $V_4 = R_4 \times 1mA$. Also, when the reference junction is at 25°C and the process temperature is at 0°C, e_{in} should be 0.

Transposing the terms of the equation for e_{in} gives

$$V_4 = e_{in} - V_{TC} + V_6$$

so that with $T_2 = 25°C$, $V_6 = 600mV \times (51/2051) = 14.9mV$. Also when $T_{TC} = 0°C$, $V_{TC} = -1.28mV$ (from the thermocouple tables). Then when $e_{in} = 0$, (4mA out), $V_4 = 16.18mV$ and with a 1mA current R_4 is calculated to be 16.18Ω. What's more, varying R_4 achieves zero suppression and elevation as needed, with no interaction between zero and span adjustments.

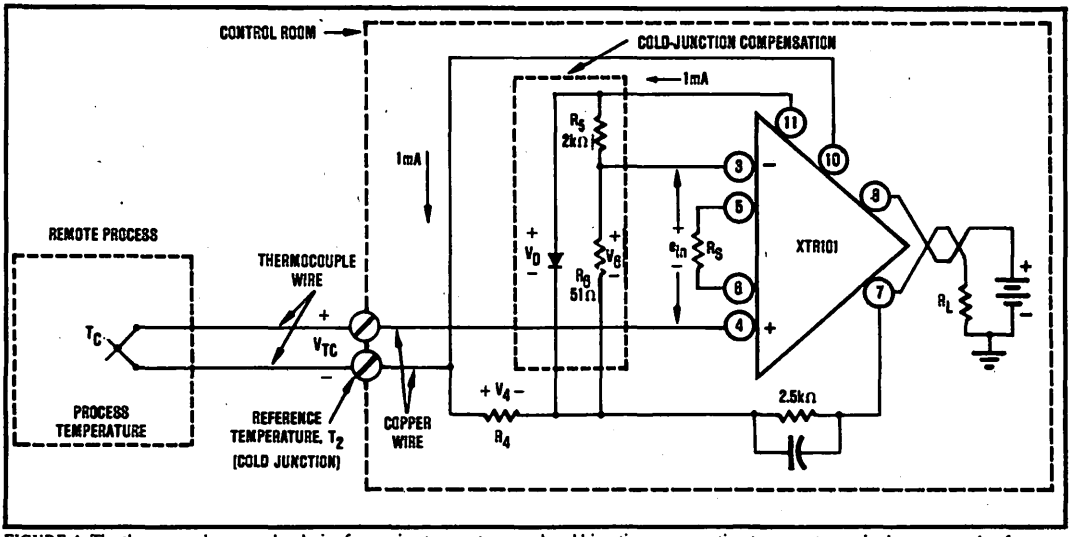


FIGURE 4. The thermocouple, a popular device for sensing temperature, needs cold-junction compensation to generate an absolute output. A reference diode, V_D, tracks the ambient temperature to perform the compensation.

Thermocouples are frequently used in very hostile environments such as hot, corrosive atmospheres, where they often burn out. A convenient way to determine when burnout occurs is to force the two-wire transmitter current beyond its normal range and detect an abnormal condition using a limit or level detector.

DETECTING BURNOUT

With the XTR101, forcing the output above or below its range is done with the input bias currents and hence requires no extra components. When the thermocouple burns out, it opens and its impedance becomes very large. The input bias current flowing into the positive input (pin 4) causes I_L to go to the value of its lower range limit, about 3.8mA. If instead an up-scale indication is needed, a circuit can be built so that when the thermocouple opens, the transmitter's output goes to its upper range limit, about 38mA (see Figure 5).

BRIDGE TRANSDUCERS, TOO

One of the most popular uses of two-wire transmitters is in bridge circuits. These circuits include transducers for

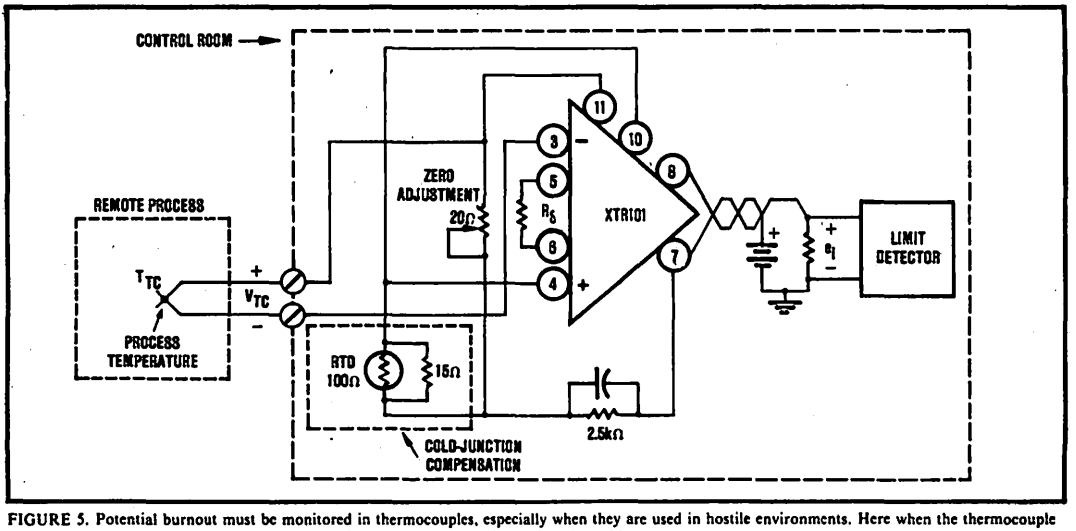


FIGURE 5. Potential burnout must be monitored in thermocouples, especially when they are used in hostile environments. Here when the thermocouple opens (burns out), the transmitter's output goes to its maximum, 38mA, indicating the problem.

measuring pressure, load cells for measuring force and weight, and strain gauges for measuring vibration and acceleration. However, 4mA to 20mA two-wire transmitters impose some special constraints on the selection of a bridge. Because only 4mA is available to power the transmitter and the bridge sensor, the current available for bridge excitation is often too low for some types of bridges. For example, a 350Ω thin-film strain-gauge bridge, which, when excited with 10V, produces a full scale signal of 30mV and draws 28.6mA, would produce only 2.1mV full scale if it were excited with a 2mA current source.

Because of this limitation, diffused semiconductor strain gauges are most often used with 4mA to 20mA transmitters. Such units typically produce a 100mV full scale output when excited with only a 1.5mA current source.

THE TRANSMISSION SYSTEM CHOICES

What are a designer's signal conditioning options? First, there is the brute force technique (see Figure 6A), which has serious disadvantages. For instance, three wires are needed to minimize the effect of line resistance. Also, the signals are transmitted using a voltage mode and are therefore susceptible to voltage noise pickup. Worse, because the voltages are usually very small, good shielding is needed, and even that may not prevent noise.

A second scheme places the amplification at the transducer (see Figure 6B). The advantage here is that the voltage levels are higher—typically 10V full scale. However, now four wires are needed—two for the signal and two for power—and some shielding is still necessary. Moreover, since the line resistance and the input resistance of the control instrument form a voltage divider, the impedance of the control instrument must be high to avoid signal attenuation and higher line impedance results in greater noise pickup.

Finally, there is the two-wire transmitter (see Figure 6C). Only two wires are needed because the power and output signal are carried on the same leads. Furthermore, by using current-mode transmission, shielded wire is unnecessary. A simple twisted pair of copper wires is sufficient, and since current is being measured instead of voltage, the line resistance does not affect accuracy.

A TWO-WIRE TRANSMITTER IN IC FORM

The XTR101 is a 4mA to 20mA two-wire transmitter IC containing a highly accurate instrumentation amplifier, a voltage-controlled output current source, and dual-matched precision current references. These features suit it for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs (resistance temperature detectors), thermistors, and strain-gauge bridges.

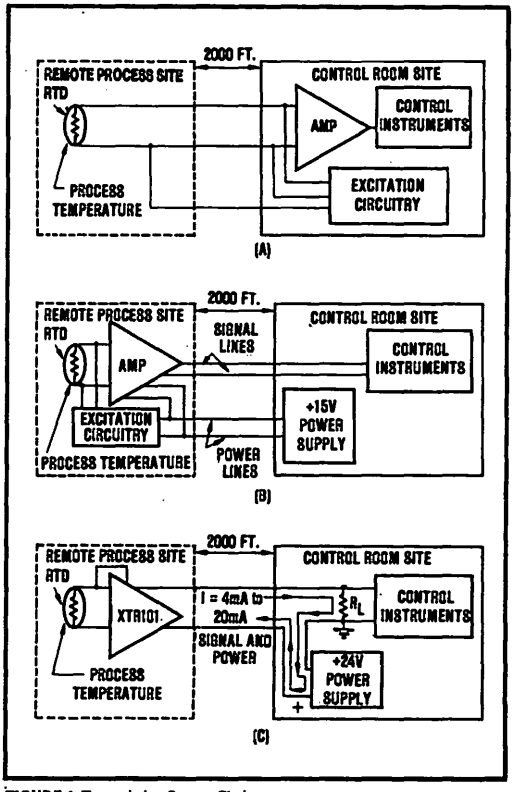


FIGURE 6. Transmission System Choices.

With the two-wire transmitter, signal and power are supplied on a single-wire pair by modulating the power-supply current with the input signal source. The transmitter is immune to voltage drops from long transmission lines, as well as to noise from motors, relays, actuators, and other industrial equipment.

The input stage of the XTR101 is essentially a high performance instrumentation amplifier. Its features include:

High input impedance	400MΩ
Low offset voltage	30μV maximum
Low offset voltage drift	0.75μV/°C
High common-mode rejection	90dB minimum
Low nonlinearity	0.01% maximum

GETTING TRANSDUCERS TO "TALK" TO DIGITAL COMPUTERS

Digital computers can't interpret transducer signals without help from data converters. Here's how these system components are interfaced.

Transducers and computers don't speak the same language. So a data converter must translate the analog signal from a transducer into a digital signal. To apply data conversion, you must look at not only the type of data converter and its specifications, but also the type of transducer, the converter support circuitry and the method of interfacing the converter to your computer.

TAKE A LOOK AT THE TRANSDUCER

Temperature, pressure, flow, level, position and other physical parameters must be translated before they can be handled digitally. The electrical signals produced can range from small to large voltages or currents.

Fortunately, the electrical signals produced by most transducers fall into three major categories: high level voltage, low level voltage and current. High level voltages generally range from zero to several volts, typically not more than 10. Low level voltages range from zero to a few tens of millivolts. Most current transducers use the following ranges: 0-20mA, 4-20mA or 10-50mA.

It's possible to design an analog interface to match all these levels in one system, but it's unnecessary - especially for microcomputers. Typically, a microcomputer system is responsible only for a few similar types of transducers. The microcomputer system may interface to a larger central computer that monitors a number of microcomputer loops, but the analog interface is needed only at the microcomputer level.

The types and number of tranducers interfacing to the microcomputer will dictate the analog interface needed. Take, for example, a microcomputer system that monitors and controls a combustion boiler (Figure 1). Inputs come from flame temperature sensors, effluent gas analyzers and fuel flowmeters. Computer outputs control fuel and oxygen, and also drive a small strip chart recorder to record the burner's operation.

The input transducer in this case produces low level voltage outputs. Before the signals can be processed, they must be converted by an analog-to-digital (A/D) converter. Since there is more than one input, multiple A/Ds must be used or all inputs must go through a multiplexer switch into one A/D converter. Presently, the least expensive and most accepted method is to multiplex several inputs into one A/D converter. Since converters require inputs of several volts, a differential instrumentation amplifier must amplify the low level signals.

Digital output signals from the computer are converted by a D/A (digital-to-analog) converter. The computer output then becomes a control signal. Electrically operated fuel and mixture valves are adjusted through voltage setpoint inputs. And high level voltage inputs drive the strip chart recorders as well.

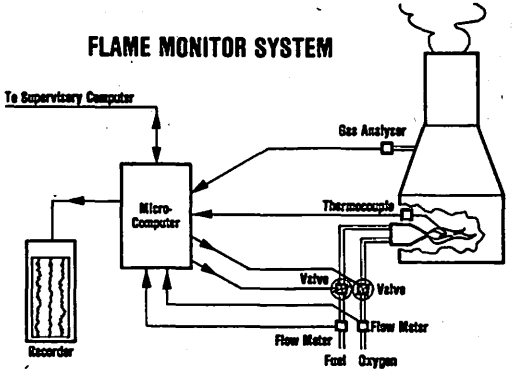
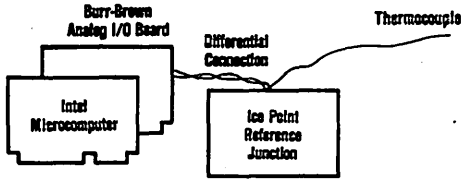


FIGURE 1. A microcomputer monitors and controls a combustion boiler. Inputs from flame temperature transducers, effluent gas analyzers and fuel flow meters are monitored by the microcomputer. Using the inputs to compute the control algorithm, it adjusts the valves controlling fuel and oxygen and also drives a small strip chart recorder.

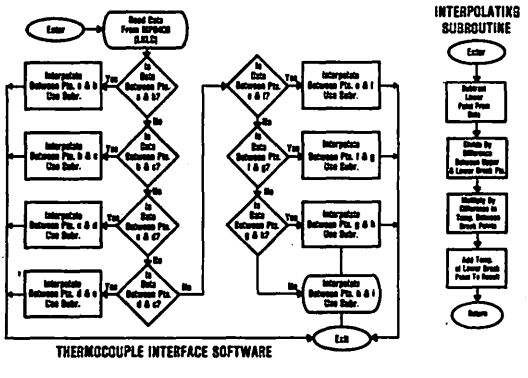
INTERFACING A THERMOCOUPLE TO A MICROCOMPUTER

Interfacing a thermocouple to a microcomputer is not just a matter of hardware; it also requires software. In this example, we interface a thermocouple using an ice point reference junction (32°F) to an Intel SBC80/10 single-board microcomputer. The interface is a Burr-Brown analog I/O system with 8 differential (or 16 single-ended) inputs. Because the thermocouple converts the temperature to a low level voltage, we use one differential input. The instrumentation amplifier on the I/O board is set for 1000. In this case, the Burr-Brown interface is the type that forces the processor to wait during conversion.



The system software consists of two parts: those instructions involved with the actual reading of data and those responsible for the data's linearization. Since we are using the processor halt method of interface, a single assembly language instruction (LHLD) is all that is required to specify the particular thermocouple channel, start the conversion and read the data when the conversion is complete.

The data can be linearized in a couple of ways: The basic problem is to determine the temperature that corresponds to a given voltage output from the thermocouple's nonlinear transfer function. This can be done by either evaluating a linearizing polynomial or by interpolating between points on a piecewise linear approximation. A piecewise linear approximation, in this case, is a table of the values of the thermocouple breakpoints stored in memory. The following flowchart reflects this method:



THERMOCOUPLE INTERFACE SOFTWARE

CONVERTER SHOULD MATCH THE TRANSDUCER

Once you know the transducer outputs, you can look at the interface components. To specify the appropriate component for your application, you must understand the basic characteristics of the components and what the specifications mean (see Figure 2).

First, let's look at the D/A converters, which are typically matched with high level voltage signals. With D/A converters, digital data is applied to a binary or BCD (binary coded decimal) weighted resistor network so that each resistor selectively draws current from a precision voltage source. The currents are summed to produce a total current flow proportional to the digital data. The current itself can be considered the converter's output and converted with several operational amplifiers to produce either a 4-20mA output or a voltage output.

The key specifications to look at for the D/A converter are: resolution, monotonicity, and linearity.

WHICH A/D CONVERTER?

Analog-to-digital conversion is commonly performed in one of two ways: successive approximation or integration. The successive approximation method is fast, accurate and inexpensive. But because the signal is converted at a given instant in time, a high noise environment can cause error.

Integrating converters are more accurate, less expensive, but much slower than successive approximation types. An integrating converter, however, is not affected by noise since the signal is built over a period of time.

As with the D/A converters, key specifications for A/D converters are: resolution, monotonicity, and linearity.

INFLUENCE OF SAMPLE AND HOLD

In many analog interface applications, a very fast time varying signal must be digitized. In fact, the rate of change of these signals may be so fast that it will exceed the basic inaccuracy of the converter. The sample and hold amplifier overcomes this problem by "freezing" the input signal at its output during the conversion process.

The amplifier's key specification is "dynamic nonlinearity." This is the total non-adjustable input to output error. It includes errors due to throughput nonlinearity, thermal transients and feedthrough. Typically, it's measured as a percentage error consisting of all errors that cannot be adjusted to zero for a 10 volt input change after a 10 microsecond acquisition time and a 1 millisecond hold time.

AMPLIFIER FOR LOW LEVEL SIGNALS

Low-level voltage (millivolt) signals must be amplified to several volts before they can be input to the sample and hold circuit or converter. The instrumentation amplifier does this, plus it rejects much of the noise that can enter the conversion system. This is because the amplifier does

not return the common of the system's transducer to ground, but connects as another input, minimizing the effects of the common-mode signal - which is usually a source of noise.

The primary specifications for an amplifer are: range of gain, gain nonlinearity, common-mode rejection (CMR), and settling time.

MULTIPLEXER FOR MULTIPLE INPUTS

Multiple analog inputs can be selectively connected to the A/D converter with a multiplexer constructed of relays or switches. Although electromechanical relays (reed) are common, they are slow and eventually wear out. Solid state switches overcome both of these problems. But they should not be used where high common-mode interchannel voltages must be handled. These voltages can either destroy the switch or cause a high amount of crosstalk that will interfere with the readings on other channels. Solid state switches are usually field effect transistors (FETS) and are grouped in integrated circuits that contain the associated addressing logic as well.

Key specifications for a multiplexer are:

● *Number of channels* - The number of inputs that the multiplexer can accept. They can be specified as either single-ended or differential. Single-ended inputs can be used for high level signals; differential inputs, consisting of two lines, should be used for low level signals.

● *Voltage range* - The maximum voltage above or below ground to which a channel can be raised.

● *Crosstalk* - The percentage of signal transferred from an off channel to the output of the multiplexer.

● *Settling time* - The time required for the output of a multiplexer to reach the value of the input within a given accuracy. This must be considered when a channel is first turned on or when a step change in the input occurs.

PUTTING IT ALL TOGETHER

For the control outputs, a digital-to-analog converter may be all that's required. But for the data acquisition portion of your system, you will need an A/D converter, amplifier and probably a sample and hold circuit and a multiplexer. Not only is this the area that requires more complete specifications (since it is the most accurate and speed-sensitive part of the system), but also the trickiest part of the system to interface to the computer.

When reading an analog input channel, the multiplexer addresses must first be set to the desired input channel. Enough time must be allowed for the multiplexer, instrumentation amplifier and sample and hold amplifiers to settle to their new readings. When the components have settled to the desired accuracy, the sample and hold amplifier is switched from sample to hold and the conversion begins. When the conversion is complete, the converter issues an end-of-conversion signal so that digital data can be removed and another channel processed.

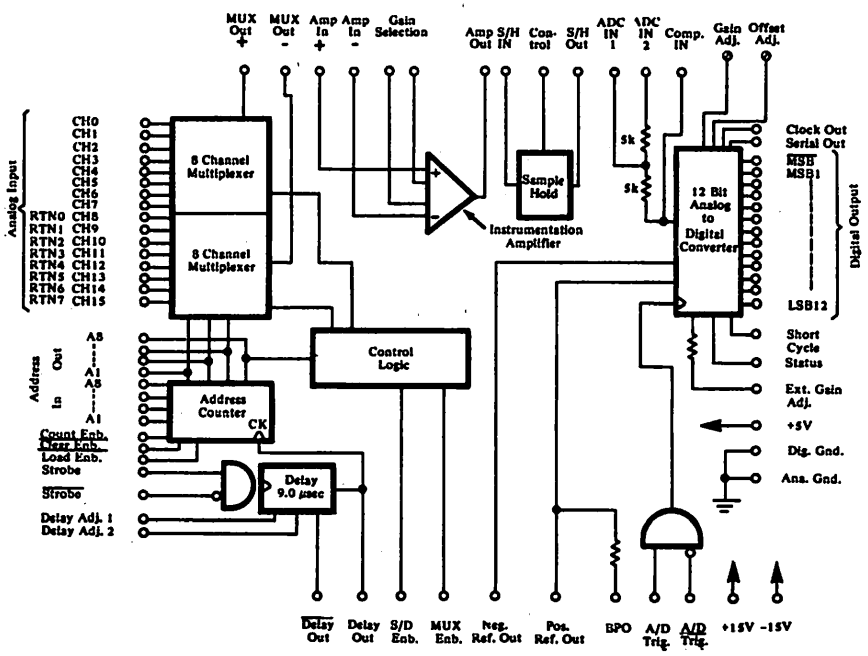


FIGURE 2. Converting the analog signal to a digital signal usually requires more than an A/D converter. Typically, analog signals are first multiplexed into an instrumentation amplifier that amplifiers the low level voltage signal into a high level voltage signal that can be converted. The sample and hold circuit then freezes the input for the conversion process, which is performed by the A/D converter.

All these operations are initiated by software although the wait period of settling time can be controlled by an external timing circuit. Because software is so important in the data conversion process, it's important to look at the way converters are connected to the computer. This can affect the software program significantly.

COMPUTER INTERFACE AFFECTS THE SOFTWARE

From a software standpoint, it is usually easier to treat each analog channel as a separate address. Computers can address a converter as either an I/O device or as part of memory. In the case of the I/O address, the converter is connected to the computer's I/O bus. The computer's I/O bus has a limited number of addresses, which a system of any complexity can quickly use up. If the converter is treated as memory, its address is mapped into a memory address field. Besides the ability to handle more input channels, memory mapped I/O provides more flexible programming since there are many more memory instructions than I/O type instructions with a microcomputer.

In addition to deciding how to address a converter, users must also consider how to handle the timing of the analog conversions. Using the simplest method, the program, after starting the process, continually checks or polls for an end-of-conversion signal to determine when the conversion is finished. This method, although simple, wastes processor time since the processor can't do anything else but poll for an end-of-conversion signal (Figure 3).

SOFTWARE FOR VARIOUS INTERFACE METHODS

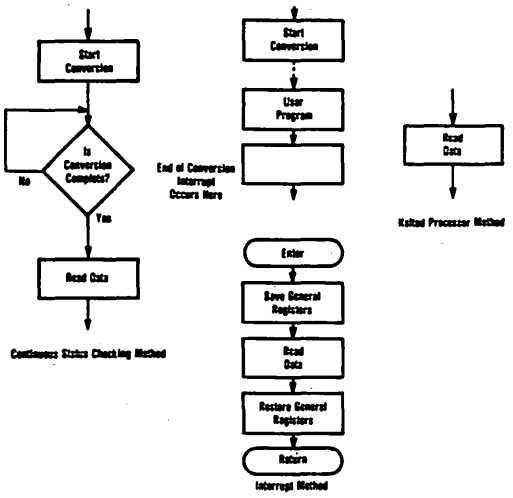


FIGURE 3. Software flowcharts for various A/D interfacing approaches. With the continuous status checking method, the processor continually polls for an end-of-conversion signal from the converter. In the interrupt method, the processor performs other computations until the end-of-conversion signal pulls the interrupt line of the processor. Another method simply halts the processor during the entire conversion process. The DMA method used for continuously scanning a block of channels is not shown here since the approach depends on the processor.

A better method relies on the processor's interrupt system to report the end of conversion. During the conversion time, other segments of the program can be executed until the end-of-conversion signal pulls the interrupt line. Although this approach may appear efficient, caution should be used when interfacing very fast A/D systems. The overhead time associated with servicing the interrupt may take the processor longer than the time required for the conversion. The net effect would be slower throughput than if the processor were to constantly poll for an end-of-conversion signal.

Another approach that overcomes the interrupt method's speed disadvantages is to connect the analog system so the processor is placed in a wait state during the conversion. With some processors, it's possible to halt the processor mid-cycle to wait for the conversion. In this way, the entire conversion process can be carried out during a single memory read instruction with the timing of the operation totally transparent to the programmer. Halting the processor during the conversion time provides the highest throughput speed for programmed data transfers. It also reduces noise generated by the digital system.

One drawback to this method is that the processor is oblivious to any other outside event during the conversion. If a processor must respond to external events faster than the given conversion time, then this method should not be used.

Still another method, if a block of channels must be continually scanned, is direct memory access (DMA). Although more complicated from a hardware standpoint, this maximizes channel throughput with a minimum of software.

DMA can take one of several forms, depending on the processor. In one mode of operation, a segment of memory can be continually updated by continuous automatic operation of the analog system and the digital data can be transferred between processor cycles. Only a slight reduction in software execution speed will result and the data can be fetched from memory without regard to the operating details of the analog interface. With another mode of operation, several channels are processed and then an interrupt is generated to signal the software that a block of data is available.

PLAN THE ANALOG INTERFACE

Like all other aspects of microcomputer systems, the analog interface requires attention and careful planning. A number of prepackaged, fully interfaced systems are available for both the board type microcomputer and the individual processor components. Although such systems reduce the amount of design time required in an analog application, their operation and limitations must still be understood to apply them to a particular system.

MAINTAINING ACCURACY IN HIGH-RESOLUTION A/D CONVERTERS

Design engineers have many techniques at their disposal that preserve the integrity of an analog signal in high-resolution A/D conversion and get optimum performance from precision data converters.

Although 14- and 16-bit A/D converters are providing the high resolution needed in many demanding applications, their circuits must be built with special care if the devices are to achieve maximum accuracy. Circuit problems that might cause only second- or third-order errors in 8-, 10-, and 12-bit converters can induce first-order errors in 14- and 16-bit devices.

The Burr-Brown model ADC76KG 16-bit A/D converter (see Figure 1) has a maximum specified nonlinearity error of ±0.003% (14-bit). In converters of this type, most layout problems result from poor grounding techniques.

A good rule of thumb is to separate the grounds for the converter's analog and digital circuits from the rest of the circuit and connect them to a low-impedance point near the power supply. The currents flowing into these grounds can change during the normal conversion process, and if there is a high impedance in the ground line, the changes in current can cause changes in voltage at the analog ground pin of the converter. Such changes can increase the nonlinearity errors of the converter and increase noise at critical transition points.

To avoid these problems, keep the ground traces from the converter to the power supply return as short as possible and make the ground pattern as wide as possible to further reduce the impedance. A solution to the noise problem is to use a ground plane, or shield, under the converter. However, if there are changing ground currents in the ground plane, the shield can behave like an antenna—increasing noise rather than decreasing it. The ground plane, therefore, should be connected only to the analog ground pin of the converter. If it is not possible to separate the A/D converter's grounds from the rest of the circuit, the grounds can be bound together and tied to a point close to the supply return.

BYPASSING IS IMPORTANT

Another important factor in maintaining converter accuracy is power-supply bypass (see Figure 2). Most converters are not affected by small, low frequency variations on the supply lines. However, as the frequency increases —when a switching power supply is used, for example— more noise couples into the critical reference circuitry inside the converter and induces errors. Even if well filtered power supplies are used, high frequency noise can still couple into these lines from such sources as system clocks and address switching.

Large tantalum capacitors (10μF to 100μF), paralleled with smaller ceramic capacitors, are effective in reducing

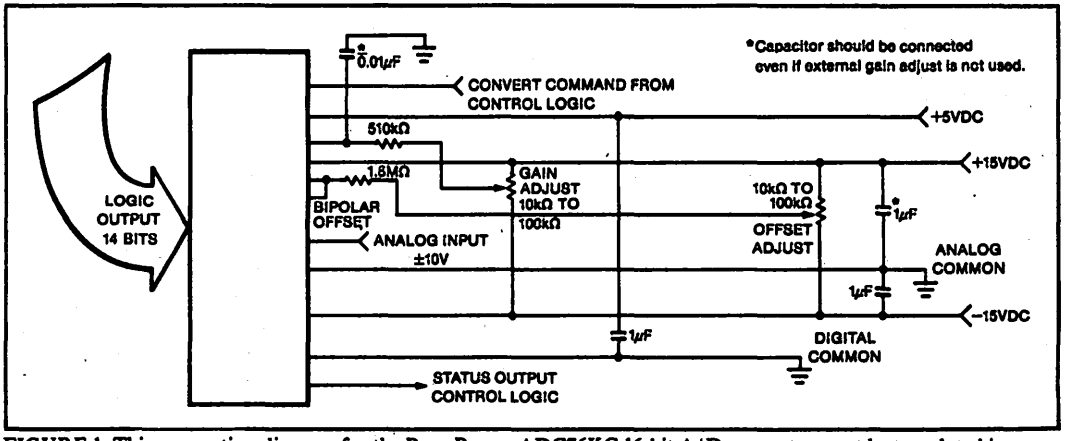


FIGURE 1. This connection diagram for the Burr-Brown ADC76KG 16-bit A/D converter must be translated into an optimum circuit board layout to ensure specified performance.

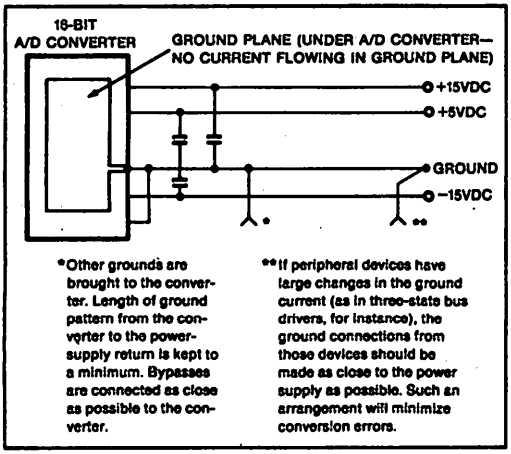


FIGURE 2. Good grounding, shielding, and bypassing techniques are essential when designing with high-resolution A/D converters.

such noise. These capacitors should be located as close to the converter as possible and tied to a solid ground—connecting the capacitors to a noisy ground defeats the purpose of the bypass.

Other sources of noise in an A/D converter are high impedance inputs. The most critical of these are the comparator inputs—particularly in a successive-approximation A/D converter. Much of such noise can be avoided by leaving the comparator reference input pin open and surrounding it with an analog ground plane or a low impedance power-supply plane. However, with the pin open, offset adjustment, which normally is done at the comparator input, must be done elsewhere in the circuit—possibly at the amplifier in front of the converter. If the offset adjustment must be made directly at the converter input, the series resistor and the potentiometer should be connected as close to the converter as possible to minimize noise pickup.

If the converter is used in the bipolar mode, the comparator input is connected to the bipolar offset pin. In a bipolar configuration, the bipolar offset pin is just as critical as the comparator input and should be equally well shielded.

The gain adjust pin is another input that represents a relatively high impedance to the outside world; it is, therefore, susceptible to noise. Any noise on this line will feed directly to the individual bit currents and compromise the accuracy of the transfer function.

As with the offset adjust, the gain adjust should not be done at the gain adjust input but at some other point in the circuit. The gain adjust pin should be surrounded by a ground plane, and on the ADC76, it is bypassed with a 0.01μF to 0.1μF capacitor even if the gain adjustment is done elsewhere in the system.

SEPARATE ANALOG AND DIGITAL LINES

The converter's analog-input lines can also be sources of errors. These lines should be separated and shielded from the digital I/O lines. The coupling of high frequency digital signals into the analog lines by mutual, or stray, capacitance can produce errors that are even more significant than those caused by poor grounding.

A fraction of a picofarad of stray capacitance, for instance, can cause 3V to 4V TTL signals with rise times of 20ns to 30ns to induce glitches of several LSBs in the analog-input line (5kΩ to 10kΩ impedance). A low impedance shield between the TTL signal and the analog input line should be used to ground the noise signals.

The input impedance of a typical successive-approximation A/D converter is relatively low (5kΩ to 10kΩ), so a buffer amplifier is often required to provide a very high impedance to the source signal and a very-low impedance to the converter. The characteristics often considered in the selection of this amplifier are the open-loop gain (to minimize non-linearity error in the closed-loop configuration) and DC specifications such as offset voltage and drift.

However, the AC characteristics of the amplifier must also be considered. The input current of the converter changes rapidly during the normal successive-approximation A/D process as each bit current is compared to the analog input current. Since the output impedance of the amplifier changes as a function of frequency, an error voltage induced by these sudden current changes at the converter input generates a corresponding error at the output of the amplifier (see Figure 3).

Note the large glitch that occurs when the most-significant-bit current of 1mA is compared to the analog-input current. The glitch becomes successively smaller as the current being compared is reduced by a factor of two.

One solution to this problem is to simply put a large capacitor at the analog input to the converter. The capacitor presents a low impedance to high frequency glitches. However, placing the capacitor at the analog input also reduces the bandwidth of the input signal.

Another alternative is to add a simple two-transistor buffer inside the feedback loop of the amplifier (see Figure 4). This reduces the output impedance at high frequencies yet preserves the maximum input signal bandwidth.

Even with proper grounding and shielding of analog-input lines, the adequate bypassing of power supplies, and a suitable buffer configuration, there still may be too much noise at the transition points from one digital-output code to the next. The A/D converter inherently generates its own internal noise.

The graph in Figure 5 shows a portion of the transfer function for a Burr-Brown model ADC71KG converter operated with 14-bit resolution. As the analog-input signal slowly increases, the converter operates continuously at a 50μs update rate. Note the uncertainty, or transition noise of about 0.2LSBs at a number of the transitions from one code to the next.

In Figure 6, the same portion of the transfer function is shown with the A/D conversion rate slowed down to 90μs. The noise is about the same as before because the bandwidth of the internal comparator and D/A converter has not been changed. And Figure 7 shows it with a 100pF capacitor on the comparator input and a 100μs conversion rate. The capacitor reduces the bandwidth of the comparator input.

Here, the transition noise or uncertainty is greatly reduced—but at the expense of conversion time. This is a good way to minimize uncertainty or maximize the repeatability of the A/D converter output if a slower conversion time will not compromise the system design.

Another method of minimizing transition uncertainty is to use digital-signal-processing techniques. Figure 8 illustrates a protion of the transfer function for an ADC76KG converter operating in the 14-bit mode. This device has a maximum conversion time of 15μs—which is about three-and-one-half times greater than that of the ADC71KG.

This increase in conversion speed results largely from the use of a comparator with a wider bandwidth—though such a comparator produces a transition noise of 0.3LSB to 0.4LSB, compared to 0.2LSB for the ADC71KG. The noise is random for the most part, so it can be reduced digitally by the simple averaging of two or more conversions. For every doubling of the number of conversion cycles, there will be a 3dB reduction in the random noise.

Figure 9a illustrates the effect of averaging five conversions to determine the digital-output code (total conversion time = 5 × 15μs = 75μs). Figure 9b shows the effect of averaging 10 conversions for a 150μs conversion time.

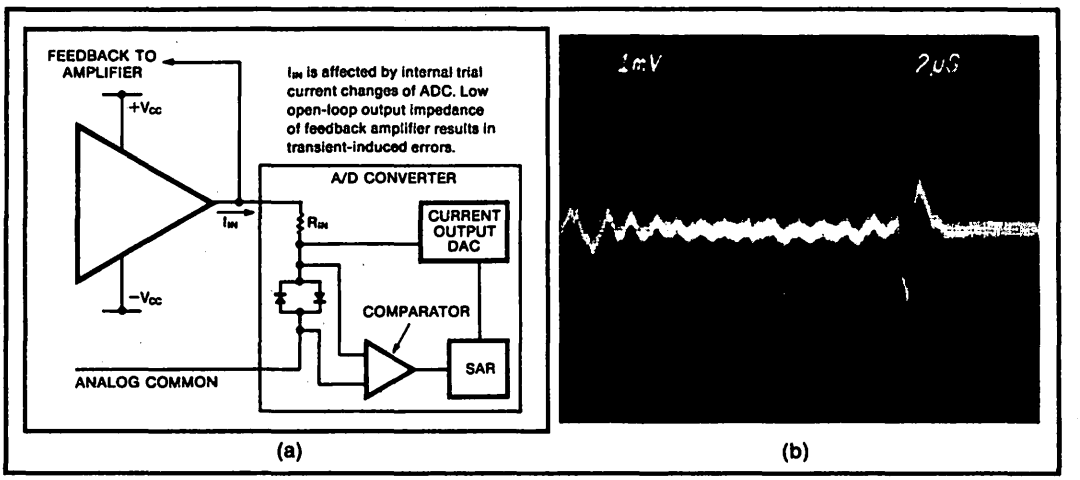


FIGURE 3. A successive approximation A/D converter can be driven with an external buffer amplifier (a). The glitches at the output of the buffer (b) are caused by input-current modulation that occurs in the converter during the conversion process.

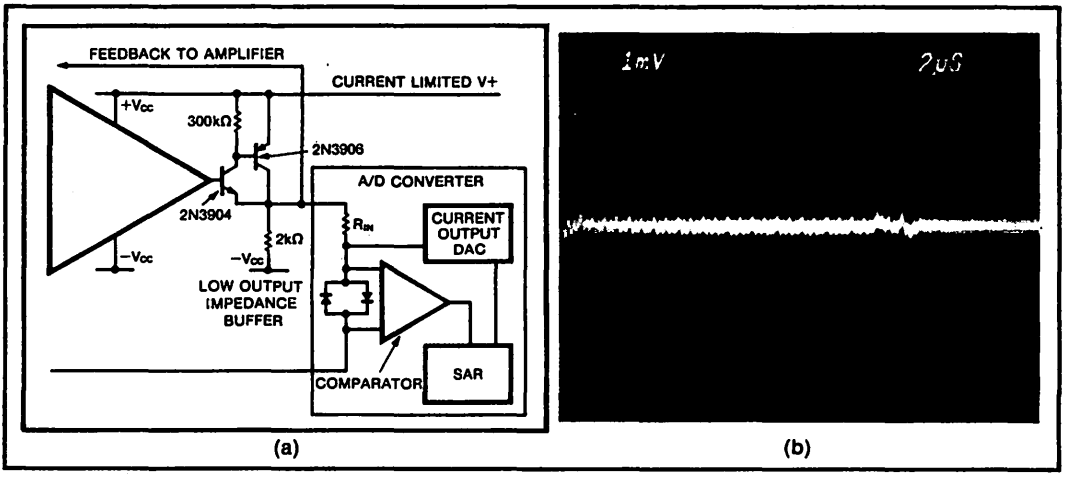


FIGURE 4. A simple two-transistor buffer-amplifier circuit (a) inside the feedback loop of the amplifier reduces the output impedance at high frequencies without disturbing the circuit's overall DC transfer characteristics. As a result, the output (b) is relatively clean and nearly free of spikes and glitches.

Using digital techniques to reduce the effects of random noise enables an efficient system design. The post-converter logic can be commanded to perform only as much averaging as is necessary. For example, in a multiple-channel system, high accuracy may be required on some channels, and high speed (with reduced accuracy) may be needed on others.

Furthermore, the effective resolution of the system can be increased by one bit for every factor-of-four increase in the number of conversions averaged. For example, four 14-bit conversions will result in 15-bit resolution, and sixteen 14-bit conversions will result in 16 bits.

This technique, known as over-sampling, is effective for increasing the resolution in A/D converter systems without sacrificing accuracy. It's most often used in digital-audio applications but can be easily adapted to many data acquisition tasks.

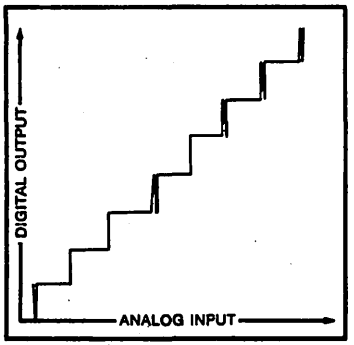


FIGURE 5. A portion of the transfer function for an ADC71KG converter with 14-bit resolution—operating at the specified maximum conversion time of 50μs—shows inherent noise at transition points.

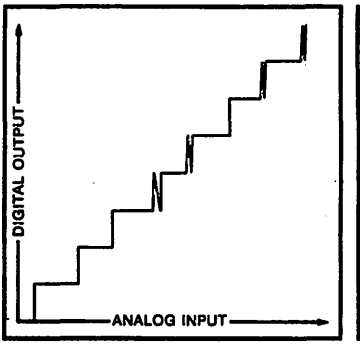


FIGURE 6. The ADC71KG with its conversion time slowed down to 90μs still displays some noise at transition points in the transfer function.

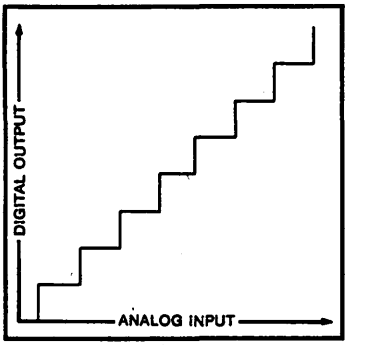


FIGURE 7. A 100pF capacitor, added between the comparator input and analog ground, reduces the bandwidth of the comparator and, hence, filters the signal at the critical decision point and eliminates the noise.

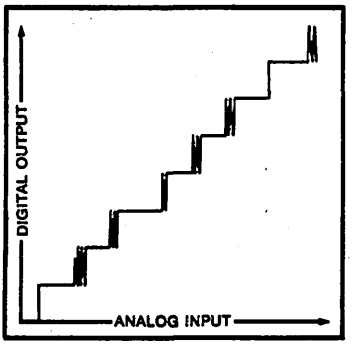
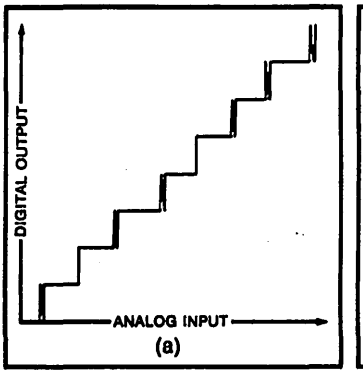


FIGURE 8. This portion of the transfer function for Burr-Brown's ADC76KG shows noise at the transition points because of the faster conversion speed—15μs—and associated wider bandwidth.



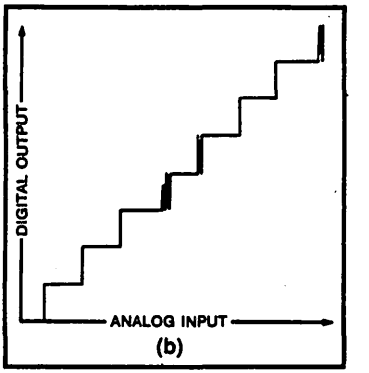


FIGURE 9. Averaging five consecutive conversions of the ADC76KG cleans up some the transition noise (a). The effect of averaging 10 conversion (b) is and even cleaner transfer function, but only at the expense of a longer effective conversion time (150μs).

PCM, A DAC FOR ALL SYSTEMS

BACKGROUND

Compact disc players were first introduced in 1982 and in 1982 Burr-Brown introduced its first monolithic 16-bit DAC manufactured specifically for CD applications. This was the PCM52, which was closely followed by PCM53 and, in mid-1985, PCM54 and its SOIC equivalent, PCM55. Due to a significant advantage in performance and a very competitive price, PCM54/55 became the market leader. Assembly was carried out in Japan which considerably enhanced our image. To maintain our position in the marketplace a new product, PCM56, is being introduced. This, in addition to ultra-low distortion and low noise, offers the facilities of serial input and high speed operation. Serial input greatly simplifies CD player construction and improves reliability. High speed operation allows the part to be used in over-sampling schemes which are gaining in popularity.

When the new part was first proposed to our major customers, the response was quite positive. One very large manufacturer undertook a redesign of its LSI circuit to take advantage of the proposed PCM product. This offered the prospect of a large sales order, but the product had to be ready for introduction in a very short time. We had to commit to a delivery of samples within six months. The challenge was accepted, our reputation was placed on the line, and an extremely intense design cycle was begun.

In the relatively short period from 1982, when the first CD players were introduced, competition has become very fierce. Manufacturers are looking for every advantage in cost and performance. Listeners are hearing high fidelity sound quality unattainable with analog techniques and the market is growing rapidly.

FUNDAMENTALS OF DIGITAL AUDIO REPRODUCTION

Linear PCM is employed for compact disc recording. This entails sampling of the audio signal at a rate of 44.1kHz and storing the amplitude as a 16-bit word. It has been shown that 16-bit resolution is equivalent to a 98dB signal-to-noise ratio. During reproduction the digital words representing the audio content are retrieved from the disc. The words are checked and errors corrected before being assembled into a serial data stream representing alternate left and right channel samples. In many systems the information is de-multiplexed into 16-bit parallel outputs corresponding to a particular left or right channel sample. The 16-bits representing the analog amplitude of the sample are fed simultaneously into a DAC. Here, the digital word is transformed back into an output voltage level. This circuit is thus at the heart of the reproduction process and is the key element in determining sound quality. All the care taken in the original recording and the ingenuity of error correction will be wasted if the DAC does not reconstruct a true representation of the original sound signal. The output of a DAC when changing from one output sample value to another takes a finite time to reach and settle to the new value. With many DACs this change is also accompanied by a large voltage spike known as a glitch. To remove these uncertainties, and possibly erroneous outputs associated with the DAC's change of state, an output sample and hold circuit, known also as a deglitcher, is employed. This is timed so that it only samples the DAC output when it has finally settled to the new value. During the time of the DAC output glitch, the deglitcher is operating in the hold mode and the disturbance is not coupled to the output. After de-glitching the audio signal, which now corresponds to a pulse-amplitude-modulated wave, is passed through a smoothing or reconstruction filter which removes all traces of the sampling frequency and its associated mixing and harmonic products, and provides at its output a faithful reproduction of the original audio waveform.

The function of the DAC is to reconstruct from the digital information an exact copy of the analog information used to record that particular sample. Thus, assuming that the recording process was accurate and that any corruption of the digital word during storage and retrieval has been corrected, the fidelity of the entire process is dependent on the performance of the DAC. Traditionally DAC specifications refer to gain error, offset error, integral and differential linearity. For industrial applications these specifications are adequate to describe the performance expected. For audio applications, some of the previously rigorous specifications—such as gain error and offset error—are no longer necessary. Gain error merely acts as a small change in sound volume, which is always under the control of the listener. Offset error merely gives rise to a DC offset voltage which is removed by capacitive coupling.

Although these specifications are not so important there are new specifications to consider. Total harmonic distortion is very closely related to the linearity of the DAC:

$$THD = \frac{e_{rms}}{E_{rms}} = \sqrt{\frac{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}{E_{rms}}} \times 100\%$$

E_{rms} = the rms signal level
n = the number of samples in one cycle
$E_L(i)$ = the linearity error at a particular sampling point
E_Q = the quantization error at that sampling point

but since the error at any particular digital code is due to a unique summation of bit errors, it does not give a complete picture. For this reason PCM DACs usually specify THD as measured with differing amplitude, digitally coded sine waves. This gives a much clearer indication of final performance.

At Burr-Brown our monolithic DACs are fabricated using highly stable thin film resistors and the final accuracy is adjusted by wafer level laser trimming, which is achieved economically. Experience with a large number of PCM parts over a number of years has taught us the

bit linearity pattern required to achieve a particular THD specification.

In addition to accuracy, for present CD applications, the part must require a minimum of external components, operate over a wide supply voltage and temperature range, consume minimal power and be economically priced.

The digital information stream, as extracted from the disc, combines alternate left and right channel samples. In many high end CD players, two separate DACs are employed, one for each channel, and the digital input is steered to the appropriate DAC.

This arrangement provides the maximum degree of channel separation but is not the most cost effective. Thus for lower-end users the DAC is more often multiplexed between channels. For this application the DAC must respond fast enough to give two clean outputs in one sampling period. The output of the DAC is then multiplexed using a deglitching circuit between the left and right channel filters.

As stated previously, many DACs give rise to a large voltage spike at the instant the DAC changes output levels. This is often due to elements in the circuit, namely the reference, fluctuating as the bit currents are switched. If this voltage spike is not fixed but varies with the digital code, as is usually true, the output of the filter will contain extraneous information. Being code-dependent, this will be correlated with the audio signal and hence give rise to distortion. To prevent this, it is usual to employ a sample-and-hold circuit, which may also function as the demultiplexer in the case when only one DAC is employed. In the case where separate right and left channel DACs are used, it is necessary to follow each with a separate deglitching circuit.

In any sampled data system it is necessary to band-limit the input signal in order to prevent aliasing. The sampled output waveform must be similarly filtered to remove those frequencies inserted by the sampling operation. Since the desired dynamic range of the system is greater than 90dB, these extraneous frequencies must be attenuated by at least this amount. To achieve this degree of attenuation in a single octave (22kHz → 44kHz) requires a multi-pole analog filter. Such a filter is expensive and difficult to build and invariably introduces some amplitude and phase distortion. To overcome this problem many CD player manufacturers are turning to digital filtering. Although this requires very complex digital circuitry, it can be economically realized in a LSI circuit.

The result of digital filtering is an increase in sampling frequency of two or four times. This effectively removes the frequency bands centered around the original sample frequency and harmonically related components up to the new oversampled frequency. Digital filtering is applied to the digital word and takes place prior to D-to-A conversion. After conversion and deglitching, only a modest amount of analog filtering is required to remove the remaining oversampling frequency components. For example, when four times oversampling is employed, a simple third-order low-pass filter is sufficient. In addition to reduced size and cost, the benefits of digital filtering include much reduced phase distortion and improved transient response. One disadvantage of the process is the increased speed requirement placed on the DAC, which must now operate at a much increased sample rate.

EVOLUTION OF SPECIFICATION

In order to meet the needs of present and future systems, the DAC must meet some very demanding specifications.

First linearity: the industry has grown accustomed to the extremely low levels of total harmonic distortion achieved by PCM54/55. This level of performance has to be retained and demands 14-bit accuracy and 15-bit monotonicity. The serial input function must be achieved with no deterioration of linearity or noise performance. To cover the case of four times oversampling, while simultaneously multiplexing between both left and right channels, requires clock speeds in excess of 8.5MHz and fast settling of the DAC and output amplifier. Coping with the shorter-time-constant deglitcher that may be required demands improved output drive current capability. All of the above features must be included for a minimal increase in power consumption and chip size.

The specification thus calls for high speed, low power, high density logic functions which must be implemented in a way that minimizes digital feedthrough and clock noise. The most suitable of the available processes has been developed for high performance analog functions requiring high breakdown voltage and not high density logic. This process is ideal for the high performance linearity specifications which are of prime importance in the manufacture of PCM parts, but dictates novel circuit design techniques to achieve the logic performance.

DESIGN SOLUTION

Examination of user requirements both present and future determines the circuit functions. A block diagram is shown in Figure 1. The input shift register is followed by a latch, which allows maximum flexibility of loading. Separate analog and digital supplies reduce the probability of digital feedthrough. Voltage reference and output amplifier are included to minimize the use of external components. In view of the very limited design time available for this project, previously designed circuit elements are employed wherever possible. In order to employ the well proven PCM DAC arrangement, the DAC current switches must be placed between ground and the negative supply rail. Since in this case the DAC is driven from latches, it makes sense to place the latch and shift register functions below ground, because level shifting is then only required between the three logic inputs and the shift register and latch circuits.

To design the required logic functions, heavy reliance was placed on SPICE simulations rather than laborious breadboarding with its limited performance distorted by unreal parasitics. To further minimize risk, total engi-

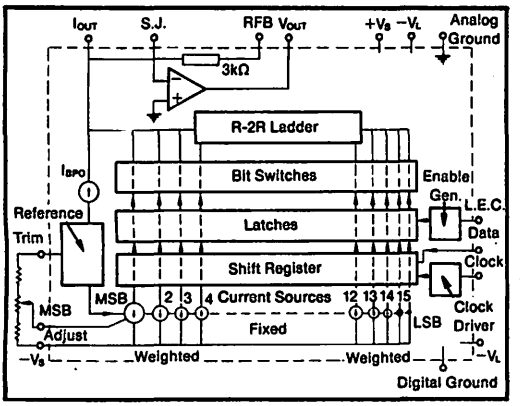


FIGURE 1.

neering resource was focused on the design during probing design reviews. With this combined experience, some areas of marginal performance were uncovered and corrected before committing the design to layout.

CIRCUIT DESCRIPTION

Voltage Regulator

An onboard voltage reference reduces the need for external components and enhances system performance by tracking the temperature changes of the DAC. It is the most critical element of a digital-to-analog converter, since the basic accuracy is directly dependent on it. A buried zener is at the heart of the reference and provides a highly stable low noise voltage source. The zener sets up its own bias, producing a constant current which doubly ensures a stable reference voltage. This type of feedback biasing demands the use of a "startup" circuit, which in this case is provided by means of an N-channel epi FET. When the zener turns on, the gate voltage rises—pinching the FET off and removing it from the circuit. The circuit is fully temperature compensated and corrects for both V_{BE} and Beta drifts.

Shift Register and Latch

The input shift register employs differential current mode logic (DCML) which gives an optimum solution to the high speed, low current, minimum area requirement. The shift register consists of a straightforward master/slave arrangement, but is more efficient than the typical ECL construction since the master/slave functions are coupled together. The resulting savings of two transistors is significant where 16 such stages are required. To prevent saturation of the emitter-coupled input transistors of the latch circuit, it is necessary to employ level shifting. To avoid the necessity for emitter followers between every shift register and latch stage, a separate bias line is generated to provide a shift-register-positive supply which is one diode drop below that of the latch.

Enable Pulse Generator

Since 16 latches are required, the edge-triggered master/slave approach is far too area-consuming. A single cross-coupled latch occupies minimum area but requires a sliver pulse to operate correctly. Since the LSI circuits on the market do not generate such a pulse, it is necessary to generate it on chip.

The enable pulse generator consists of a D-type flip-flop with a constant logic "1" at its input. It is clocked by the external latch-enable control signal and reset by the next occuring positive clock edge. The D-type flip-flop is constructed from the DCML master/slave structure used in the shift register. but this structure is simplified (since the D input is always high) by the omission of the master driver stages. The reset function is achieved by gating the clock pulse with the enable output. An output amplifier and driver stage is added to enable fast operation of the 16 latches tied to this output.

As has been stated, the generator is stacked below ground and referenced to the negative supply voltage. The input logic signals are generally TTL levels, between positive supply and ground, and need to be level-shifted to interface with the enable generator. To fulfill the specification, positive and negative supplies can take on a wide range of values; this makes voltage-level-shift schemes very difficult to implement. This problem may be overcome by converting the input logic signal to a current which can be returned to the negative supply rail. A differentially connected lateral PNP transistor pair is employed to perform this function and has subsequently been found to operate comfortably with clock frequencies in excess of 30MHz.

Clock Driver

The clock driver must supply the sixteen master/slave shift register stages. This represents a much heavier load than that applied to the enable output and as a consequence places much greater demands on the driver. Many simulations were performed before the final solution was found. The circuit employs the PNP level shift circuit described previously. However, in this case, the level-shifted currents are applied to an NPN current mirror stage, which employs emitter scaling to drive an inverting amplifier and emitter-follower bias current. This circuit acts in a push-pull mode at the clock rail outputs and any capacitance on the clock lines is thus driven by the total current available. Results have shown that this circuit is very efficient and allows extremely fast clocking with a modest 1mA of quiescent current.

Current Sources and Bit Switches

The arrangement of bit currents is such that the three most significant bits use binary weighted current sources, the next nine bits use equal current sources which are binary weighted through an R-2R ladder network, and the least significant bits use emitter division of a single current source. The current sources are defined by the reference voltage and stable thin-film NiCr resistors. These resistors are laser trimmed at the wafer level to achieve 16-bit performance. Each current source is switched either to ground or to the output by a differentially driven emitter-coupled switch. The emitter size of the switches is scaled to match the bit current so that base current losses track. Differential switching helps to

ensure that turn-on and turn-off times are equal, which considerably reduces glitch energy. In fact, differential circuitry is used for all clock and data signals throughout the shift register and latch stages. In this way digitial feedthrough is minimized.

Output Amplifier

The output amplifier is a typical operational amplifier structure using a phase splitter to drive an all-NPN output stage. It produces the 3V peak audio output level that is required. Slew rate, a respectable 12V/μs, is achieved with emitter degeneration of the lateral PNP input stage of 3kΩ. The amplifier possesses a typical 90dB open loop gain and a unity gain bandwidth in excess of 4MHz. Unlimited short circuit protection is achieved whenever an abnormally high voltage is developed across the low value emitter resistors associated with the output transistors. This in turn causes the drive to be removed from the output stage. The amplifier will drive 8mA load currents and allows an overall settling time of 1.5μs for an output voltage change of 6V. This well-proven design is essentially the same as that employed in the PCM54.

TESTING AND TRIMMING

Circuit design and layout are important steps in the production of a 16-bit part, but an equally important factor is testing and trimming. This is the stage of the process where the final performance is determined. To ensure economical manufacture and to avoid the creation of intolerable bottlenecks during high volume production, it is important to carry out this highly sensitive procedure in under 10s.

To achieve this end requires innovation in the test solution. With an LSB of 91.5μV, the need for additional gain at the probe level is mandated, but trim time negates any possible additional measurements for error correction. The solution, a precision current sink, removes 1mA from the output amplifier summing junction which causes the DUT to operate in a quasi unipolar mode (approximately 0 to 6V). This allows an additional gain stage onboard the probe card without the danger of lockup or the need for a pedestal DAC and the resulting overhead of additional software calibration. This gain is available on bits 1 and 3 through 16. Bit 2 is a special case as its weight in either mode is great enough to cause a lockup condition. For bit 2 the current sink removes 500μA from the summing junction.

Another problem concerns the fact that high energy laser pulses, used to trim the nichrome resistors, cause large and unpredictable photo currents to flow in the circuit. These currents are often sufficient to unlatch circuits and lose the bit information. Time does not allow for a synchronous trim technique and so during trim the DUT is continuously loaded at a conversion speed of 500kHz. and digital feedthrough which may introduce noise or circuit malfunction. For a 16-bit DAC any possible thermal effects due to self-heating are also of great concern, which demands that critical transistors such as the DAC current sources are placed on isothermal lines. Bringing all these considerations to bear while minimizing circuit area and completing the process in a short period is attributable to the experience and dedication of the layout personnel. A chip photograph is shown in Figure 2.

CAD LAYOUT

Since a large part of the circuit consists of shift register and latch stages, it is very important that this repetitive element be extremely space-efficient. From overall circuit topography this cell must be tall in the "Y" direction and narrow in the "X", which requires the various circuit elements, e.g., current sources and DCML gates, to be stacked on top of each other. This causes interconnection problems in a single-layer metal process. The solution is the use of diffused resistor cross-unders in the circuit areas that can tolerate them, such as the emitter-follower, load-current source connection. The cell is repeated but is carefully merged into other areas of the circuit at either end of the chain and at discontinuities such as those formed at the corners of the chip. While ensuring maximum packing density, it is also necessary to consider the effects of voltage drops along metal runs,

TIMING CONSIDERATIONS

CD player standards dictate a 44.1kHz/channel sampling frequency which gives 22.43μs between samples. Since both left and right channels must be sampled, the time between samples is 11.34μs. In a X4 oversampling system, the time is reduced to 2.835μs. Without a latch it would be necessary to clock in the data, settle and integrate within this time. With the latch it is possible to settle and integrate one sample while the next sample is being clocked into the register. The presence of the latch allows the user considerable versatility in clock timing. To enable sufficient time for the enable pulse generator to produce the sliver pulse, a delay circuit is employed in the data path. The connection of the delay circuit is such that the data may be advanced or delayed by almost one-half clock period from the clock. It is the 16 bits of data, prior to the latch enable control signal going low, which are switched into the latches. The data format is straight twos complement with the MSB first in.

An extremely fast settling active ground driver is provided to minimize errors caused by non-equal ground currents. Auto laser alignment, which minimizes trim time and maximizes yield, is available on each die via either destructive measurement of an on-chip bridge resistor, or preferably by utilizing an in-house reflective alignment process. Power supply consumption is tested first to eliminate gross failures. Functional test of all parameters are carried out, including individual bit tests, end point errors, and a test to determine the average LSB. Differential linearity is trimmed on the upper 12 bits if required, using software techniques designed to minimize system measurement errors. Each bit is tested after trim and a smart retrim is allowed under conditions relating to the amount of error and the trim position at the point of failure. At the conclusion of the trim process, bipolar zero and bipolar gain are trimmed and tested.

PERFORMANCE

The result of this effort is a precision 16-bit part which offers the convenience of fast serial loading and provides a fast settling voltage output with almost zero glitch energy. A shortened data sheet is shown in Table 1. The input shift register will typically clock at up to 30MHz and the output settles to within 0.006% in 1.5μs.

Pins 14 and 15 are brought out to facilitate external adjustment of bit 1. This feature allows the differential linearity error at bipolar zero to be adjusted to zero, and is an attractive feature for the high end user. By bringing out pin 15 from the internal reference, tracking of the adjustment current over temperature is ensured. The suggested arrangemnt is illustrated in Figure 1.

With this level of performance and convenience in a 16-pin DIP, operating at a mere 175mW from ±5V supplies, the part has already found wide acceptance among CD player manufactuers.

Serial input requires only three input connections between control circuit and DAC, which utilizes less space than the usual 16 inputs.

APPLICATIONS

The part is suitable for use in systems employing separate DACs for each channel and those with one DAC multiplexed between channels. It will operate at up to four times oversampling frequencies in either of the above modes, and the glitch energy is small enough that in many applications no deglitcher is required. Digital feedthrough is minimal and the combined analog and digital noise is typically less than $12\mu V_{rms}$ in a 20kHz bandwidth. Typical applications of the DAC detailing the interface to some existing LSI control circuits are shown in Figures 3 and 4. Figure 3 shows the connections between the SONY SDX 1130Q control circuit, PCM56, and the left and right channel integrate-and-hold circuits. The CXD 1130Q operates at a clock frequency of 4.23MHz and includes a ×2 oversampling digital filter. The single serial output contains data which is decoded by the DAC and multiplexed to the appropriate

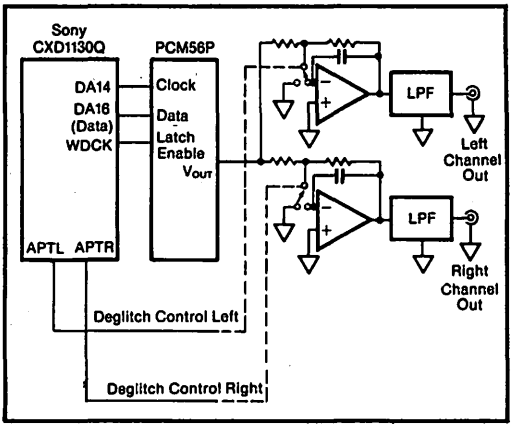


FIGURE 3.

channels by means of FET switches driven by signals from the LSI circuit APTR AND APTL.

Figure 4 illustrates another popular configuration which provides separate DACs for both left and right channels. In this example the NPC SM5804A digital filter is depicted with its separate left and right channel output operating at ×4 oversampling frequencies. In this example deglitching circuits are employed and the control signals are generated from the latch enable output, CO4. To avoid a possible race, condition delays are required and are provided by the inverters shown.

If deglitching circuitry is not required — many manufacturers operate in this mode — the dely circuit may be dispensed with.

In addition to digital audio applications, the performance of this part is of great interest to some industrial

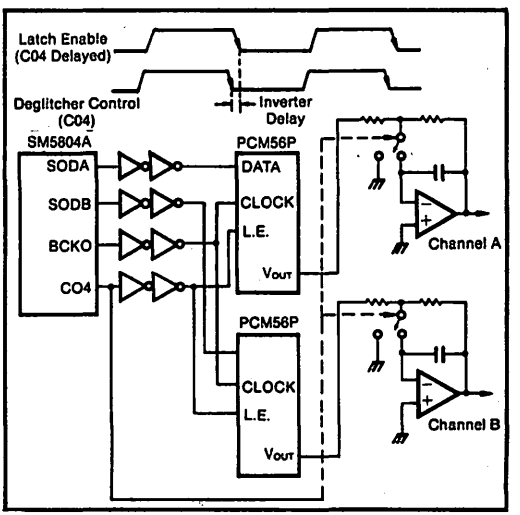


FIGURE 4.

users. Many users find they can live with the looser gain, offset, and drift parameters for the added convenience of serial input and the compact 16-pin DIP format. In addition, because the part is sold in such large quantities to the CD industry, the price is very attractive.

Characterization is being carried out to assess the feasibility of grading out parts with tighter gain, offset, and drift specifications. These parts will be slightly more expensive, reflecting the extra test time, but will be much closer to typical Burr-Brown industrial specifications.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and nominal power supply voltages of ±5V unless otherwise noted.

MODEL	PCM56P/-J/-K			
	MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Digital Inputs[1]: V_{IH}	+2.4		$+V_L$	V
V_{IL}	0		+0.8	V
I_{IH}, V_{IH} = +2.7V			+1.0	µA
I_{IL}, V_{IH} = +0.4V			−50	µA
Input Clock Frequency	10.0			MHz
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±2.0		%
Bipolar Zero Error		±30		mV
Differential Linearity Error		±0.001		% of FSR[2]
Noise (rms, 20Hz to 20kHz) at Bipolar Zero (V_{OUT} models)		6		µV
TOTAL HARMONIC DISTORTION				
V_O = ±FS at f = 991Hz: PCM56P-K		0.002	0.0025	%
PCM56P-J		0.002	0.004	%
PCM56P		0.002	0.008	%
V_O = −20dB at f = 991Hz: PCM56P-K		0.018	0.020	%
PCM56P-J		0.018	0.040	%
PCM56P		0.018	0.040	%
V_O = −60dB at f = 991Hz: PCM56P-K		1.8	2.0	%
PCM56P-J		1.8	4.0	%
PCM56P		1.8	4.0	%
MONOTONICITY		15		Bits
DRIFT (0°C to +70°C)				
Total Drift[3]		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.006% of FSR)				
Voltage Output: 6V Step		1.5		µs
1LSB		1.0		µs
Slew Rate		12		V/µs
Current Output, 1mA Step: 10Ω to 100Ω load		350		ns
1kΩ load[4]		350		ns
WARM-UP TIME	1			Min
OUTPUT				
Voltage Output Configuration: Bipolar Range		±3.0		V
Output Current	±8.0			mA
Output Impedance		0.10		Ω
Short Circuit Duration	Indefinite to Common			
Current Output Configuration:				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.2		kΩ
POWER SUPPLY REQUIREMENTS[5]				
Voltage: $+V_S$ and $+V_L$	+4.75	+5.00	+13.2	V
$-V_S$ and $-V_L$	−4.75	−5.00	−13.2	V
Supply Drain (No Load): +V ($+V_S$ and $+V_L$ = +5V)		+10.0	+17.0	mA
−V ($-V_S$ and $-V_L$ = −5V)		−25.0	−35.0	mA
+V ($+V_S$ and $+V_L$ = +12V)		+12.0		mA
−V ($-V_S$ and $-V_L$ = −12V)		−27.0		mA
Power Dissipation: V_S and V_L = ±5V		175	260	mW
V_S and V_L = ±12V		468		mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTES: (1) Logic input levels are TTL/CMOS-compatible. (2) FSR means full-scale range and is equivalent to 6V (±3V) for PCM56 in the V_{OUT} mode. (3) This is the combined drift error due to gain, offset, and linearity over temperature. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) All specifications assume $+V_S$ connected to $+V_L$ and $-V_S$ connected to $-V_L$. If supplies are connected separately, $-V_L$ must not be more negative than $-V_S$ supply voltage to assure proper operation. No similar restriction applies to the value of $+V_L$ with respect to $+V_S$.

PRINCIPLES OF DATA ACQUISITION AND CONVERSION

Data acquisition and conversion systems are used to acquire analog signals from one or more sources and convert these signals into digital form for analysis or transmission by end devices such as digital computers, recorders, or communications networks. The analog signal inputs to data acquisition systems are most often generated from sensors and transducers which convert real-world parameters such as pressure, temperature, stress or strain, flow, etc., into equivalent electrical signals. The electrically equivalent signals then are converted by the data acquisition system and are then utilized by the end devices in digital form. The ability of the electronic system to preserve signal accuracy and integrity is the main measure of the quality of the system.

The basic components required for the acquisition and conversion of analog signals into equivalent digital form are the following:

1 - Analog Multiplexer and Signal Conditioning
2 - Sample/Hold Amplifier
3 - Analog-to-Digital Converter
4 - Timing or Sequence Logic

Typically, today's data acquisition systems contain all the elements needed for data acquisition and conversion, except perhaps, for input filtering and signal conditioning prior to analog multiplexing. The analog signals are time multiplexed by the analog multiplier; the multiplexer output signal is then usually applied to a very-linear fast-settling differential amplifier and/or to a fast-settling low aperture sample/hold. The sample/hold is programmed to acquire and hold each multiplexed data sample which is converted into digital form by an A/D converter. The converted sample is then presented at the output of the A/D converter in parallel and serial digital form for further processing by the end devices.

SYSTEM SAMPLING RATE - Error Considerations

The application and ultimate use of the converted data determines the required sampling and conversion rate of the data acquisition and conversion system. System sampling rate is determined, as shown in Figure 1, by the highest bandwidth channel, the number of data channels and the number of samples per cycle.

Aliasing Error

From the Nyquist sampling theorem, a minimum of two samples per cycle of the data bandwidth is required in an ideal sampled data system to reproduce sampled data with no loss of information. Thus, the first consideration for determining system sampling rate is aliasing error, i.e., errors due to information being lost by not taking a sufficient number of samples per cycle of signal frequency.

Figure 2 illustrates aliasing error caused from an insufficient number of samples per cycle of data bandwidth.

How Many Samples per Cycle?

The answer to this question depends on the allowable average error tolerance, the method of reconstruction (if any),

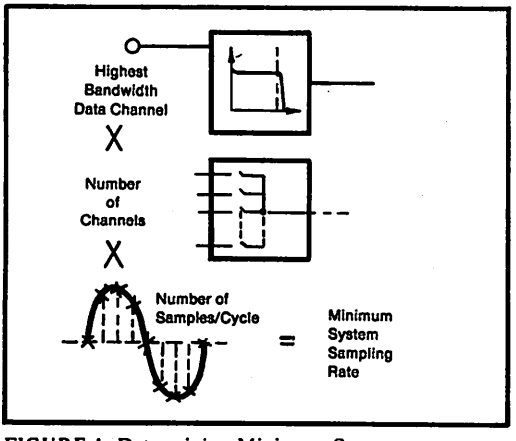


FIGURE 1. Determining Minimum System Sampling Rate.

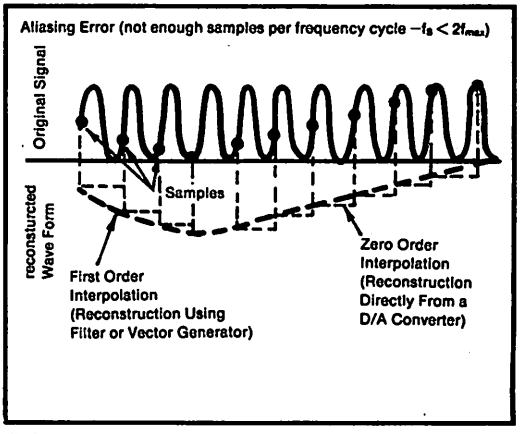


FIGURE 2. Aliasing Error vs Sampling Rate.

and the end use of the data. Regardless of the end use, the actual error of the discrete data samples will be equal to the throughput error of the data acquisition and conversion system plus any digital errors contributed by a digital computer or other digital end device.

For incremental devices such as stepping motors and switches, the average error of sampled digital data is not as important as it is for end devices that require continuous control signals. To illustrate average sampling error in sampled data systems, consider the case where the minimum of 2 samples per cycle of sinusoidal data are taken, and the data is recontructed directly from an unfiltered D/A converter (zero-order reconstruction). The average error between the reconstructed data and the original signal is one-half the difference in area for one-half cycle divided by π, or 32% for zero order data and 14% for first order reconstruction. However, the instantaneous accuracy at each sample point is equal to the accuracy of the acquisition and conversion system, and in many applications, this may be sufficient for driving band-limited end devices. The average accuracy of sampled data can be improved by (1) increasing the number of samples per cycle; (2) presample filtering prior to multiplexing, or (3) filtering the D/A converter output.

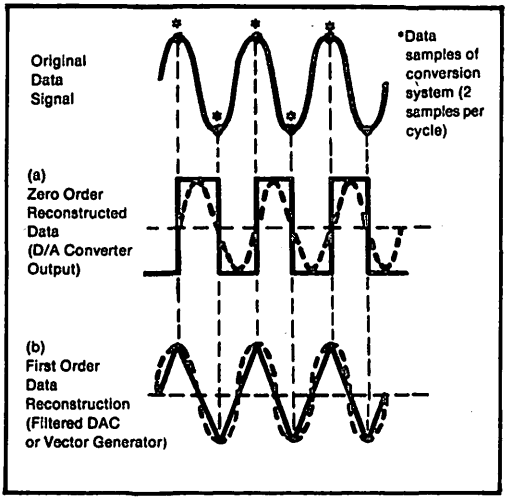


FIGURE 3. Reconstruction of Sampled Data Where $f_s = 2\,f_{max}$.

The improvement in average accuracy of sampled data is dramatic with only a slight increase in the number of samples per cycle as shown in Figure 4. The theoretical limit is the throughput accuracy of the acquisition and conversion system for continuous sampling.

For zero order reconstruction of data, it can be seen from Figure 4 that more than 10 samples per cycle of data bandwidth are required to reconstruct sampled data to average accuracies of 90% or better. A commonly used range is 7 to 10 samples per cycle.

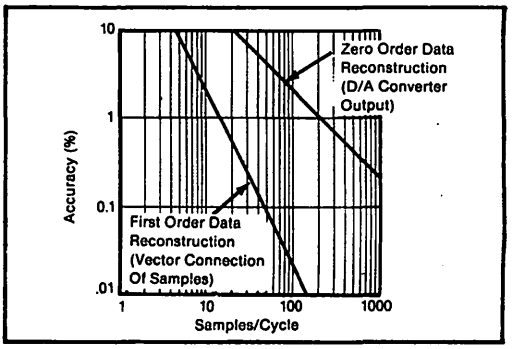


FIGURE 4. Reconstruction Accuracy vs. Number of Samples Per Cycle.

Aperture Error

Aperture error is defined as the amplitude and time errors of the sampled data points due to the uncertainty of the dynamic data changes during sampling. In data acquisition and conversion systems, aperture error can be reduced or made insignificant either by the use of a sample/hold or with a very fast A/D converter.

For sinusoidal data, maximum aperture error occurs at the zero crossing where the greatest $\frac{dv}{dt}$ occurs, and is expressed mathematically as:

$$\text{Aperture error} = d\left(\frac{A \sin 2\pi ft}{dt}\right) \times t_A \times 100\%$$

$$= 2\pi f t_A \times 100\% \text{ max}$$

where f = maximum data frequency

t_A = aperture time of system (this can be the conversion time of the A/D converter with no sample/hold or the aperture time of a sample/hold if one is used in front of an A/D converter).

This expression is shown graphically in Figure 5 for frequencies of 1Hz to 10kHz with ±1/2LSB error highlighted for 8-, 10- and 12-bit resolution A/D converters. The need for a sample/hold becomes readily apparent when data frequencies of 10Hz or higher are sampled, because the A/D converter conversion speed must be 2µsec or faster for aper-

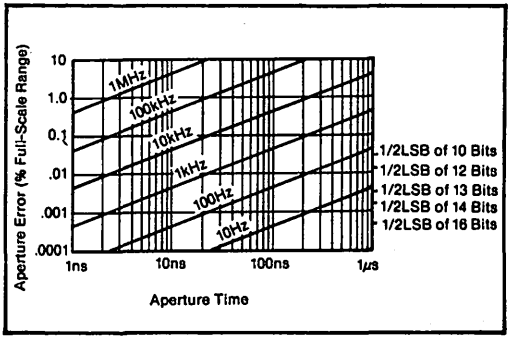


FIGURE 5. Aperture Error vs. Aperture Time for Data Frequencies from 10Hz to 1MHz.

ture errors less than ±1/2LSB for 12-bit resolution, and high speed A/D converters are complicated and expensive when compared to slower A/D converters with a low aperture sample/hold.

A sample/hold with an aperture time of 50nsec to 60nsec produces negligible aperture error for data frequencies up to 100Hz for 10- and 12-bit resolution A/D converters and is less than ±1/2LSB for 8-bit resolution for data frequencies near 5kHz. Use Figure 5 to determine your system aperture error for each data channel versus the desired resolution.

A FEW A/D CONVERTER POINTS

A brief discussion of A/D converter terminology will help the reader understand system resolution and accuracy a little better.

Accuracy

All analog values are presumed to exist at the input to the A/D converter. The A/D converter quantizes or encodes specific values of the analog input into equivalent digital codes as an output. These digital codes have an inherant uncertainty or quantization error of ±½LSB. That is, the quantized digital code represents an analog voltage that can be anywhere within ±½LSB from the mid-point between adjacent digital codes. An A/D converter can never be more accurate than the inherant ±½LSB quantizing error. Analog errors such as gain, offset, and linearity errors also affect A/D converter accuracy. Usually, gain and offset errors can be trimmed to zero, but linearity error is unadjustable because it is caused by the fixed-value ladder resistor network and network switch matching. Most quality A/D converters have less than ±½LSB linearity error. Another major error consideration is differential linearity error. The size of steps between adjacent transition points in an ideal A/D converter is one LSB. Differential linearity error is the difference between adjacent transition points in an actual A/D converter and an ideal one LSB step. This error must be less than one LSB in order to guarantee that there are no missing codes. An A/D converter with ±½LSB linearity error does not necessarily imply that there are no missing codes.

TABLE I. Relationship of A/D Converter LSB Values and Resolutions for Binary Codes.

A/D Converter Resolution (Binary Codes)		Value of 1LSB		Value of 1/2LSB	
Number of Bits (n)	Number of Increments (2^n)	0 to +10V Range (mV)	+10V Range (mV)	0 to +10V Range (mV)	+10V Range (mV)
16	65536	0.152	0.305	0.076	0.152
12	4096	2.44	4.88	1.22	2.44
11	2048	4.88	9.77	2.44	4.88
10	1024	9.77	19.5	4.88	9.77
9	512	19.5	39.1	9.77	19.5
8	256	39.1	78.2	19.5	39.1

Selecting the Resolution

The number of bits in the A/D converter determines the resolution of the system. System resolution is determined by the channel(s) having the widest dynamic range and/or the channel(s) that require measurement of the smallest data increment. For example, assume a channel that measures pressure has a dynamic range of 4000psi that must be measured to the nearest pound. This will require an A/D converter with a minimum resolution of 4000 digital codes. A 12-bit A/D converter will provide a resolution of 2^{12} or 4096 codes - adequate for this requirement. The actual resolution of this channel will be $\frac{4000}{4096}$ or 0.976 psi. The A/D converter can resolve this measurement to within ±0.488 psi (±½LSB).

Resolution

The number of bits in an A/D converter determines the resolution of the data acquisition system. A/D converter resolution is defined as:

$$\text{Resolution} = \text{One LSB} = \frac{V_{FSR}}{2^n}, \text{ for binary A/D converters}$$

$$= \frac{V_{FSR}}{10^D}, \text{ for decimal A/D converters}$$

LSB = Least Significant Bit

V_{FSR} = Full Scale Input Voltage Range

where n = number of bits

D = number of decimal digits

The number of bits defines the number of digital codes and is 2^n discrete digital codes for A/D converters.

For this discussion, we will use binary successive-approximation A/D converters. Table I shows resolutions and LSB values for typical A/D converters.

INCREASING SYSTEM THROUGHPUT RATE

The throughput rate of the system is determined by the settling times required in the analog multiplexer and input amplifier, sample/hold acquisition time and A/D converter settling and conversion time.

Two programming modes that are commonly used in data acquisition systems are normal serial programming (Fig. 6A) and overlap mode programming (Fig. 6b). The range of typical system throughput rates for these types of modes are shown in Table II for the Burr-Brown SDM857KG modular data acquisition systems.

A wide range of throughput speeds can be achieved by "short cycling" the A/D converter to lower resolutions and by overlap programming the data acquisition system.

The multiplexer and amplifier settling time is eliminated by selecting the next sample (channel n + 1) while the held sample (channel n) is being converted. This requires a sample/hold with very low feed-through error.

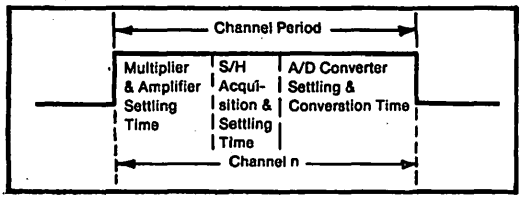


FIGURE 6a. System Throughput Rate - Serial Programming.

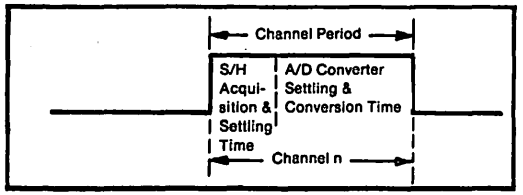


FIGURE 6b. System Throughput Rate - Overlap Mode.

TABLE II. System Throughput Rates and RSS Accuracy for Normal and Overlap Mode Programming for Burr-Brown Model SDM857KG Modular Data Acquisition System.

Resolution	Normal Programming		Overlap Mode	
	Max System throughput Rate	RSS Accuracy	Max System throughput Rate	RSS Accuracy
12 Bits	18kHz	0.025%	27kHz	0.025%
10 Bits	19.5kHz	0.08%	30kHz	0.08%
8 Bits	21.1kHz	0.30%	34.1kHz	0.30%

SYSTEM THROUGHPUT ACCURACY

The most common method used to describe data acquisition and conversion system accuracy is to compute the root-sum-squared (RSS) errors of the system components. The RSS error is a statistical value which is equivalent to the standard deviation (1σ), and represents the square root of the sum of the squares of the peak errors of each system component, including ADC quantization error:

$$\epsilon_{RSS} = \sqrt{\epsilon_{MUX}^2 + \epsilon_{AMP}^2 + \epsilon_{SH}^2 + \epsilon_{ADC}^2}$$

where ϵ_{MUX} = analog multiplexer error
ϵ_{AMP} = input amplifier error
ϵ_{SH} = sample/hold error
ϵ_{ADC} = A/D converter error

The source impedance, data bandwidth, A/D converter resolution and system throughput rate affect these error calculations. To simplify, errors can be calculated by assuming the following:

1. Aperture error is negligible - i.e., less than 1/10LSB.
2. Source impedance is less than 1000 ohms.
3. Signal range is ±10 volts.
4. Throughput rate is equal to or less than the maximum shown in Table III.

TABLE III. System Error Contribution and RSS Error vs. Resolution for Burr-Brown Model SDM857KG Modular Data Acquisition System.

Error Source	Resolutions		
	8 Bits	10 Bits	12 Bits
MUX Error	0.0025%	0.0025%	0.0025%
AMP Error	0.01%	0.01%	0.01%
S/H Error	0.01%	0.01%	0.01%
ADC Errors			
Analog	0.2%	0.05%	0.012%
Quantizing	0.2%	0.05%	0.012%
RSS Error	0.283%	0.072%	0.022%

DIGITAL CODES

One final consideration in data acquisition and conversion systems is the digital coding of the data at the output of the A/D converter. Data is usually encoded in either binary or binary-coded-decimal (BCD) form.

Binary encoded data formats are most commonly employed for digital computer-oriented applications where the processing is normally performed in binary notation. BCD data encoding is usually required in applications where the data is fed to decimal end devices such as digital readouts and printers. The majority of applications require binary encoding.

The most commonly used binary codes in A/D converters are:

1. Unipolar Straight Binary (USB) - used for unipolar analog signal ranges i.e., 0 to +5V, 0 to +10V, etc.
2. Bipolar Offset Binary (BOB) - used for bipolar analog signal ranges i.e., ±5V, ±10V, etc.
3. Bipolar Two's Complement (BTC) - used for bipolar analog signal ranges in many digital computer applications.

Two BCD codes, unipolar BCD and sign-magnitude BCD (SMD) are used in A/D converters. The definition of these codes is shown in Table IV and V.

TABLE IV. Definition of Binary Codes.

Definition	Output Digital Code	USB Code	BOB(2) Code
	MSB LSB		
+Full Scale	111....11 ϕ(1)	$+V_{FSR} - \frac{1}{2}LSB$	$\frac{+V_{FSR} - \frac{1}{2}LSB}{2}$
Mid Scale	100....00 ϕ	$+V_{FSR}/2$	Zero
-Full Scale	000....00 ϕ	$+\frac{1}{2}LSB$	$\frac{-V_{FSR} + \frac{1}{2}LSB}{2}$
One least Significant Bit		$\frac{V_{FSR}}{2^n}$	$\frac{\pm V_{FSR}}{2^n}$

NOTES: (1) ϕ is the transition value of the LSB. (2) BTC Code—invert the MSB (sign bit) of the digital code—ranges same as BOB codes.

TABLE V. Definition of Decimal Codes.

Definition	Output Digital Code (3 Digits)	Decimal Value	
		BCD Code	SMD Code
Sign	MSD(1) LSD		
+Full Scale	1 1001 1001 1001	999	+999
Zero	1 0000 0000 0000	000	+000
-Full Scale	0 1001 1001 1001	N/A	-999
One least Significant Bit		$\frac{V_{FSR}}{10^n}$ (2)	$\frac{\pm V_{FSR}}{10^n}$ (2)

NOTES: (1) MSD = most significant digit. (2) n represents number of digits—4 bits per digit.

SUMMARY

The criteria that determine the key parameters and performance requirements of a data acquisition and conversion system are:

1. Number of analog input channels.
2. Amplitude of data source signals.
3. Bandwidth of data.
4. Desired resolution of data.
5. End use of converted data.

Although this discussion did not treat all system criteria from a rigorous mathematical point of view, it does not identify and attempt to shed insight on the most important considerations from a practical viewpoint.

TO SIDESTEP SAMPLE/HOLD PITFALLS, RECOGNIZE SUBTLE DESIGN ERRORS

By knowing the key parameters and practices that govern important sample/hold functions, you can obtain optimum performance from these deceptively simple devices.

You can avoid the potential design traps that lurk in sample/hold applications by understanding and applying proven sampling rules and definitions. Widely used for voltage storage in analog-signal-processing and data conversion systems, sample/hold devices provide seemingly simple operation that often misleads designers.

In practice, functional intricacies hide error sources that can degrade sample/hold performance. Unfortunately, when manufacturers describe these errors, further complications can arise because most vendors use their own nonstandard terminology. (For some widely accepted definitions, see below.)

To help clarify a muddled situation, therefore, this application note presents some sample/hold design-verification guidelines. By carefully defining the basic sample/hold types - their primary specifications and their chief time- and frequency-response considerations - these guidelines arm you with the design information needed for proper sample/hold application (see Table I).

A GLOSSARY OF SAMPLE/HOLD TERMS

Acquisition time - Time after the sample-to-track command activates for the hold capacitor to charge to a full-scale voltage change and settle within a specified error band around the final voltage value.

Aperture delay - Elapsed time from activation of the sample-to-hold command to the opening of the switch in Hold mode.

Aperture time - Time for a switch to go from sample to Hold mode, measured from the 50% point of mode-control transition to when the output stops sampling the input.

Aperture uncertainty time - Variation in the time required for a switch to open after sample-to-hold transition occurs, or the time variation in aperture delay.

Bandwidth - For small signals, the frequency span between the points at which a sample/hold's gain goes down 3dB from its DC value (the frequency span between the points at which the output signal's amplitude equals 0.707 times the input signal). This parameter serves as a gauge of amplifier performance in Sample mode.

Charge injection - Offset error voltage on the hold capacitor when charge transfers from the capacitor to the gate-drive circuit via capacitive coupling at switch turn-off.

Droop rate - Hold capacitor's voltage-output decay or drift in Hold mode, arising from switch leakage current, hold-capacitor value and op amp bias current.

Feedthrough - Amount of input signal that appears at a sample/hold's otuput in Hold mode.

Gain accuracy - Expressed by the deviation in gain from its nominal value.

Monotonicity - In ADCs, describes an output that increases continuously with increasing input.

Quantizing error - Inherent uncertainty in digitizing an analog voltage to the nearest digital code word.

Sample/hold - Amplifier circuit that acquires analog input voltages during very short sampling times and stores them on a hold capacitor for a specified time.

Settling time - Time taken after a sample-to-hold transition for a sample/hold's output to assume final voltage value with a specified accuracy.

Spectrum response - Charcteristic that traces a sample/hold's amplitude - versus - frequency values.

Slew rate - Fastest rate, usually measured in volts per second, at which a sample/hold's output can change.

Zero-order hold - Filter that reconstructs an analog signal from a train of impulses by producing the first term of a power series approximation of the input.

TABLE I. Characteristics of Diode-Bridge and FET Sample/Hold.

DIODE BRIDGE TYPE	FET TYPE
Lower charge injection error.	Greater DC accuracy; has no offset and doesn't need feeback resistors.
Less generation of spikes; lower drive voltages are needed for bridge switching.	Faster in higher voltage applications; offers larger slewing current.
Shorter aperture delay; Diodes switch faster than FET's.	Smaller droop; Exhibits less inherent leakage.

FOR HIGH SPEED, USE DIODE-BRIDGE UNITS

High performance wideband and sample/holds come in two versions - junction FET and diode bridge types (see Figure 1). Diode bridge devices more readily accommodate applications that call for short RC time constants. Emphasing speed rather than accuracy, these applications generally involve 6-bit to 10-bit data acquisition systems with sampling rates of 1MHz to 50MHz.

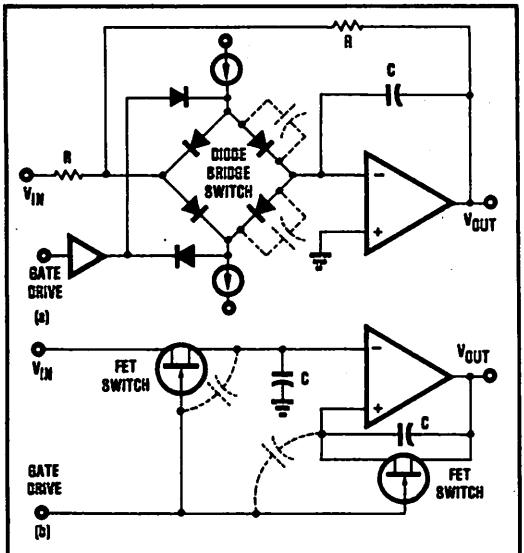
Because diode bridge devices require up to 5mA bias, their slew rate becomes the limiting factor in large capacitor and large input signal applications. When the hold capacitor exceeds 15pF, for example, the diode bridge's slew rate starts to decrease. (In such cases, consider the FET-type sample/hold.)

An important diode bridge application centers on deglitching a fast DAC (see Figure 2). Diode bridges' straightforward interfacing capability allows them to serve well here, and the relatively low voltage switching levels involved lead to very fast operation. In display applications, especially, DAC deglitchers must deliver low noise signals with minimal spiking at high update rates (3MHz to 20MHz). The deglitchers operate by placing the sample/hold in Hold mode before updating the DAC.

CALL ON FET DEVICES FOR BOTH SPEED AND ACCURACY

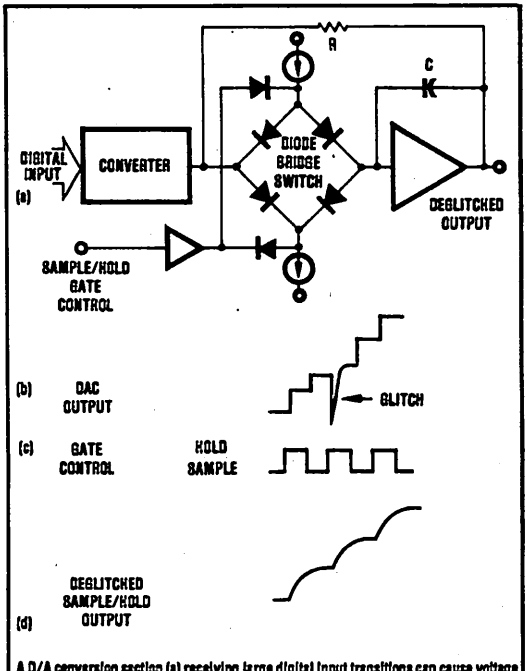
For more demanding applications, FET-type sample/holds yield superior performance in high speed, high accuracy, 10-bit to 13-bit data acquisition systems. Accuracy and speed result from the use of two FET switches, both of which help cancel the charge-injection error caused by the gate's drive waveform, permitting a low hold capacitor value. Additional FET-type sample/hold advantages include higher input impedance than diode bridge types and the elimination of offset, bias, and feedback resistors. And because FET sample/holds exhibit much lower leakage than diode bridge units - as well as a balanced configuration - the FET type's output buffer amplifier contributes virtually no leakage current.

In high voltage applications, where slewing time can cause long operational delays, high speed FET sample/holds have 25mA to 40mA available for slewing the hold capacitor, compared with 5mA for the diode bridge types. And although a diode bridge's lower charge-injection error eliminates the need for a large hold capacitor, this



In a basic sample/hold circuit, an analog switch closes and charges a capacitor to the input voltage (Sample mode). When the switch opens, the capacitor passes the stored voltage to the output amplifier (Hold mode). For fast small-signal switching at reasonable accuracy, consider a diode bridge type sample/hold (a). To obtain high accuracy as well as fast large-signal switching, use an FET-type sample/hold (b).

FIGURE 1. Diode-Bridge and Juntion-FET Sample/Hold Circuits.



A D/A conversion section (a) receiving large digital input transitions can cause voltage spikes, or glitches, in the analog output (b). Connected to the DAC's output as a deglitcher, a sample/hold removes these unwanted transients by taking a new analog data sample after the glitch has settled (c). Then the sample/hold returns to Hold mode before the DAC's output changes again, resulting in a relatively smooth monotonic transition between both samples (d).

FIGURE 2. Diode-Bridge Sample/Hold Used for Deglitching a Fast DAC.

advantage still doesn't overcome its lower slewing-current limitation.

Further, FET devices' single time constant - based on feedback resistance and hold capacitor - is much shorter than that of the diode-bridge types. When an FET unit's time constant equals or becomes less than the device's buffer-amplifier time constant, the sample/hold's settling time tends to depend upon the amplifier's settling characteristics. Generally, this relationship applies for a hold capacitor of about 10pF and a feedback resistor of about 300Ω. But when the time constant produced by these components becomes much larger than the amplifier's time constant, the sample/hold's settling characteristics do not depend on the amplifier. In this case, the FET-type sample/hold provides faster settling than a diode bridge device.

CLEARING UP SOME FOGGY SPECS

Many sample/hold problems emerge not from lack of knowledge about circuit design, but from difficult-to-understand nonstandard specifications. Complex parameter descriptions frequently result in designer confusion and misunderstanding. Further compounding the problem, parameter nomenclatures and definitions differ markedly among vendors. To help remedy this problem, some detailed explanations can help clarify the more important sample/hold characteristics.

Input impedance. In most applications, a sample/hold's input impedance depends directly on the operational mode. If this impedance level differs greatly from that of the signal source, you must insert a buffer amplifier between the devices. Otherwise, the impedance mismatch usually leads to a gain error. Obviously, the buffer amplifier's characteristics affect sample/hold operation and must be incorporated into the overall circuit design.

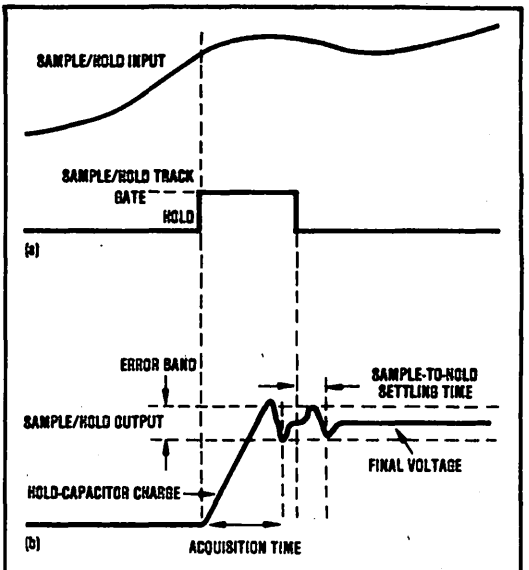
Settling time. This parameter must include both the acquisition time and the sample-to-hold settling time (see Figure 3). Specifying only one of these values does not fully describe it.

Aperture delay and aperture uncertainty. These quantities measure the acquired signal level when a sample/hold enters the Hold mode. Generally, the mode-control command is delayed as it passes through the sample/hold's switch driver. In synchronous applications, this aperture delay can cause time-interval sampling error. More serious errors occur when aperture delay varies excessively over a wide temperature range.

Aperture uncertainty specifies the sampling point's stability (see Figure 4). If time uncertainty exists when the sample/hold enters Hold mode or if time jitter occurs, this time-related "noise" transforms into signal-voltage noise as follows: signal noise equals aperture uncertainty times input-signal change at instant of sampling.

To pinpoint aperture uncertainty time (T_A), use the equation:

$$T_A = \frac{e_n}{de_s/dt}$$



Considered the most important specification for sample/holds, acquisition time begins at the hold-to-sample gate transition (a). It measures how long the hold capacitor takes to charge to a full-scale voltage change and remain within a specified error band (b). A correct definition of this parameter must include the settling time incurred after the sample-to-hold transition.

FIGURE 3. Sample/Hold Response Time.

where e_n = allowable signal noise and de_s/dt = signal rate of change.

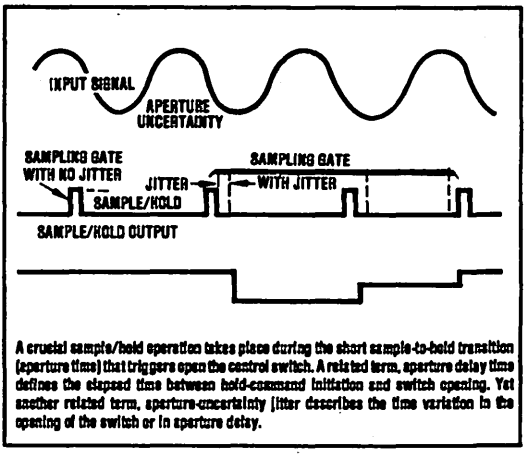
For example, assume that the allowable system nosie for an 8-bit, 10MHz ADC sampling system is 0.1LSB and that the input signal makes a full scale change (E_{FS}) at 5MHz (f). In this case,

$$e_s = E_{FS} / 2 \quad (\sin 2\pi ft.)$$

Thus,

$$T_A = \frac{e_n}{de_s/dt\ (max)} = \frac{e_n}{E_{FS}\pi f}$$

$$= \frac{0.1LSB}{(256LSB)(\pi \times 5 \times 10^6)} = 25psec.$$



A crucial sample/hold operation takes place during the short sample-to-hold transition (aperture time) that triggers open the control switch. A related term, aperture delay time defines the elapsed time between hold-command initiation and switch opening. Yet another related term, aperture-uncertainty jitter describes the time variation in the opening of the switch or in aperture delay.

FIGURE 4. Aperture Time Uncertainty.

Change-transfer or injection error. This error usually occurs when a sample/hold's gate drive couples onto the hold capacitor via charge-injection capacitance. The injected charge (Q) depends on the relationship.

$$Q = C_C V_G$$

where C_C = coupling capacitance and V_G = voltage arising from gate-drive capacitance. With respect to the output, the induced error becomes:

$$Q = V_I C_H$$

where V_I = voltage (error) arising from charge injection and C_H = hold capacitance. Eliminating Q from both equations yields:

$$V_I = \frac{C_C}{C_H} V_G$$

Furthermore, because the output responds to the *differential* charge transfer, the voltage-error equation changes to

$$V_I = \frac{\Delta C_D}{C_H} V_G$$

where C_D = the difference between the two capacitances in Figure 1.

Typically, this voltage behaves like a DC offset error - the output voltage differs from the input voltage by a constant value. In practice, diode bridge sample/holds can maintain a charge-transfer error of 0.005pC over a ±50°C span, whereas high-performance FET sample/holds achieve about 0.25pC over the same temperature range.

Sample/hold spiking. In many display applications, unwanted spikes appear on the CRT's involved. Vendors commonly dimension this error in volts x seconds (V x T), because the spikes' amplitudes depend on either the measurement circuit's or the sample/hold drive circuit's bandwidth.

If you model the spike as a narrow pulse fed into a sample RC circuit, the voltage output equals

$$e_o = \frac{VT}{RC} \epsilon^{-t/RC}$$

In effect, the low-pass RC circuit lowers the spikes' amplitudes but spreads out their duration.

In conjunction with a charge-injection error, sample/hold spiking can cause output signal noise. To overcome this problem, use a filter that effectively cancels positive spiking with negative spiking. Further improvement results when the output signal's bandwidth greatly exceeds that of the spike. Of the two sample/hold types, diode bridges yield the smallest spike.

Feedthrough. Usually stated as a percentage, this parameter indicates how much input signal appears at a sample/hold's output in Hold mode. Highly frequency-dependent, feedthrough affects processing accuracy because the output signal should stay constant during Hold mode.

Droop. Vendors usually specify the hold capacitor's voltage decay (droop) during Hold mode as a leakage current when referring to an external capacitor, and in volts per second when the sample/hold contains an integral capacitor. In analog-to-digital applications, the amound of tolerable droop depends on the ADC's conversion time and accuracy.

DATA-SYSTEM MODEL AIDS SPECTRAL ANALYSIS

Another major group of sample/hold design problems stem from noise effects. Unlike a linear process, such as amplification, the sample/hold sampling process generates output noise at frequencies that intermix with the input signal frequencies. Obviously, this noise interferes with the signal flow.

To gain insight into a sample/hold's spectral response, consider a representative data sampling system comprising (in series from input to output) a sample/hold device, an ADC, a digital processor, and a DAC. Theoretically, the sample/hold's output spectral response resembles that of the DAC. In practice, however, the DAC's output contains quantizing noise and, possibly, spiking noise. To simplify system operation without markedly affecting spectral response, assume that the ADC directly drives the DAC.

DUAL-SWITCH SAMPLE/HOLD SIMPLIFIES SAMPLING

As an aid in developing the data-sampling system's spectral properties, consider a sample/hold model employing two switches (see Figure 5). This model allows partitioning of the sampling process into multiplier and sample/hold portions, thus separating the former's noise analysis from the latter's bandwidth analysis.

Recall that when you multiply signal frequency f_1 by signal frequency f_2, new frequencies $f_1 + f_2$ and $f_1 - f_2$ result. On a spectrum analyzer, therefore, the multiplier's output appears as vertical lines corresponding to the new frequencies.

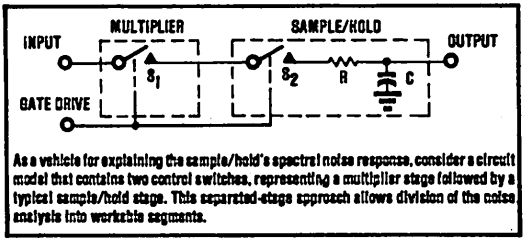


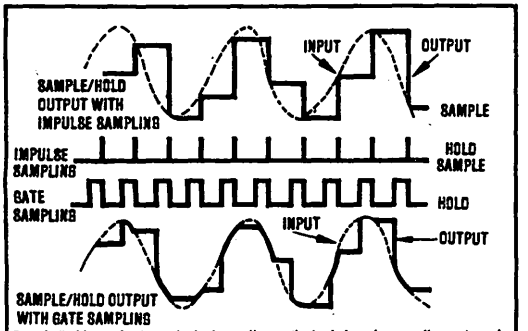
FIGURE 5. Simplified Model of Sample/Hold.

Furthermore, assume that the gate drive signal consists of impulses. This assumption focuses the discussion of the spectral components' amplitudes at the sample/hold's output. As Figure 6 shows, the frequency spectrum at the DAC's output is independent of the gate width; therefore, the foregoing impulse-input assumption is valid for this analysis. Note also in Figure 6 that so long as the sample/hold's output value remains the same for both impulse and gate-sampling methods, the ADC makes the same conversion, provided the gate stays closed long enough to acquire the signal. With impulse sampling, you can thus mathematically describe the gate drive's wave-

form by:

$$f(t) = \sum_{0}^{\infty} \sigma(t - nT)$$

where n = 0, 1, 2..., and where (t-nT) is an impulse that occurs when t = nT. T is the sampling interval.



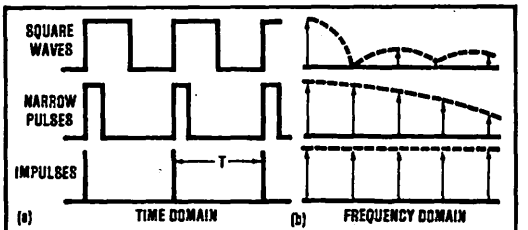
Sample/holds employ two principal sampling methods - in impulse sampling, extremely narrow gate pulses place the sample/hold in sample mode for very short time intervals and then quickly return the device to Hold mode. In gate sampling, relatively wide gate pulses keep the sample/hold in a Sample mode for longer time intervals before returning it to Hold mode. Note that the sample/hold's output value stays the same for both methods.

FIGURE 6. Sample/Hold Output as a Function of Gate Width.

USE IMPULSE RESPONSE FOR BANDWIDTH CHECK

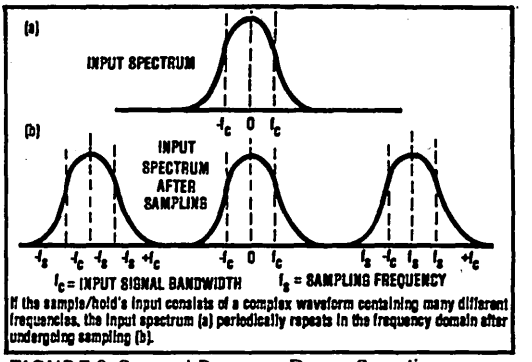
Remember that the spectrum of an impulse train in the time domain can be represented as a series of lines in the frequency domain separated by the sampling frequency (see Figure 7). Note that as the pulse widths get narrower, the spectral lines' amplitudes become uniform. Thus, impulse sampling becomes equivalent to multiplying an input frequency f_1 by nf_2, where n = 0, ±1, ±2, etc.

If you use a complex input waveform containing many frequencies, the input spectrum periodically repeats in the frequency domain (see Figure 8). Each spectral line of the sampling waveform, including the line at zero, shifts the input spectrum. This shifting also illustrates that if the highest frequency in the input spectrum equals half the sampling frequency, the sampled spectrum tends to merge. Such a condition makes it impossible to recover the original signal by filtering (the classic Nyquist sampling approach).



You can display the gate drive's pulse trains in either the time or the frequency domain. In the time domain (a), as the gate pulses get narrower, the sampling interval (T) expands. Accordingly, the spectrum extends in frequency. In the frequency domain (b), the Fourier-series representation of the corresponding time-domain waveforms demonstrates that with a frequency increase, the pulse amplitudes become uniform.

FIGURE 7. Time and Frequency Domain Descriptions of Gating Wave Forms.

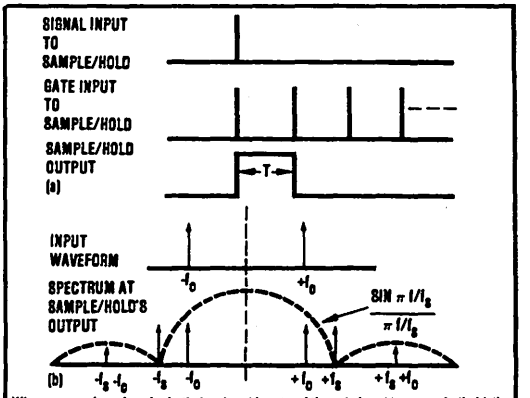


If the sample/hold's input consists of a complex waveform containing many different frequencies, the input spectrum (a) periodically repeats in the frequency domain after undergoing sampling (b).

FIGURE 8. Spectral Response Due to Sampling.

You can now compute the sample/hold's bandwidth by evaluating its impulse response. Figure 9 shows that a sample/hold's response to impulse inputs is a pulse whose width equals the sampling time. Taking the Fourier transform of the time-domain response thus yields the sample/hold's frequency characteristic:

$$\frac{F(f)}{F(0)} = \int_0^t f(t)\, \epsilon^{j2\pi ft}\, dt = \frac{f(T)\, \epsilon^{j2\pi ft} - 1}{j2\pi fT}$$



When you use impulses for both the signal input and the gate input to a sample/hold, the sample/hold generates a pulse output of width T (sample time) in the time domain (a). Taking Fourier transforms of this impulse response produces the sample/hold's frequency response (b).

FIGURE 9. Impulse and Spectral Response to Sample/Hold.

After some manipulation, this expression equals:

$$\frac{F(f)}{F(0)} = \epsilon^{j\pi f/f_S}\, \frac{\sin \pi f/f_S}{\pi f/f_S}$$

A sampled signal becomes harmonically distributed over the frequency domain, modified by this equation's sine term, where f is the input frequency and $1/f_S$ is the sampling period. With an applied input sine wave, the sample/hold's bandwidth drops 3dB down at $f/f_S = 0.443$.

SUPERPOSITION: THE HIDDEN DAC LINEARITY ERROR

As More DACs Become Available With Resolutions of 12 Bits and Greater, Users Should Know the Causes and Effects of Superposition Error on Relative and Absolute Accuracy and What to Do to Minimize It.

A digital-to-analog converter (DAC) translates digital signals to analog signals. For example, a 12-bit DAC takes a 12-bit binary number, called an input code, and converts it into one of 4,096 analog output voltages or currents. When the contribution to the output voltage or current of each individual bit is independent of any other, it means that the device exhibits no superposition error or that "superposition holds." For a DAC with little or no superposition error, the linearity error for any given code will relate to the linearity error at some different code. This allows you to determine the worst case linearity error, and the digital code where that error occurs, with a very simple test.[1]

However, if the DAC under test has excessive superposition error, this simple test will give erroneous results; therefore, you must test all digital codes to determine the worst case error and code. Superposition error, or bit interaction, often is significant in converters with a resolution of 12 to 16 bits. If the error becomes large enough, a DAC may fail to meet a 1/2LSB linearity error or relative accuracy specification even with each individual bit adjusted perfectly. This specification becomes important in many applications such as automatic test equipment or precision voltage standards where the absolute value of the output voltage must remain within specified limits after calibration of offset and gain errors.

For a DAC with low superposition, the following equation determines the output voltage, if we assume that the offset and gain errors have been removed:

$$V_o = V_{FS}[b_1(1/2 + \epsilon_1) + b_2(1/4 + \epsilon_2) + \ldots + b_n(1/2n + \epsilon_n)], \quad (1)$$

where $\epsilon_i \times V_{FS}$ equals the linearity error associated with the ith bit and b_i equals the value (0 or 1) of the ith bit of the DAC input code. Since the analog output error with all input code bits off (000...000) and all input bits on (111...111) has been adjusted to zero, then the summation of all the bit errors,

$$(\epsilon_1 + \epsilon_2 + \epsilon_3 \ldots \epsilon_n) \text{ or } \left(\sum_{i=i}^{n} \epsilon_i\right), \quad (2)$$

becomes zero. This means that the errors are symmetrical or, in other words, for every possible input code there exists an equal and opposite error associated with the one's complement of that code. The linearity error (sometimes called relative accuracy, integral linearity, nonlinearity or end-point linearity) is defined as the maximum error magnitude that occurs.

Now consider the relationship between the individual bit errors (ϵ_i) and the linearity error. There exists some digital input code ($b_1, b_2 \ldots b_n$) that yields the maximum linearity error (E_{max}) and the one's complement of this code ($\bar{b}_1, \bar{b}_2 \ldots \bar{b}_n$), that must yield an error of the same magnitude but in the opposite direction ($-E_{max}$). The relative magnitude and polarities of the errors determine which actual input code has the most linearity error. For the error to be maximum, all of the error terms must be additive and the following proves true:

$$|E_{max}| + |-E_{max}| = |b_1\epsilon_1 + b_2\epsilon_2 + \ldots + b_n\epsilon_n| + |\bar{b}_1\epsilon_1 + \bar{b}_2\epsilon_2 + \ldots + \bar{b}_n\epsilon_n|$$

$$2|E_{max}| = (b_1 + \bar{b}_1)|\epsilon_1| + (b_2 + \bar{b}_2)|\epsilon_2| + \ldots + (b_n + \bar{b}_n)|\epsilon_n|; \quad (3)$$

but $b_i + \bar{b}_i = 1$, making the maximum linearity error:

$$|E_{max}| = 1/2[|\epsilon_1| + |\epsilon_2| + \ldots + |\epsilon_n|]. \quad (4)$$

This result proves interesting because it relates the maximum linearity error to the individual bit errors; therefore, you can evaluate a DAC by simply measuring the output error associated with n digital input codes instead of all of the 2^n possible combinations.[2,3]

Stated another way, the sum of the positive bit errors should equal in magnitude the sum of the negative bit errors when the gain and offset errors have been removed. Any difference in these magnitudes indicates the presence of a superposition error. If this difference proves greater than approximately 1/10 of an LSB (JDEC standard for superposition error), further testing may become necessary to determine the accuracy of the DAC. However, a superposition error of more than 1/10LSB does not by itself imply that a DAC cannot meet a linearity specification of, say, ±1/2LSB; it simply means that you must conduct a more elaborate test to determine the worst case linearity error and digital input code where that error occurs.

A 3-BIT DAC

An example illustrating the relationship between linearity error and the individual bit errors for a 3-bit DAC appears in Figure 1a. Any deviation in the DAC output from the straight line drawn between all bits off and all bits on indicates a linearity error. With the superposition error less than 1/10LSB, the error pattern will appear as symmetrical around midscale as indicated.

Figure 1b shows a transfer characteristic for a 3-bit DAC which exhibits superposition error. Note that, in this example, the symmetrical error pattern around midscale no longer exists. You must consider the difference between the electrical sum and the algebraic sum of the bit errors when determining whether to use a more comprehensive test.

The data in Table I came from a 12-bit hybrid DAC. Note that, for this test, the full scale voltage was increased to 10.2375V, making the ideal bit weights, starting at the LSB, equal to 2.5mV, 5.0mV, 10.0mV... 2.560V and finally 5.12V for the MSB. You can memorize these numbers easily and calculate the error voltages quickly by inspection. The difference between the algebraic sum of the positive bit errors (320μV) and negative bit errors (−310μV) equals only 10μV, which indicates a low superposition error. Thus, the maximum linearity error becomes $1/2 \times (320 + 310) = 315\mu V$.

The data in Table II came from a monolithic bipolar 12-bit DAC. Note that the difference here between the positive bit errors (+550μV) and the negative bit errors (−1,650μV) equals −1.1mV or almost 1/2LSB. In this situation, superposition does not hold and you cannot say anything definite about linearity with the data available.

TESTING ALL INPUT CODES

When the short-cut method of measuring linearity error does not prove sufficient, you can develop a high speed measurement circuit capable of testing all 2^n code combinations. A simple schematic of this type of tester appears in Figure 2. The binary counter has n + 1 stages to provide a binary count from 0 to $2^n - 1$ and to reset the counters at the end of the count. The reference DAC and the × 10 error amplifier must have combined settling times to ±1/10LSB of less than 10μsec since the system clock must operate at 20kHz to have a flicker-free display. For a 12-bit converter, a complete cycle takes 50μsec × 4,096 counts or approximately 100msec. The output of the nth counter stage also displays on the scope to indicate the midscale transition point, and offset and gain adjustment potentiometers are provided to zero the end points of the error display.

This tester works well for 8-, 9-, and 10-bit converters. For a 12-bit DAC, the 4,096 segments displayed on the

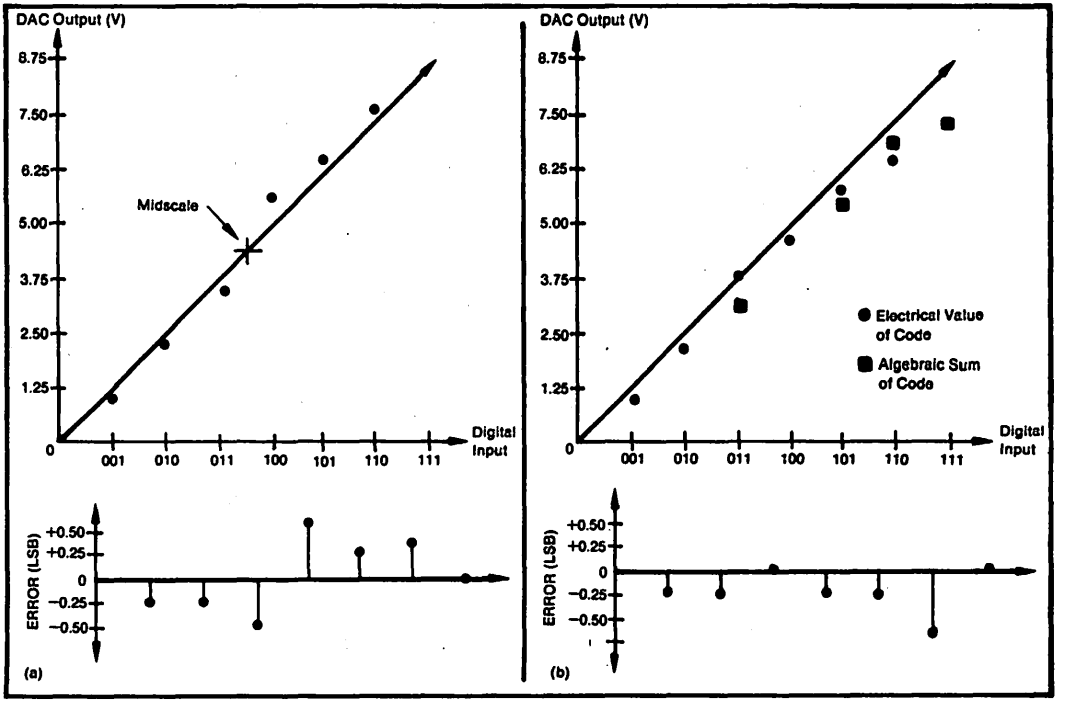


FIGURE 1. Both of these 3-bit DAC transfer functions exhibit errors. Linearity error (a) exists for input codes 001, 010, 101 and 110; note the symmetry of the errors about midscale. Superposition errors (b) lack symmetry about midscale.

TABLE I. In this data from a 12-bit hybrid DAC, the full-scale voltage was increased to 10.2375V, making the ideal bit weights, starting at the LSB, equal to 2.5mV, 5.0mV, 10.0mV...2.560V and finally 5.12V for the MSB. You can easily memorize these numbers and quickly calculate the error voltages by inspection.

Input Code	Ideal Output (V)	Actual Output (V)	Error (μV)
All Bits "On"	+10.23750	+10.23750	0
All Bits "Off"	0	0	0
Bit 1 (MSB)	5.12000	5.11995	− 50
Bit 2	2.56000	2.55982	−180
Bit 3	1.28000	1.27994	− 60
Bit 4	0.64000	0.63998	− 20
Bit 5	0.32000	0.32004	+ 40
Bit 6	0.16000	0.16004	+ 40
Bit 7	0.08000	0.08004	+ 40
Bit 8	0.04000	0.04005	+ 50
Bit 9	0.02000	0.02010	+100
Bit 10	0.01000	0.01002	+ 20
Bit 11	0.00500	0.00502	+ 20
Bit 12 (LSB)	0.00250	0.00251	+ 10
Positive Sum			+320
Negative Sum			−310
Difference			+ 10

CRT are spaced so close together that the switching transients create a wide band of noise making it difficult to tell if the converter meets its specification, especially with a linearity error near the ±1/2LSB limit. One way around this problem, if you assume that the errors contributed by the last four bits of the DAC are small,

TABLE II. Note that the difference between the positive bit errors (+550μV) and the negative bit errors (−1,650μV) in this data from a monolithic bipolar DAC, equals −1.1mV or almost 1/2LSB. In this situation, superposition does not hold and you cannot say anything definite about linearity with the amount of data available.

Input Code	Ideal Output (V)	Actual Output (V)	Error (μV)
All Bits "On"	+10.23750	+10.23750	0
All Bits "Off"	0	0	0
Bit 1 (MSB)	5.12000	5.11927	− 730
Bit 2	2.56000	2.55928	− 720
Bit 3	1.28000	1.27996	− 40
Bit 4	0.64000	0.64013	+ 130
Bit 5	0.32000	0.32013	+ 130
Bit 6	0.16000	0.16003	+ 30
Bit 7	0.08000	0.07887	− 130
Bit 8	0.04000	0.03997	− 30
Bit 9	0.02000	0.02000	+ 0
Bit 10	0.01000	0.01008	+ 80
Bit 11	0.00500	0.00512	+ 120
Bit 12 (LSB)	0.00250	0.00256	+ 60
Positive Sum			+ 550
Negative Sum			−1650
Difference			−1100

entails inhibiting these bits with the AND gates shown in Figure 2; this reduces the binary count to 256 and also gives each count 16 times longer for the glitches to settle out. You can make other improvements to this tester such as automatic offset and gain error nulling, a sample/hold deglitcher to remove the glitches at the error output and a go/no go window comparator to test the linearity error at each binary count.

Using the test circuit shown in Figure 2 and three different 12-bit DACs produced the oscilloscope photographs in Figure 3. The offset and gain errors have been nulled at the left and right portions of the photographs respectively; and the linearity error appears as the deviation from the horizontal center line of the scope, with the vertical sensitivity 1/2LSB per division. The digital input to the MSB indicates the midrange and full-scale binary counts.

The DAC errors displayed in Figure 3a appear symmetrically about the center of the scope, indicating very little superposition error; while those in Figure 3b are almost all positive which indicates a moderate amount of superposition error. Figure 3b shows why some manufacturers specify linearity error as the maximum deviation from a best fit straight line rather than a straight line through the end points. You can see, in this example, that a linearity error specification of ±1/2LSB proves easier to meet when using the best fit straight-line method. In a DAC with symmetrical error patterns, as shown in Figure 3a, a straight line through the end points becomes the same as a best fit straight line.

SOURCES OF SUPERPOSITION ERROR

Generally, superposition error in monolithic and hybrid converters results from the feedback resistor, R_f, changing in value as the output voltage varies from 0V to +10V. This apparent nonlinearity comes from the variable power dissipation that occurs in this resistor which can produce a temperature rise (self-heating) of as much as 1°C to 2°C in some DACs. This in turn changes the absolute value of the feedback resistor since it will have a temperature coefficient (TC) of between 50ppm/°C and 300ppm/°C for a thin-film material and over 1,000 ppm/°C for a monolithic diffused resistor. This problem generally does not occur in discrete data converters because the physical size of the feedback resistor is so large that the temperature rise, and therefore the resistance variation, remain extremely small. In a monolithic converter, however, with real estate at a premium, the mass of the feedback resistor is often so small that a large temperature rise will occur for even small changes in power dissipation, due to self-heating.

To determine if the feedback resistor is at fault, substitute a low TC external resistor for the internal feedback resistor of the DAC and see if the nonlinearity disappears. The oscilloscope photograph in Figure 4 shows the results of using the test circuit shown in Figure 2 and the same DACs whose transfer functions appear in Figures 3a and 3b respectively, with the internal feedback resistors being replaced by low TC external resistors. Note that the DAC errors in both cases are now almost evenly distributed about the center of the oscilloscope which indicates that the major cause of the superposition error has been removed. You cannot use an external feedback resistor, of course, in most practical applications because it will cause excessive gain drift since it will not track the internal diffused or thin-film reference resistor with variations in time and temperature.

Superposition error or bit interaction can occur in other ways—by temperature gradients on a monolithic chip which cause the magnitude of a bit output to be a function of the state of the other bit switches, or by feedback resistors which have an appreciable voltage coefficient of resistance (VCR), such as diffused resistors might. Again, the presence of superposition error does

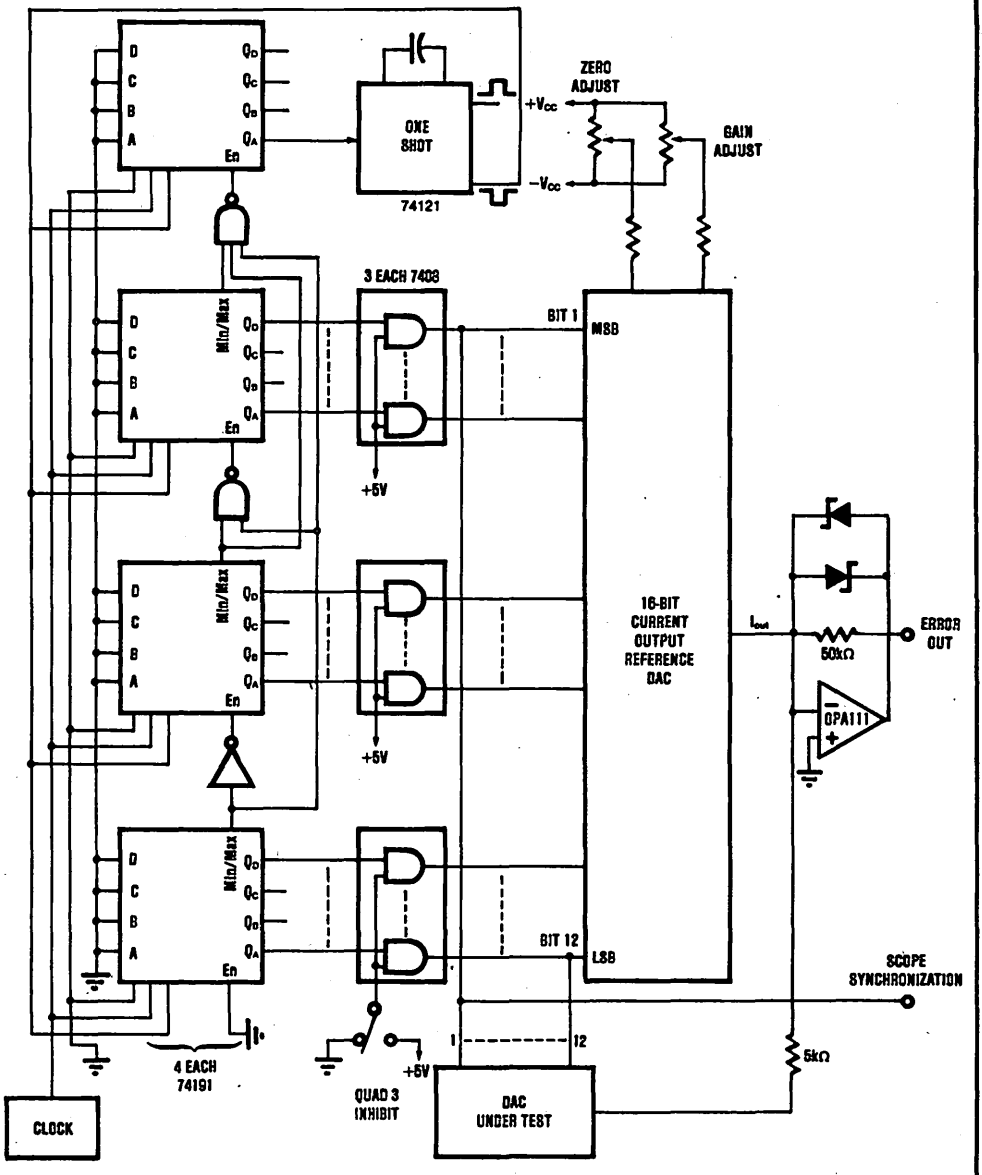
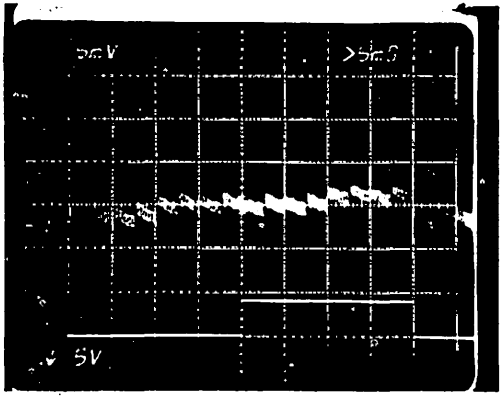
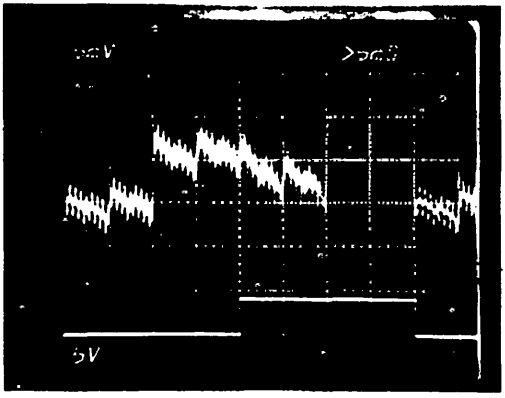


FIGURE 2. This tester works well for 8-, 9-, and 10-bit converters. For a 12-bit DAC, the 4,096 segments displayed on the CRT are spaced so close together that the switching transients create a wide band of noise making it difficult to tell if the converter meets its specification, especially with a linearity error near the ±1/2LSB limit. One way around this problem, if you assume that the errors contributed by the last four bits of the DAC are small, entails inhibiting these bits with the AND gates shown.



(a)



(b)

FIGURE 3. In these scope waveform photographs showing the output of the test circuit in Figure 2, the top traces indicate the linearity error and the bottom traces reflect the status of the MSB of the input code. The hybrid DAC (a) exhibits little superposition error, while the asymmetry of the linearity error (b) about midscale shows superposition error for the monolithic bipolar DAC. The MSB transition marks the horizontal center.

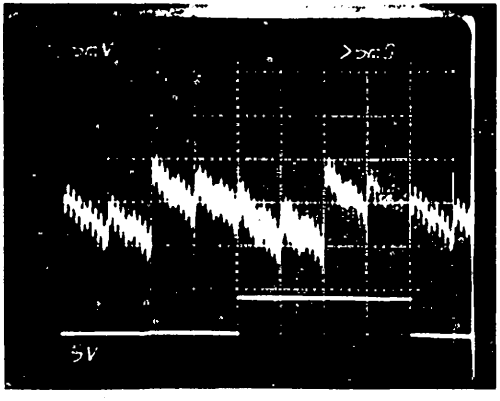


FIGURE 4. An external feedback resistor can decrease superposition error for the monolithic bipolar DAC shown in Figure 3b.

not mean a DAC will not meet its linearity specification, but you will need more extensive testing to verify if it does.

Superposition error, however, is by no means the only source of linearity error. Pay attention to your wiring whenever you use or test a DAC. When critical portions of a circuit share the same metallization path (e.g., a metallization path on a monolithic chip or in a wirebond; the contact resistance of a socket; or the wiring resistance of a test circuit), varying voltage drops caused by changing current levels can cause serious errors which could "drown out" any existing superposition error.

You can minimize the effect of wiring resistance (R_w) external to the DAC by paying careful attention to the grounding and connection scheme employed. Figure 5a shows a correct connection configuration that you can use with most commercially available DACs to yield maximum accuracy. You can reduce or eliminate the effects of various wiring and contact resistances, R_1, R_2, R_3 and R_4, as follows:

- R_1 appears in series with the feedback resistance and therefore introduces only a gain error that can be nulled during calibration.
- R_2 appears inside the output amplifier feedback loop and the loop gain will reduce its effect.
- R_3 appears in series with the load resistor and will cause an error in the voltage across R_L. One-half LSB error would result at full load for $R_3 = 0.02\Omega$ for a 16-bit DAC. Therefore, if possible, you should sense the output voltage in such a way as to include R_3. Figure 5b illustrates the optimum connection made possible by the ground sense pin available on some higher accuracy DACs. In the configuration shown, $R'_F = R_F$ and $R_B = R_{DAC}$. This causes rejection of any signal developed across R_3 as a common mode input, and R_3 will not affect the voltage across R_L. This configuration will also reject noise present on the system common.
- R_4 remains negligible in both circuits with ground connections made as shown.

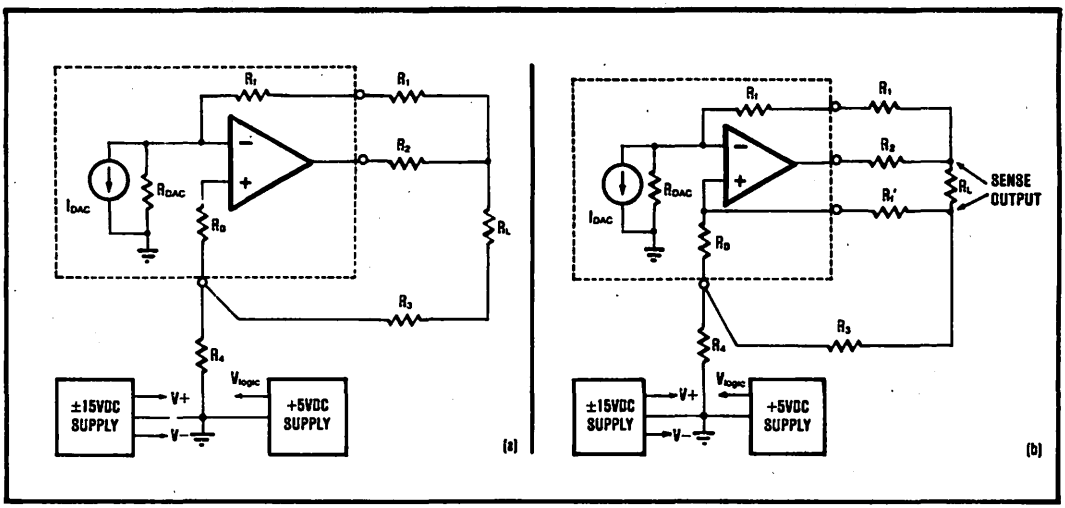


FIGURE 5. These connection diagrams show how to reduce the effects of wiring and socket resistance for a typical DAC (a) and a high accuracy DAC (b). Resistors R_1, R_2, R_3, and R_4 represent wiring and contact resistance.

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18-BIT HYBRID D/A CONVERTER BREAKS SIZE AND PERFORMANCE BARRIERS

In the world of high resolution, true 16-bit accurate digital-to-analog converters, most designs have been restricted to modular "bricks." Such modular designs, by virtue of their size and complexity, take up needed PC board space in user applications. Other disadvantages for modular designs include large power dissipation, long warm-up times and high costs. Now, a new hybrid 18-bit digital-to-analog converter has entered the high-resolution market. Containing a precision 2ppm/°C 10V reference, monolithic 18-bit DAC chip with laser-trimmed current sources, and a low noise, high-speed-output operational amplifier (I/V converter), the Burr-Brown 18-bit DAC729 is a first among the next generation of D/A converters. The DAC729 is fully contained within a 40-pin double-wide side-brazed package. the DAC729's small outline makes it ideal for user applications where precision accuracy is needed without compromising PC board real estate. With its compact size, multiple DAC729s can be used with external latches to interface to a user's data bus to create a system of programmable voltage or current sources, all on one PC board. An equivalent system, built around modular D//A converters, would require many separate PC boards to implement.

The DAC729 is a complete D/A converter within itself. No external components or adjustments are required to perform 18-bit conversions with an integral linearity accuracy of ±76μV. Moreover, the DAC729 was designed to permit maximum user flexibility. In some systems, multiple devices, including the D/A converters, must track each other over time and temperature. For such cases, all devices that must track each other are referenced to a global system reference voltage. The DAC729 has the option of using such an external voltage reference so that the gain of the DAC will track changes in the external reference potential. If an external reference is not needed, the DAC729 internal 10V reference can be used by connecting the Reference Out and Reference In pins together.

The DAC also has an uncommitted operational amplifier I/V converter which is normally used for voltage output applications to achieve output ranges of 5V, 10V or 20V (unipolar or bipolar offset modes of operation). The internal amplifier is the best overall choice for applications where low noise and high speed are needed at the same time. However, if noise reduction is more important than speed, and external low-noise op amp such as the Burr-Brown OPA27 can be used instead. If an application requires current out operation, a current output of 0 to −2mA for unipolar operation or ±1mA for bipolar operation is provided. The absolute accuracy of this output current is ±0.1% of full-scale range (FSR). This allows the output range to be accurately changed, for example to 10.24V, by simply adding an external 240Ω 1% resistor in series with the DAC feedback resistor.

In addition, while the DAC729 can perform conversions to an accuracy of ±76μV or 1/2LSB at the 16-bit level, external bit adjustment pins are provided for the first four MSBs so that higher accuracy can be achieved with external adjustment (see Figure 1). 18-bit accuracy is typical provided external adjustment of the MSBs is done. With 40 pins available, the DAC729's pinout is designed to permit maximum use flexibility, all in a single double-wide package.

DESIGN GOALS

The goal in designing the DAC729 was to make a hybrid 18-bit D/A converter, which would fit into a double-wide package, with performance equal to or better than the Burr-Brown 16-bit accurate modular DAC73. The size requirement of the DAC729 was important so as to optimize a precision D/A converter which could easily be accommodated in applications such as automatic test equipment, precision voltage sources, digital audio, analog-to-digital converters and robotics. Alongside the goal of

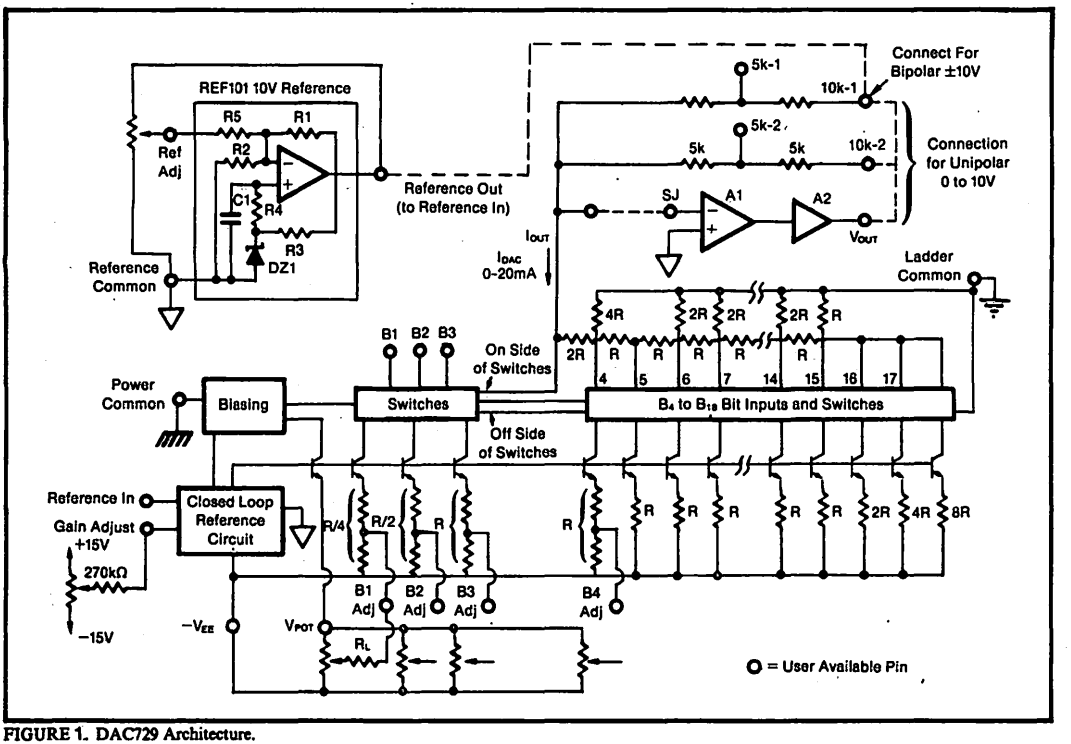

FIGURE 1. DAC729 Architecture.

designing the part to fit into a small outline package was the goal of reducing the complexity or chip count of the part. With reduced complexity came lower cost and higher reliability. Performance, however, was not traded off for reduced complexity. A summary of preliminary specs for the DAC729 such as linearity, drift, noise and settling time are shown in Table I.

TABLE I. Preliminary DAC729 Data Sheet Specifications.

Specification	Limit	Units
ACCURACY		
Linearity Error at +25°C	0.00075	% of FSR
Gain Error: Voltage	0.1	% of FSR
Current	0.1	% of FSR
Offset Error: Unipolar	2	mV
Bipolar	5	mV
10V Reference	5	mV
DRIFT		
Linearity	0.5	ppm/°C
Gain	5	ppm/°C
Offset	5	ppm/°C
10V Reference	2	ppm/°C
NOISE (Unipolar)		
Voltage at 100kHz	70	μV, rms
Current at 100kHz	4	nA, rms
SETTLING TIME (to .00075% of FSR)		
10V Step (Unipolar)	10	μs
20V Step (Bipolar)	10	μs
Slew Rate	20	V/μs
I_{OUT} 2mA Step	300	ns
SIZE	50.50 × 15.75 × 8.40	mm (L × W × H)

ARCHITECTURE

A block diagram of the DAC729 is shown in Figure 1. The architecture of the DAC is basically made up of four sections: 1) 10V reference; 2) Closed-loop reference circuit; 3) Output I/V converter; and 4) DAC current sources and R-2R ladder.

10V REFERENCE CIRCUIT

The 10V reference is an improved version of the Burr-Brown REF101 precision 10V reference. The reference consists of a low-noise OPA27 op amp, thin-film nichrome resistor network and an ultra-stable reference zener diode. Capacitor C1 was added to the REF101 circuit to create a pole at $f = 1/2\pi R4C1 = 3.5kHz$ to eliminate high-frequency noise from the reference zener. The reference, as well as the other components of the DAC729, undergo a burn-in at 125°C to insure longterm stability. After burn-in, the reference's TC is determined so that the operating current of DZ1 can be trimmed at package level to give a reference drift spec of less than 2ppm/°C. The burn-in of the reference and zener diode results in a typical stability rating of 25ppm/1000 hours. The reference output is available at the Reference Out pin of the DAC and can be used as ultra-stable 10V source to supply up to 5mA to external loads. The reference has an adjustment pin, Reference Adjust, available which can be directly connected to a potentiometer, as shown in Figure 1, in order to adjust the Reference Out voltage to 10.0000V.

CLOSED-LOOP REFERENCE CIRCUIT

The closed-loop reference circuit provides the DAC current sources with the proper bias voltage for operation. The closed-loop reference output is dependent upon the input voltage Reference In. Reference In is normally tied to the Reference Out pin of the DAC, but can be connected to an external reference voltage. Similar to multiplying D/A coverters, the DAC729 will track ratiometrically to the voltage applied to the Reference In pin. However, the Reference In voltage must be held within a range of 10V ±0.5V for proper operation. For users with external reference voltages outside this range, a possible solution is to scale the external voltage to 10V so that it can be used. Whether internal or external reference are used, the DAC current sources will track the Reference In potential to better than 3ppm/°C over a temperature range of −25 to +85°C.

The closed-loop reference must also track changes in the minus power supply, $-V_{EE}$. This is because the output current of any given current source is determined by the total voltage drop across its base-emitter junction and emitter degeneration resistor. If this voltage is not held constant with changes in $-V_{EE}$, the DAC output current will be modulated relative to $-V_{EE}$.

The closed-loop reference has a gain adjust pin, which can be used to adjust out any DAC gain errors. The gain adjustment pin can be connected to an external potentiometer and current limiting resistor as shown, or it can be used with an external 8-bit calibration DAC. The gain adjust will rotate the DAC transfer function around BPO with an adjustment range of 0.3% of FSR as shown in Figure 2a. However, if gain rotation about BPZ is desired, and the internal 10V reference is tied to Reference In, the Reference Adjust pin can be used. Any changes in the Reference In potential will rotate the DAC transfer function around BPZ, as shown in Figure 2b.

The actual circuit for the closed-loop reference consists of a servo amplifier and bias circuit which interfaces to the DAC current mirror. Several .01μF chip capacitors are used with the servo amplifier and bias network to achieve fast current-out settling time and low-wideband noise. I_{OUT} settling time is typically 300ns to 0.00076% of FSR and current-out noise is 4nA rms at 100kHz. This type of performance is not easily achieved on completely monolithic DACs because large value capacitors are not practical to integrate.

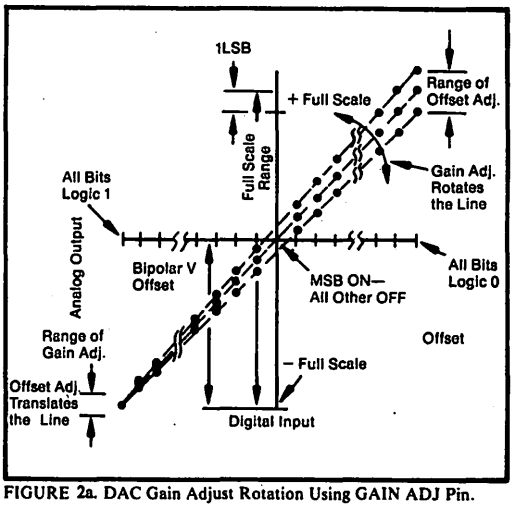

FIGURE 2a. DAC Gain Adjust Rotation Using GAIN ADJ Pin.

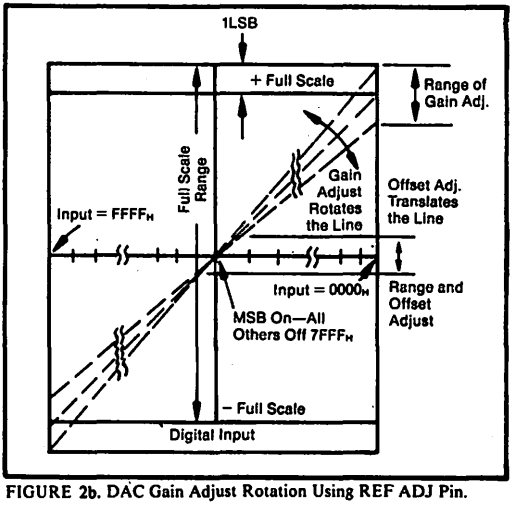

FIGURE 2b. DAC Gain Adjust Rotation Using REF ADJ Pin.

OUTPUT I/V CONVERTER

The output I/V converter is made from two separate monolithic components, A1 and A2. A1 is a single-op-amp version of the Burr-Brown dielectrically-isolated FET OPA404 quad-op amp having a slew rate of 20V/μs and a wideband noise spec of $12nV/\sqrt{Hz}$ at 10kHz. A2 is a unity gain, high-speed buffer capable of driving a 5mA load. A two-chip approach was taken in the design of the I/V converter in order to reduce thermal feedback from the power-sourcing-output stage to the op-amp-input stage. Such thermal feedback, if occuring on A1, would cause the input offset voltage, V_{OS}, of A1 to change with the DAC's input code due to thermal gradients on the chip. This would cause apparent linearity errors in the DAC transfer function, as the DAC output is defined as,

$$V_{DAC} = I_{DAC} \times R_{FB} + V_{OS} \times \frac{1 + R_{FB}}{R_{LADDER}}$$

where R_{FB} is the I/V converter feedback resistor and R_{LADDER} is the R-2R ladder impedance of the DAC. Such linearity errors due to the I/V converter's V_{OS} changing could not be trimmed out during laser-trim. With the two-chip design, however, A1 is looking into A2's input impedance of 1.5MΩ. Thus, the output stage power dissipation of A1 is never more than 17μW for a 10V output swing. The DAC output stage buffer A2, on the other hand, can deliver tens of mW to external loads without thermal feedback to A1's input stage, while maintaining a total I/V converter linearity of 18 bits.

18-BIT DAC CHIP

The heart of the DAC729 is the 18-bit monolithic DAC chip, containing 22 switchable current sources and R-2R ladder, as shown in Figure 1. For simplicity, bits 1 and 2 are shown as only having one transistor current source and scaled emitter resistance. In actuality, four parallel connected current sources are used for the MSB and 2 parallel connected sources for bit 2. The remaining current sources are scaled with the R-2R network to achieve binary ratioing of the DAC output current.

Bit adjustment pins are available to the user for adjusting the linearity of the first four bits. By using these pins. DAC linearity can typically be adjusted to an 18-bit level of accuracy. The bit adjustments are accomplished by summing an external current into the DAC bit-current source. The emitter resistors of bits 1 through 4 are tapped and brought out to external pins. By using an external potentiometer and a series current limiting resistor, R_L, an offsetting current can be produced, as shown in Figure 1 for the bit 1 current source.

The DAC729 employs a unique approach to bit adjustment. As discussed earlier, changes in the $-V_{EE}$ supply voltage can be a potential source of error in the bit-current sources. The same problem exists for the bit adjustments unless the tapped voltage of the pot tracks equally to the voltage potential at the bit adjust pin. Otherwise the voltage drop across R_L will vary with $-V_{EE}$ and cause the bit weight to change. To overcome this problem, the 729 uses a pin to which all external bit adjustment pots are to be connected. Named $V_{POTENTIOMETER}$, or V_{POT} for short, this pin provides a voltage which will track the internal current source base rail as the $-V_{EE}$ power supply fluctuates. V_{POT}'s voltage is derived from an emitter follower connected to the current mirror-base rail. This emitter follower acts as an equivalent DAC current source, with its output current taken to ground, when the external pots are connected from it to the $-V_{EE}$ supply. Thus, as the minus supply moves up or down, the voltage across the pots will remain constant, similar to the DAC current sources. This is important, for example, if at one time the DAC's linearity was adjusted with $-V_{EE} = -15V$, but then at a later time $-V_{EE}$ was equal to $-14V$. The external connections for the adjustment pots are as shown, with only the series current-limiting resistor, R_L, shown for bit 1 for clarity.

There are four feedback resistors available to the user. These feedback resistors have values of 5kΩ and 10kΩ. They can be used in several ways to provide a wide variation of gain and offset modes. With the DAC output current I_{DAC} having a range of 0 to −2mA, 10k-1 can be connected to the 10V Reference In pin to generate a 1mA offset current for bipolar operation, thus making a ±1mA current at the I_{OUT} pin. For the above configuration, if 5k-2 is used as the I/V converter feedback resistor, an operating range of ±5V will exist. If 10k-2 is used instead, the range will be ±10V. For unipolar operation, 10k-1 and 10k-2 can be connected together to give 0 to +10V operation. Zero to +5V can be achieved by connecting all feedback resistor pins together in order to make an equivalent 2.5kΩ resistor. All feedback resistors have absolute tolerances of ±0.1%.

DAC ERROR BUDGET ANALYSIS

The design of the 18-bit DAC chip (where the weight of an LSB is 2^{-18} or 0.00038% of FSR) turned out to be a real challenge. The design issues that needed special attention included:

1. matching and tracking over temperature of the resistors and the transistors in the switchable current sources;
2. matching critical IR drops in the interconnections of aluminum (which has a temperature coefficient of about +4000ppm/°C);
3. achieving fast settling time from transients created by dynamic switching signals;
4. reducing errors caused by thermal changes and thermal gradients across the chip;
5. minimizing the sources of shot and Johnson noise;
6. reducing superposition errors in order to achieve monotonic operation;
7. achieving good long term stability.

The most critical design requirement is to maintain low integral linearity error (ILE) over temperature. An analysis of the major contributions to this error will be done at the major carry where the input code changes from 011---111 to 100---000.

First let us consider the VBE matching in the current sources required to limit the ILE drift to ±1/2LSB at the

17-bit level (±3.8ppm of FSR) over a temperature span of 25°C (ILE drift of 0.15ppm/°C).

This is best demonstrated with the 4-bit DAC example shown in Figure 3. Figure 3a shows the input/output transfer functions of a perfectly calibrated DAC at temperature T_0. Bits 2–4 are considered to be ideal or reference bits for the purpose of this analysis; therefore their value will remain constant. At temperature T_1, Bit 1 has shifted in value by 1LSB as shown in Figure 3b. Since ILE is defined as the worst case deviation from a straight line through the DAC end points, our example has an ILE of ±1/2LSB. The worst case ILE often occurs at the major carry, so this simplified analysis actually gives a good estimation of the precision required to maintain ±1/2LSB ILE.

For the following calculations in this section, the 18-bit DAC can be simplified as illustrated in Figure 3c, where bits 2–18 are merged into a "reference" current source. When we apply the above reasoning to our 18-bit DAC, we see that a shift of ±1/2LSB in the ILE (at the 17-bit level) will be caused by a Bit 1 shift of 1LSB, which is 7.6ppm of FSR or 76μV. Note from Figure 3c that R_1 = 5kΩ and has 5V across it. The output for Bit 1, E_{O1}, is also 5V since R_{FB} = 5kΩ; therefore there is a one-for-one relationship between a shift in VBE_1 and a change in E_{O1}.

Therefore, the maximum allowable shift in VBE_1, is 76μV at T_1. Next we need to find the initial VBE matching required from wafer processing. It is known that VBE tracking between two transistors will vary 3.3μV/°C per each millivolt of VBE mismatch.[1] Therefore the VBE matching requirement is given by

$$VBE_{Q\,1A} - VBE_{Q\,REF} = \Delta VBE = 76\mu V \div [(3.3\mu V/°C)/mV \times 25°C] = 0.9mV \quad (1)$$

Next we will find the temperature tracking (Equation 6) requirement of R_1 relative to R_{REF}. Because of the unity gain of Bit 1, E_{O1} can be written as

$$E_{O1} = 5V \times R_{FB}/R_1 \quad (2)$$

Expanding and solving we find that

$$E_{O1} + \Delta E_{O1} = 5V \times R_{FB}/(R_1 + \Delta R_1) \quad (3)$$

then

$$\Delta E_{O1}/E_{O1} = -(\Delta R_1/R_1) \quad (4)$$

but $E_{O1} = 1/2E_O$ (at full scale), therefore the maximum shift allowed in R_1 is

$$\Delta R_1/R_1 = -2 \times (\Delta E_{O1}/E_{O\,(AT\ FULL\ SCALE)}) = 2 \times 7.6ppm = 15ppm \quad (5)$$

From this result the ratio tracking of R_1 to R_{REF} is

$$15ppm/25°C = 0.6ppm/°C \quad (6)$$

The third major contributor to shift in Bit 1 is Beta mismatch and drift in the current source and switch transistors. This same 0.6ppm/°C ratio tracking from Equation 6 applies to I_{O1} drift relative to I_{REF} drift (see Figure 3c). Because Beta in silicon transistors has a large TC of +5000ppm/°C, it is important that Beta be well matched to achieve 0.6ppm/°C ratio tracking. Starting with

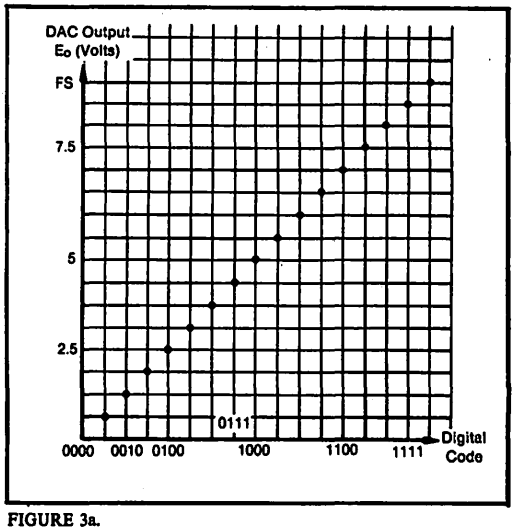

FIGURE 3a.

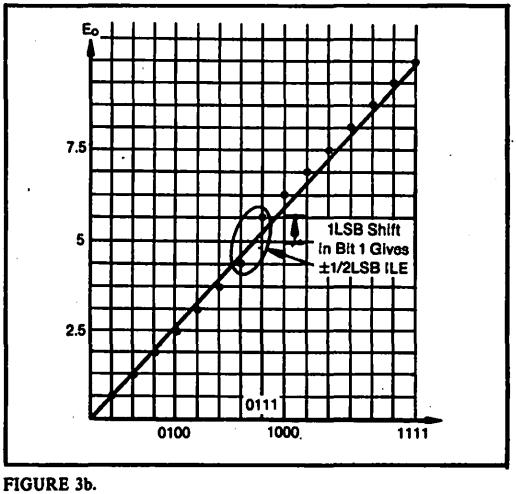

FIGURE 3b.

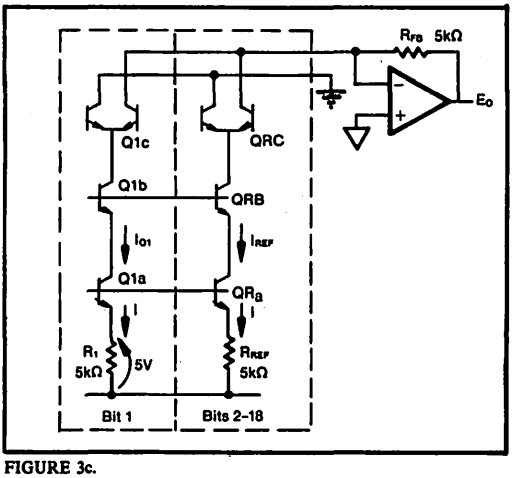

FIGURE 3c.

$$I_{O1} = [\beta_1/(\beta_1 + 1)] \times I$$

and (7)

$$I_{REF} = \beta_R/(\beta_R + 1)] \times I$$

the temperature drift of a mismatch between I_{O1} and I_{REF} due to Beta mismatch is given by

$$\Delta [(I_{O1} - I_{REF})/I_{REF}] \div \Delta T \approx \beta/\beta \times 1/\beta \times 5000\text{ppm/°C} = 0.6\text{ppm/°C} \quad (8)$$

If $\beta = 150$, then

$$\beta/\beta = (0.6\text{ppm/°C} \div 5000\text{ppm/°C}) \times 150 \times 100\% = 1.8\% \quad (9)$$

If cascode transistors Q_{1B} and Q_{RB} in Figure 3c are mismatched by 1.8%, another 0.6ppm/°C error must be added. The same is true for switch transistors Q_{1C} and Q_{RC}, giving a total worse case error of 1.8/°C. Fortunately due to averaging, the errors will rms (root mean square) giving a total error multiplier of $\sqrt{3}$ instead of 3. Therefore, Beta match must be $1.8\%/\sqrt{3} = 1.0\%$, which is not an easy wafer processing requirement.

In summary, each of these 3 error sources, namely VBE, Beta, and resistor matching can produce 0.15ppm/°C of ILE drift. When we rms these 3 drift sources the ILE result becomes $0.15/°C \times \sqrt{3} = 0.26$ppm/°C.

ILE drift from the first lot of prototype units ranged between 0.1 and 0.2ppm/°C, however, data from three lots will be required before a final specification can be determined.

SUPERPOSITION ERRORS

To achieve a ±1/2LSB ILE and monolithic operation, low superposition errors are required.[2] Superposition error is defined as a bit weight interaction that causes an individual bit weight to be dependent upon the ON/OFF state of other bits.

The management of superposition errors becomes extremely important during chip layout. Obviously, IR drops in aluminum interconnects must be considered, but a more subtle problem is the management of thermal gradients, especially those due to variable power sources. The main power offenders are:

1) the DAC output amplifier which must deliver up to 2mA to R_{FB} and 5mA to an external 2k load as the output swings 0 to 10V. This is a variable power source of 55mW;
2) the reference output amplifier which delivers up to 10mA to the reference zener and an external load; and
3) the 20mW variable power in R_{FB}.

In order not to compromise thermal performance it was decided not to include the output amplifier and the reference amplifier on the 18-bit DAC chip. R_{FB} cannot conveniently be removed from the chip as it must ratio match and track the bipolar offset resistor and the reference input resistor in the closed-loop servo amplifier. Therefore, R_{FB} was carefully positioned layout on a thermal centerline above the three MSB (most-significant-bit) current sources. R_{FB} was also spaced at a maximum possible separation since temperature rise is inversely proportional to the distance from a power source.

The proper placement of R_{FB} minimizes thermal gradients across the MSBs, but another problem with R_{FB} must be considered. Self heating in R_{FB} changes its value because of its TCR.[3][4] This effect has been reduced by making R_{FB} physically large in size and by selecting a low TCR nichrome resistor process of less than 25ppm/°C. R_{FB} is actually four separate series/parallel connected resistors so that the maximum power in each resistor is 5mW. The net result is a self-heating error of under 2ppm of FSR.

As a result of these efforts, superposition errors have measured to be less than 30μV.

Because the DAC729 has a gain drift of 5ppm/°C, another error source must be considered when the package changes temperature. For example, a 5mA external load plus a 2mA load in the I/V feedback resistor, R_{FB}, produces a 55mW power change as the DAC output varies from 0 to +10V. Since the junction-to-ambient thermal resistance of the package is about 25°C/W, the DAC729 will experience a temperature rise of 1.4°C. This temperature rise will cause the FSR (full-scale range) to shift by 7ppm or 70μV as the package heats up. Unfortunately, this shift will take several minutes to reach its final value because the package has a long thermal time constant (due to its large thermal mass). In applications where the DAC output voltage must remain constant for hundreds of milliseconds at a time, the output load current should be restricted to 1mA or less to minimize this effect. If 5mA or greater external load is required, an external I/V converter op amp should be used.

When using an external op amp I/V converter, instead of the DAC729's internal converter, it is cautioned that care be taken to choose an op amp which has sufficient rejection of thermal feedback. Otherwise, the DAC729's 16-bit linearity can easily be degraded to around 14-bits just by the external op amp.

In applications where absolute accuracy is paramount, even the low-gain-drift specification of 5ppm/°C can not be tolerated because of package temperature changes due to varying load currents or changing ambient temperature. In these cases one must resort to techniques such as the use of automatic gain recalibration (using hardware and/or software) or by using ratiometric measurement techniques. A ratiometric circuit is shown in the applications section. For other applications, such as digital audio where the output signal is AC coupled, only ILE is important in order to minimize harmonic distortion.

GROUNDING CONSIDERATIONS

In order not to compromise the DAC729 performance, three separate supply common pins have been used as shown in Figure 1. Internally the commons for A1, the closed-loop reference loop, and the 10V reference are "star" connected to the Reference Common pin. Current flowing in this pin is constant and independent of input code or output load variations. Variable currents from the biasing circuits are tied to Power Common. Finally the R-2R ladder common and the OFF side of the differential bit switches are connected to Ladder Com-

mon, in order to prevent code-dependent superposition errors. These three common pins are then star connected to the user's system referene common point, which is usually the PC board ground plane surrounding the DAC729.

APPLICATIONS

An example of using the DAC729 in a ratiometric measurement circuit is shown in Figure 4. This circuit can be used to test the linearity, gain and offset of the device under test (DUT). Since the DUT and the measurement ADC both use the DAC729's internal 10V reference, all devices track this reference. Measurements made on the DUT are taken by setting the DAC729 input code to that of the DUT. The resulting outputs of both the DUT and DAC729 are then converted to an error voltage, gained up by 100 by the instrumentation amplifier, A1. The resulting error is then measured by a 12-bit ADC. 12 bits of accuracy for the ADC is sufficient since the error signal, V_{ERROR}, has been gained up by 100. The actual DUT voltage can then be calculated by,

$$V_{DUT} = (V_{ERROR}/100) + V_{729}$$

Because of the DAC729's 16-bit accuracy, V_{729} is set to be the ideal output of the DUT.

Because the DAC729 has a low-noise current output, it is suitable as a submodule in a high precision successive approximation A/D converter. Such an application is shown in Figure 5. The active clamp, which lowers the RC time constant at the DAC output, is optional as a speed improvement. A high-speed preamp ahead of the comparator is required to amplify the small value of an LSB. Although the A/D coverter looks simple, in practice a great deal of skill is required to implement this circuit especially because of the DAC and comparator sensitivity to coupling from logic signals.

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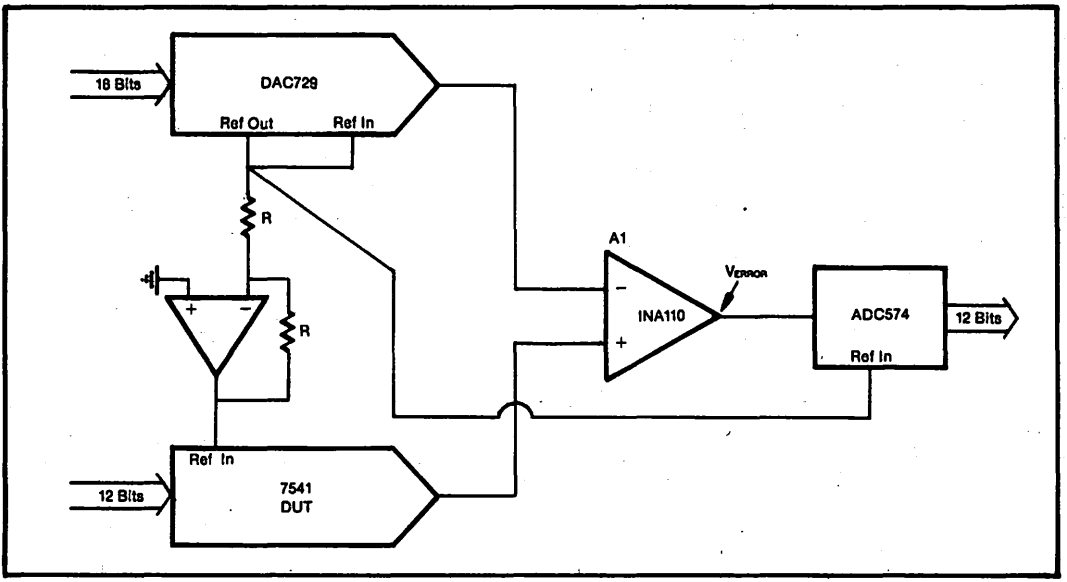


FIGURE 4. DAC729 in Ratiometric Measurement Circuit.

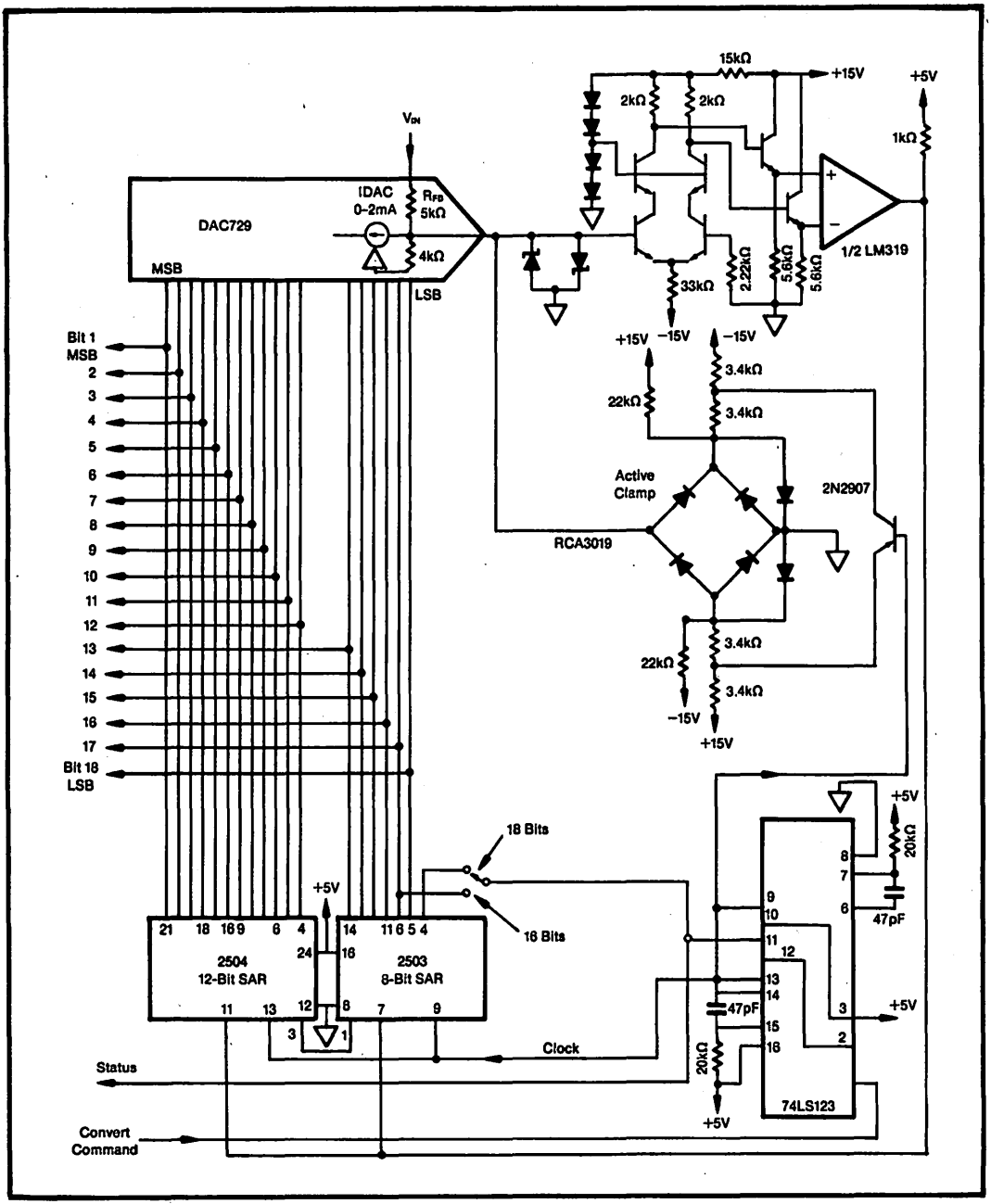


FIGURE 5. Precision SAR A/D Conversion Circuit.

DC-TO-DC CONVERTERS

Just about all electronic circuits require a DC power source. Unfortunately not all circuits can operate with just one DC level. The DC-to-DC converter was developed to allow use of different DC levels without the proliferation of large expensive central power supplies. Before the advent of switching DC-to-DC converters, a linear power supply output had to be incorporated for each DC level required. With one central supply, this entailed the design of a complex power distribution network. This network required sophisticated ground systems and filtering, and was very inflexible to changes. The first solution was to incorporate modular AC supplies distributed throughout the system. This eliminated many of the ground return and inflexibility problems. On the other hand, 60Hz power spread through the system created more noise problems than it solved. In addition, the lower efficiencies of linear supplies tended to make these systems into power hogs.

The DC-to-DC switching converter gave us a highly efficient power distribution capability flexible enough for modern electronic systems. Although the module itself is more complex and difficult to design, its use is relatively easy. The high power efficiency stems from use of switching speeds normally in excess of 100kHz. Since this is normally much greater than the system bandwidth, its associated noise can be easily controlled. The high speed also allows us to replace the bulky, inefficient 60Hz transformers with compact ferrite core transformers. The power densities for DC-to-DC converters are usually in the realm of 3W dissipation per cubic inch. This compact size allows efficient utilization of board space.

The DC-to-DC converter input voltage is normally one of six levels. These are 5, 12, 15, 24, 28, and 48V. The input voltage or main supply voltage is dictated by the type of system being designed. For example, a predominately TTL logic design would have a 5V main supply and utilize DC-to-DC converters for generating spot power for its linear circuits. A telecommunications device, however, would probably use a 48V central supply. Like the DC-to-DC converter input, the output also has a standard set of voltages. These are 5, 12, and 15V. The voltages are available with both single and dual outputs. All of the above are available as off-the-shelf items, although just about any other voltage may be obtained on a custom basis.

There are two basic types of switching DC-to-DC converters: units with voltage isolation and those without. The unisolated type usually consist of a boost or buck circuit, depending upon whether the output voltage is more or less than the input voltage. Isolated units utilize a transformer. This not only allows an efficient voltage translation, but also allows for channel-to-channel or input-to-output isolation. The basic layout is shown in Figure 1. The DC is changed to an AC signal, transformed, and then converted back to a DC signal. The input filter performs two functions. One minimizes the ripple reflected back from the modulator; the other acts as an input filter to minimize noise from the system power supply. The modulator performs the function of switching the input signal so that it can be run through the transformer. The output demodulator extracts the desired DC level and the ouptut filter minimizes the output noise and ripple.

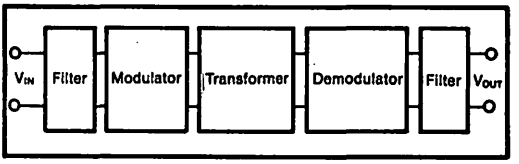


FIGURE 1. Typical DC-to-DC Converter.

INPUT STAGE

The input section consists of a filter and a modulation circuit. The filter is usually a pi type as shown in Figure 2. The main purpose is to filter out the current ripple created by the modulator's switching circuit. The modulation is implemented in three ways. These range from the simple Royer to the more sophisticated flyback and forward converters.

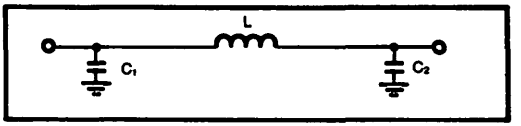


FIGURE 2. Pi Filter.

One of the simplest and probably the oldest methods is the Royer circuit. This circuit is shown in Figure 3. The switching transistors or FETs are driven by secondary windings of the output transformer. The transistors are in a push-pull configuration. Since these windings create a positive feedback, this circuit will self-oscillate and generate a square wave output. Even though the circuit is simple, it is more expensive to construct. The switching frequency may greatly vary from circuit to circuit, creating problems where synchronization is required.

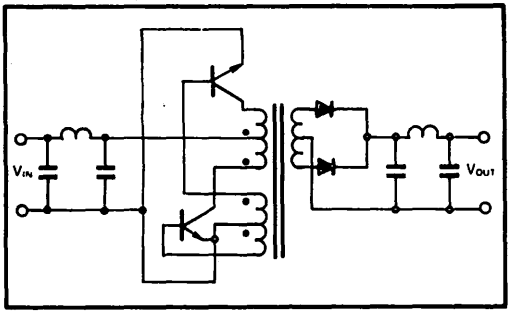


FIGURE 3. Royer Converter.

Both the forward and the flyback circuit use an IC-driven switching circuit as shown in Figure 4. This may be either a square wave or a pulse-width-modulated signal generated as feedback from the output. Pulse-width modulation (PWM) is one way of regulating the output voltage.

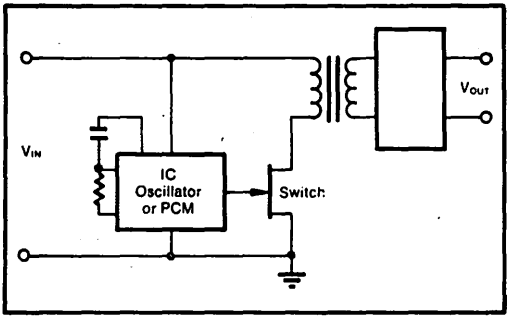


FIGURE 4. Controlled Frequency Switcher.

Figure 5 shows the flyback converter. In this configuration the energy is stored in the transformer's output winding. The energy is only transferred to the output during the time the modulator switch is not conducting. This circuit is slightly less expensive to implement than the Royer or the forward converter. However, it has a higher output ripple voltage than the other configurations.

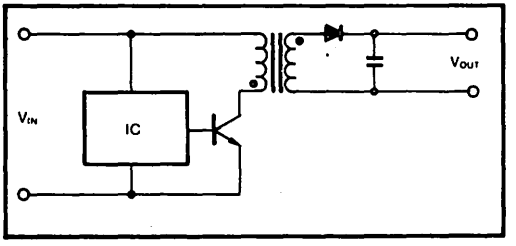


FIGURE 5. Flyback Converter.

In the forward circuit, Figure 6, the energy is stored in the output filter inductor. This allows for a low-noise, full-wave rectifier output. With the addition of a push-pull input configuration, the forward circuit gives us a high-efficiency easy-to-build input modulator.

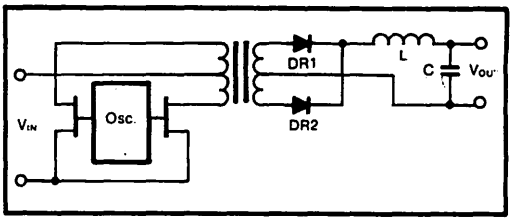


FIGURE 6. Push-Pull Forward Converter.

TRANSFORMER

The modern modular DC-to-DC converter is based on the use of high frequency ferrite materials. Ferrites are ceramic ferromagnetic elements with properties known to have a high degree of reliability and repeatability. Because of its high resistivity, the ferrite core transformer affords a low-loss device in contrast to laminated and powdered-iron core transformers. This along with its excellent long-term time and temperature characteristics, allows us to build efficient modular DC-to-DC converters.

The transformer gives us the isolation along with the voltage translation. Unfortunately, the physical characteristics which afford us good efficiency tend not to give us low cost or good isolation. The two most common types of ferrite transformers used in DC-to-DC converters are the bobbin and the toroid. The bobbin is much cheaper to construct since it lends itself to machine automation. Normally each winding is laid over the last, and the separation is made up of the wire insulation or a thin barrier molded into the bobbin. On the other hand, the toroid allows a better isolation barrier and much closer coupling. The barrier is formed by separating the windings around the toroid, as shown in Figure 7. For isolation voltages specified by the medical market, the toroid is the only practical core type. It allows a wide safe barrier while affording good close coupling. The major drawback with toroids is that the small diameters sometimes require hand winding.

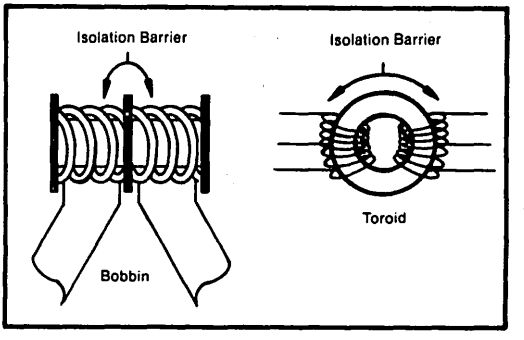


FIGURE 7. Types of Transformers.

OUTPUT STAGE

The output stage is made up of the demodulators, filters, and the regulators. The most common type of demodulator is a rectifier. This may be either a full-or half-wave

type, depending on the amount of ripple allowed in the output. The output windings may be set up to supply isolated and/or unisolated outputs. For isolated outputs the transformer windings must be separate from each other. Isolation voltages equivalent to those obtainable for input-to-output are also available from output channel to output channel. Once rectified, the signal is then filtered in order to minimize the output ripple or EMI/RFI generated by the switching operation. The filter may range in complexity from a simple capacitor to a more sophisticated pi filter. The major limitation on the amount of filtering is usually the physical size of the components. In addition to the filtering, most switching converters utilize a six-sided metal shield to minimize the radiated interference.

REGULATION

There are a number of regulation schemes used in modern DC-to-DC converters. The two types of regulation covered here are linear regulation and PWM regulation.

Probably the most common of these is the linear regulator. This type of device controls the output based on the value of a reference circuit. This type of circuit is very versatile. The only drawback is the cost in terms of efficiency. The voltage in excess of the desired output is usually dissipated in the output stage. However, this type of regulation affords a much faster transient response time. Transient response is the ability of the power supply to respond to changes in load current. It is expressed by the amount of time between the start of the load current change to the time the power supply output returns to within its specified limits. This is shown in Figure 8. For linear regulators there are practically no delays due to load changes.

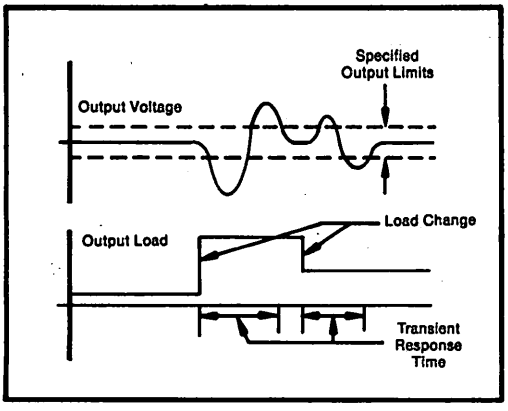


FIGURE 8. Linear Regulator.

Pulse width modulation or PWM is used to control the input based on the amount of sensed output voltage (Figure 9). For isolated outputs, the output is fed back to the input through either a transformer or optical couplers. The major advantage of this circuit is its high

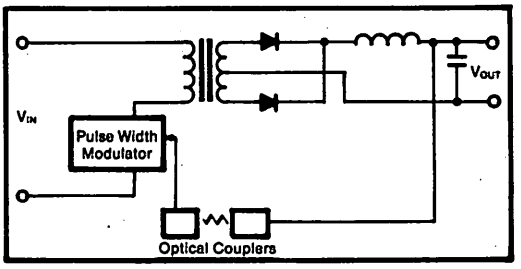


FIGURE 9. Pulse Width Modulation Regulator.

efficiency for widely varying input voltages. The output stage doesn't have to dissipate the excess voltage; instead the output voltage is controlled by varying the power from the input. This circuit has a couple of drawbacks. First, it can be very slow to respond due to the time delay caused by the feedback scheme. Second, it can be a very complex or more expensive device to build.

There are numerous ways to design a DC-to-DC converter. Which design used will depend upon the requirements of the circuit around it. The basic decision to be made is whether to use a standard catalog device which may supply more than your circuit requirements, but has no development costs, or to have a converter designed specifically for your circuit. The latter could be the most economical if the efficiencies of the design are greater than the development cost. There are many standard converters available. Often these will afford the best form, fit and value for your circuit.

DC-TO-DC CONVERTER GLOSSARY

Ambient temperature—The temperature of the air immediately surrounding the power supply.

Barrier—The region or zone which defines the isolated areas.

Burn-in—A screening method described in MIL-STD-883 Method 1015, used to minimize the effect of early infant mortality.

Case temperature—The temperature at the surface of the device.

Crowbar—A circuit designed to protect adjacent circuitry by rapidly shorting the power supply output once a predetermined output voltage is exceeded. This short is removed by either cycling the supply off and on or by a logic input.

Cross regulation—The percentage of voltage change at one output caused by the load change on another output. This applies basically to multiple output supplies.

CSA C22.2—Canadian standard used to define a safe medical-electrical environment.

Current limiting—A protection feature which limits the current to a predetermined value to prevent damage to the power supply or adjacent circuitry. As the overload condition is removed, the supply should return to normal operation.

Derating—A specified reduction in an operating parameter designed to improve reliability by reducing the internal component stress. For example, reducing the power output at elevated temperature.

Dual channel—A converter with two outputs, each of which is isolated from the other. See Figure 10.

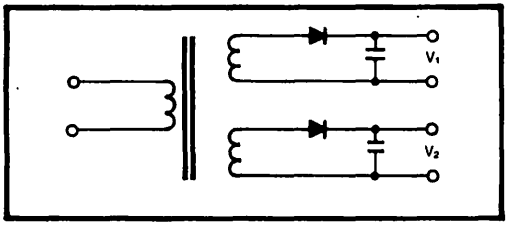


FIGURE 10. Dual-Channel Converter.

Dual output—A set of converter outputs which are not isolated from each other. See Figure 11.

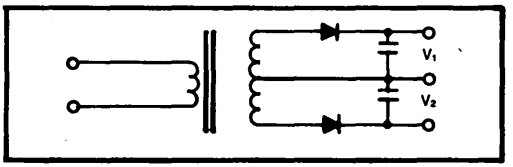


FIGURE 11. Dual-Output Converter.

Efficiency—A percentage measure of power loss in the converter itself. This is defined as the ratio of power out to power in times 100.

EMI—Electromagnetic interference generated by internal high frequency switching. This may be transmitted by radiation or conduction and is minimized by filtering and shielding.

Fault-mode input current—The power supply input current when one or more of the outputs are shorted.

Flyback DC-to-DC converter—A switching DC-to-DC converter in which the energy is stored in the transformer. This type of circuit usually employs one switch and has a half-wave output rectifier. See Figure 5. This is a low cost type of design, but can cause severe EMI problems.

Foldback—A type of protection circuit which causes the output current to decrease as the demand or load increases above the specified level. This protection routine minimizes internal power dissipation under overload conditions. See Figure 12.

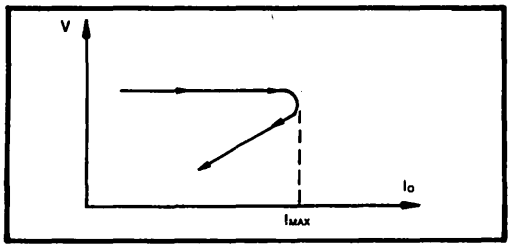


FIGURE 12. Foldback Circuit.

Ground loop—Two or more circuits sharing a common electrical ground line. This usually results in unwanted coupling of one circuit into the other.

Hi-pot test—See high voltage breakdown test.

High voltage breakdown test—A test designed to evaluate the isolation barrier. This test is usually performed at a voltage of two times the continuous rating plus 1000V. On units designed for the medical market, this voltage is defined by the referenced medical standard. In the United States this is UL544.

Input current—full load—The value of input current corresponding to a fully loaded output condition.

Input current—no load—The value of input current corresponding to an unloaded output condition.

Input filtering—Utilized to reduce reflected ripple current on the input of a switching DC-to-DC converter. Most commonly of the pi configuration.

Input rated voltage—The input voltage which produces the rated output voltage. This voltage is the design nominal.

Input voltage range—The high and low input voltage span for which the unit's specifications hold true.

Inrush current—The peak instantaneous input current drawn by a power supply.

Isolation—The electrical separation between input and output of a power supply. This is usually performed by means of a transformer. This separation may also be between output channels.

Isolation capacitance—The capacitance measured across the isolation barrier.

Isolation rated voltage—The continuous voltage for which the isolation barrier is designed. Usually expressed in VDC.

Isolation resistance—The resistance as measured across the isolation barrier.

Leakage current—The current flowing across any isolated barrier of a DC-to-DC converter. This current may be AC and/or DC and is dependent upon the barrier's capacitance and resistance.

Line regulation—The percent change in output voltage as the input voltage is varied over its specified range. This is usually designated with all other parameters at their nominal value.

Load regulation—The percent change in output voltage as the load is varied over its specified range. This is usually designated with all other parameters at their nominal value.

Long term stability—The change of a parameter in percent due to time only, with all other factors held constant.

Master/slave—A power supply which can either synchronize, or be synchronized by, another power supply. For synchronization the internal switching must be operating at the same frequency.

Maximum input current—See inrush current.

MTBF—Mean time between failure. The statistical in-operation time between the first turn on and the time the unit experiences a failure. This time is determined either by elevated temperature life testing or by calculations according to MIL-Handbook-217.

MTTF—Mean time to failure. For an unrepairable unit this is the same as MTBF.

Operating temperature range—The temperature range over which the unit will not experience permanent damage.

Output current range—The current limits over which the DC-to-DC converter is specified.

Output filtering—Filtering used to minimize the output voltage ripple or EMI/RFI generated by the switching operation.

Output rated voltage—The output voltage corresponding to the nominal or design input voltage with the output at the design maximum load.

Output rated current—The output current corresponding to the output rated voltage with the design maximum load.

Output ripple voltage—Noise voltage imposed on the output due mainly to the switching and output rectification. This AC voltage is usually expressed in both Vp-p and Vrms.

Output voltage temperature coefficient—The variation of the output voltage due to the change in the temperature environment while all other parameters are held constant.

Output voltage accuracy—The change of the output voltage in percent from one unit to another due to variations in component parts. This is usually specified with full load and all other parameters at their design nominal.

Pi filter—A type of filter commonly used in DC-to-DC converters. This filter may be used on both inputs and outputs to reduce EMI and RFI. See Figure 2.

Push-pull DC-to-DC converter—A DC-to-DC converter input design that allows the transformer to transmit power in both switch cycles by utilizing a center-taped transformer and two switches. See Figure 6.

Power dissipation—The power loss which is generated by the DC-to-DC converter. This is calculated by subtracting the output power from the input power.

Regulated converter—A DC-to-DC converter which exercises some form of internal control over the output voltage.

RFI—Radio frequency interference. Sometimes generated in the switching operation. Extensive shielding and filtering are used to minimize the effect on surrounding circuits.

Ripple current—The AC variations in input current caused by the switching operation. This is minimized by use of filtering on the inputs.

Royer DC-to-DC converter—A DC-to-DC converter input stage utilizing a secondary winding to control the input switches. See Figure 3.

Short circuit protection—A circuit designed to protect the DC-to-DC converter whenever the output current exceeds a specified level. As the overload condition is removed the supply should return to normal operation.

Six-sided shielding—The practice of encasing the DC-to-DC converter in a metal shield on all sides in order to minimize EMI and RFI.

Specification temperature—The temperature range for which the DC-to-DC converter's parameters will stay within their stated limits.

Stabilization bake—A screening method defined in MIL-STD-883 Method 1008 used normally as preconditioning treatment prior to the conduct of other tests.

Storage temperature—The temperature range which will not cause damage to an unpowered DC-to-DC converter.

Temperature cycling—A screening method defined in MIL-STD-883 Method 1010 used mainly to determine failure due to stresses caused by thermo-coefficients.

Transient recovery time—The time between the start of the load current change to the time the DC-to-DC converter output voltage returns to within its specified limits See Figure 8.

UL544—The United States standard used to define a safe medical electrical environment.

Unregulated converter—A DC-to-DC converter with an output directly dependent upon the input voltage.

VDE750—The West German standard used to define a safe medical electrical environment.

Warm-up time—The time from turn on required for the DC-to-DC converter to reach specified operation.

MINIMIZING THE EFFECTS OF DC/DC CONVERTER SWITCHING NOISE

When dealing with high frequencies, the interaction between devices requires extreme care in setup. Some devices are more susceptible to high frequency noise. This unwanted interaction can ruin the performance of otherwise excellent devices. For our example we will look at the interaction between a DC-to-DC converter's high frequency noise and a wide band isolation amplifier. The DC to DC converter is the model PWR74 and the isolation amplifier is the ISO100.

At first, the use of DC/DC converters may seem trivial. You simply apply a DC voltage to the input and obtain one or more isolated DC voltages at the output. In practice though, things are not that simple. The switching action of the converter's internal circuitry can cause noise at its input, ripple at its output, and radiated interference into adjacent circuits.

All of these undesirable effects can be minimized by the techniques given in this application note. This example, developed for and in use by a customer, typifies the measures that can be taken to optimize practical DC/DC converter applications.

The following parts were used:

DC/DC converter	PWR74
Isolation amplifier	ISO100
L1-L5	100μH RF inductor
C1	10μF
C2-C5	1μF
C6-C9	.01μF
C10	5pF
R1, R2	1MΩ
R4	2MΩ
Z1, Z2	Offset voltage span.
R5, R6	Dimensioning as required.
R3/C11	Low-pass filter at output. Dimensioning as required.

CIRCUIT

In order to be more universally applicable, this circuit (see Figure 1) was designed for three-port isolation. Thus the input from the power supply is isolated from both the input and output sides of the amplifier, which are isolated from each other. The circuit is configured with R1 = R2 = 1MΩ providing unity gain. Selection of non-inverting unipolar or non-inverting bipolar mode is made through jumpers J1 and J2 as shown on the schematic. Setting jumper J3 provides offset adjustment through an auxiliary voltage stabilized with zener diodes.

To suppress any tendency toward oscillation, reduce peaking of frequency response, and limit output noise, the output stage is slightly compensated with C10 = 5pF. Ceramic bypassing capacitors were used for each supply voltage for both input and output sides directly at the IC. (C6 − C9 = .01μF). Finally, the output voltage is available directly at output 1 or through a low-pass filter at output 2.

PCB

Ground planes relating to the three isolation voltages are implemented on the component side of the PC board (see Figure 2). Each is separated by a space sufficient to assure high-voltage isolation. These planes offer low-inductance reference points required by RF applications and also provide guarding for sensitive signal lines. Leakage current across the PCB isolation barriers are minimized by guarding both rows of pins with low-resistance paths to their respective commons. This is done on the component as well as solder sides of the board.

NOISE

If the input voltage to the DC/DC converter is not "clean", its effect on the amplifier will have to be minimized. Using the internal capacitor present in the PWR74, a pi filter was constructed with L1 = 100μH and C1 = 10μF. In addition, the filter suppresses the reflected ripple current of the DC/DC converter caused by the dynamic current component at its switching frequency (about 500kHz). This is of major importance if other circuits are supplied by the input voltage.

Each of the PWR74 output voltage ports contains an internal filter capacitor. An LC filter (L2 − L5 = 100μH, C2 − C5 = 1μF) was used for additional ripple suppression. The filtering of high frequency noise directly at its source not only eliminates conducted noise, but also simplifies circuit layout. The high frequency of the PWR74 demands low effective series resistance (ESR) capacitors for the input and output filters (C1 − C5). For this reason ceramic caps were used.

The PWR74 internal shielding is connected to the $-V_{IN}$ pin of the converter. This "quiet" ground, with respect to radio frequencies, is absolutely necessary for efficiency in shielding radiated noise. RF oscillations on the shield not only would jeopardize its desired effect, but also would become a potential source of distortion to other circuitry.

OTHER APPLICATION CONSIDERATIONS

1. For long input lines to the ISO100, use shielded or twisted pair cable.
2. The ISO100 Input Common (pin 18) and −In (pin 17) should be grounded through separate lines. The Input Common can carry large DC currents and may cause feedback to the signal input.
3. Care should be taken to minimize external capacitance across the isolation barrier.
4. Distance across the isolation barrier between external components and conductor patterns should be maximized to reduce leakage and arcing.
5. Use of conformally coated printed circuit boards is recommended.
6. When in the unipolar mode, the reference currents (pins 8 and 16) must be terminated. I_{IN} should be greater than 20nA to keep internal LED on.
7. The noise contribution of the reference currents will cause the bipolar mode to be noisier than the unipolar mode.
8. The maximum signal output voltage swing is determined by I_{IN} and RF.

$$V_{MAX\ SWING} - I_{IN\ MAX} \times RF$$

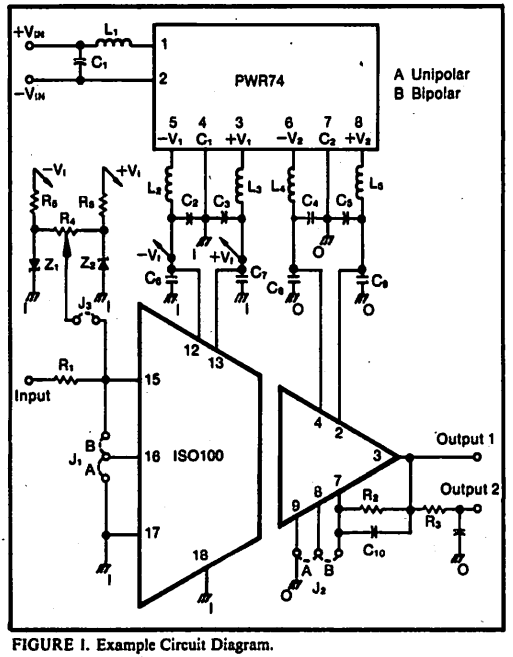


FIGURE 1. Example Circuit Diagram.

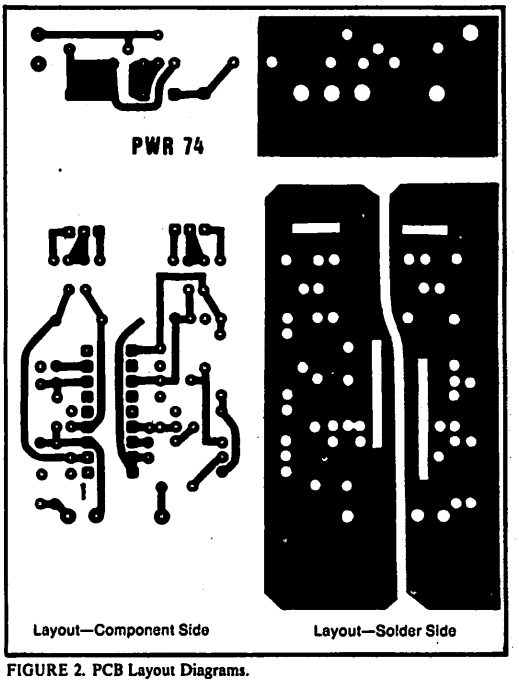


FIGURE 2. PCB Layout Diagrams.

DIGITAL GAIN CONTROL STREAMLINES SIGNAL-ACQUISITION SYSTEMS

A monolithic op amp that includes digital gain control simplifies the design and layout of a signal-acquisition system. By adding some simple circuitry to the op amp, you can combine the part's digital-gain-control function with such functions as automatic gain control and current-feedback amplification.

By adding some simple circuitry to a monolithic programmable gain amplifier (PGA), you can design circuits that combine the PGA's digital gain control with gain-polarity control, automatic gain control, current-feedback amplification, or a sample/hold function or V/F converter.

The monolithic PGA102 op amp (Figure 1a) offers programmable gains of 1, 10, and 100. It includes three input stages with a user-accessible differential input for each; however, only the selected stage closes a feedback loop, so the selected stage's tap in the feedback network determines the operating gain.

The op amp's three input stages sense different taps on a feedback network, and a gain-control circuit activates one of the three by connecting it to the input biasing current source (the other two input stages remain off). The only input stage that determines operating gain is the selected input stage, and it does so by closing the feedback loop. Because it switches the input stages instead of the feedback connections, the op amp can use switched-current circuitry.

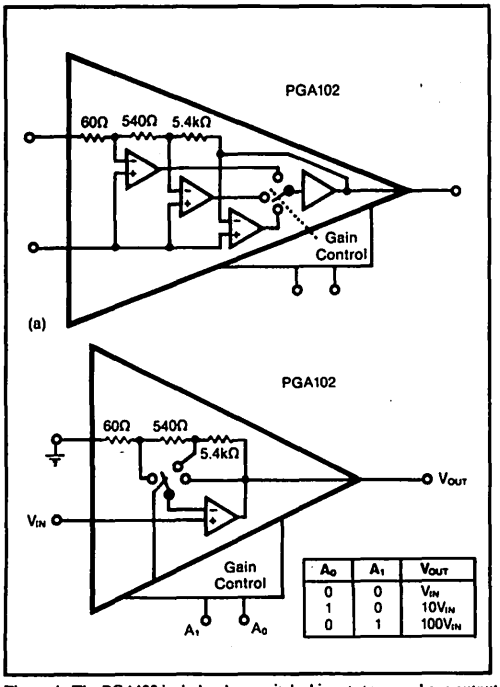


Figure 1. The PGA102 includes three switched input stages and one output stage (a). for most purposes, the circuit can be represented as a switched-gain noninverting amplifier (b).

SWITCHED-FEEDBACK EQUIVALENT

To understand how the PGA102 operates, consider the simplified, symbolic representation of the op amp in Figure 1b. In the figure, a 2-bit digital-control code switches the noninverting amplifier's gain to 1, 10, or 100. The three gain levels offer 0.05% (or better) accuracy; switching between them requires no more than 8μs for 0.01% settling. Furthermore, the amplifier's bandwidth is at least 250kHz at any gain level.

The switched-gain, noninverting amplifier in Figure 1b differs from the actual configuration of the PGA102, however, in that the figure doesn't show any dependence on the offset voltage of the gain range. In the actual PGA102 circuit, each gain range uses a separate input stage with its own offset voltage, so the offset will usually change when the gain changes. You should keep this behavior in mind when you use the simplified switched-feedback model (Figure 1b) to represent the PGA102.

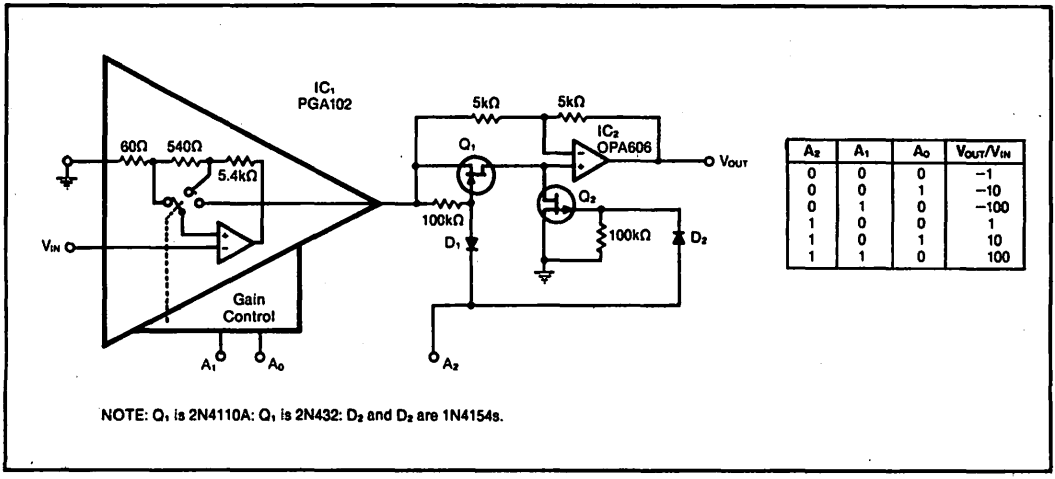
By adding a switched op-amp stage[1] to the PGA102, you can provide digital control of a signal's polarity as well as its gain (Figure 2). The third control bit, A_2, allows you to insert a gain of +1 or −1 in the signal path. Such a circuit would be useful, for instance, in a system in which the amp drives an A/D converter, because A/D converters handle unipolar signals more accurately than they handle bipolar signals.

The logic level of control bit A_2 configures IC_2 as either a voltage follower or as a unity-gain inverter. For example, a high level at A_2 applies forward bias to diode D_2 and pinches off FET Q_2, but applies reverse bias to diode D_1, allowing FET Q_1 to remain on. Under these conditions, the op amp (IC_2) behaves as a voltage follower and tracks the PGA102's output voltage.

CONFIGURE OP AMP AS FOLLOWER OR INVERTER

On the other hand, a low level at A_2 reverses the states of the two diodes and their associated FET switches, producing a unity-gain inverting amplifier. Note that A_2 must drive the FET switches to their pinch-off levels, even in the presence of a large output from IC_1; an output of ±10V, for instance, requires that the control signal have a ±12V range.

This application uses JFETs because they provide make-before-break switching (JFETs are depletion-mode devices, which remain on until they're driven off). Both switches are on for a brief interval when A_2 makes a transition from one state to the other. The switches'



A_2	A_1	A_0	V_{OUT}/V_{IN}
0	0	0	−1
0	0	1	−10
0	1	0	−100
1	0	0	1
1	0	1	10
1	1	0	100

FIGURE 2. By switching an op amp between voltage-follower and inverting-gain modes, you can digitally control both the polarity and the magnitude of gain.

closure would appear to short the PGA102's output to ground through the two JFETs in series. The JFETs have inherent current limits, which prevent shorting, however: The maximum current drain is limited to the lower I_{DSS} value offered by the two JFETs

During an A_2 logic transition from 1 to 0, the gain of op amp IC_2 drops from +1 to near zero (when both FETs are on) and then to −1. This action eliminates output transients because one of the two FET switches is always on, providing a low-impedance path for the discharge of switch capacitance during A_2's state changes. Although you could also use enhancement-mode MOSFETs, such break-before-make devices don't provide a quick-discharge path, so they can permit transients as high as 1.2V during a 30ns switching interval.

Adding the gain-polarity control doesn't have a significant effect on accuracy as long as you use an OPA606 op amp or equivalent and make two circuit adjustments. First, you can reduce the offset voltage by using the op amp's offset-adjust terminals (in any case, the op amp's input offset voltage is divided by the PGA102's gain). Next, you adjust the op amp's 5kΩ resistor values for 0.05% (or better) matching, which will provide at least 0.1% overall DC accuracy for input signals in the 100mV to 10V range.

The OPA606's fast settling time and large bandwidth preserve AC response: The output settles to 0.01% in 2.1μs for either a signal transition or a polarity-change command. For high gain, however, the PGA102's settling time (8μs) is the limiting factor in Figure 2's circuit. Similarly, because the OPA606's bandwidth is so wide (13MHz), it doesn't affect the bandwidth of the circuit, which is limited by the PGA102 to 250kHz at a gain of 100.

ADD AUTOMATIC GAIN CONTROL

To add automatic gain control (AGC) to the digital-gain-control functions of the PGA, you can use the circuit in Figure 3.[2] Unlike many implementations of automatic gain control, this circuit can accept a wide range (more than 1800:1) of signal amplitudes. In response to signal peaks detected by IC_{2B}, FET Q_1 provides basic gain control by varying the gain of inverting amplifier IC_{2A}. The peaks detected by IC_{2B} develop the FET's control voltage on holding capacitor C_1. A monitor circuit (equivalent to a 2-bit A/D converter that's accurate to at least 10%) senses that voltage in order to detect any need for a change in the PGA102's gain.

FET Q_1 serves as a voltage-controlled resistor, thereby providing the continuously variable portion of gain control. In conjunction with R_1 and R_2, the FET acts as the grounded leg of a tee network that reduces modulation of the FET's on-resistance and the consequent distortion. Further, feedback via R_5 and R_6 drives the FET's source to reduce overall distortion to 0.07%.

By controlling the variation of FET resistance, you control the tee network's range of equivalent resistance and, therefore, you control the range of gain for the basic AGC circuit. When the FET is turned off, IC_{2A}'s equivalent input resistor is 110kΩ, so IC_{2A}'s gain is −18.2. On the other hand, when the FET is fully on and has a drain-source resistance no greater than 1kΩ, this resistance is halved by the effect of feedback from R_5 and R_6, and the signal swing across the FET is doubled. Consequently, the tee network looks like a 2MΩ resistor, and the op amp's gain −1. The add-on output stage has a maximum gain range of 18.2:1 and the PGA's maximum gain range is 100:1, so the overall range is 1820:1.

ADJUST RESPONSE TIME

Voltage on C_1, the AGC holding capacitor, controls the FET and the PGA. That voltage is controlled, in turn, by feedback from IC_{2B}, which operates as a comparator. The comparator responds to the difference between the signal peaks and a reference level set by potentiometer

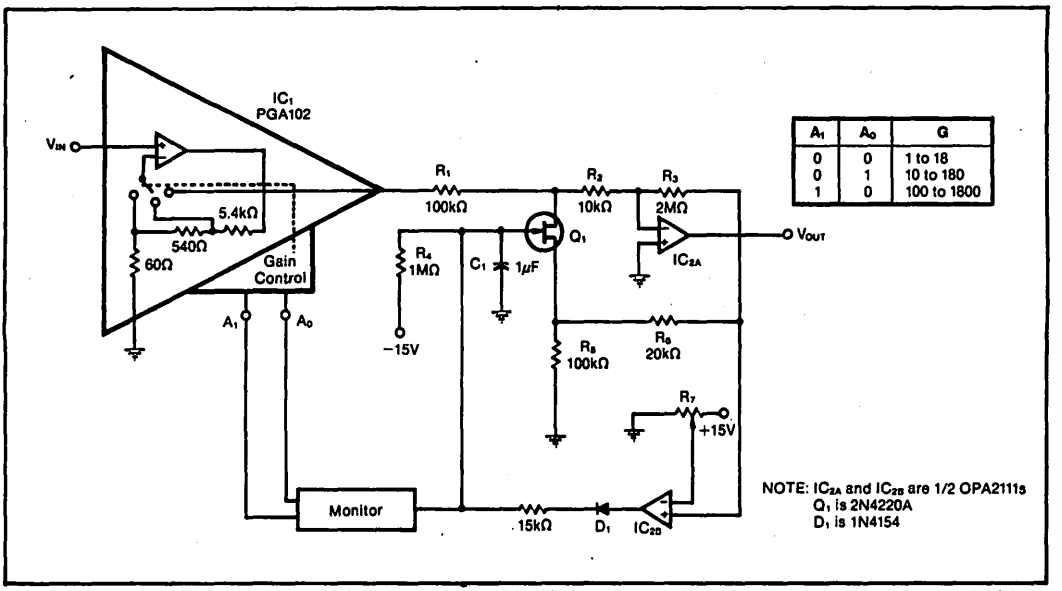


FIGURE 3. This automatic gain-control circuit maintains V_{OUT} at a set peak level for input signals having an 1800:1 dynamic range. The monitor circuit is equivalent to a 2-bit A/D converter that sets the PGA's prescale gain.

R_7. If that reference level is lower than the positive-going output peaks, the comparator output swings positive, applying forward bias to diode D_1 and increasing the voltage on C_1. The resulting drop in the FET's drain-source resistance shunts more signal current to ground.

R_8 and C_1 determine the response time for this action. If the output signal remains too low to trigger the comparator, the discharge of C_1 through R_4 will reduce the FET bias and the consequent signal-shunting effect until the increasing gain allows triggering to occur again. You should set C_1's voltage-decay rate low enough to prevent overshoot during gain changes. On the other hand, you should set the rate high enough for the circuit to respond to sudden drops in signal level, but not so high as to introduce distortion by allowing too much change in gain between signal peaks. The component values shown provide a 15ms response-time constant and a 1s decay-time constant, allowing the circuit to respond to frequencies as low as 10Hz.

FET Q_1 goes from pinch-off to full conduction as C_1 voltage ranges from −2.5V to 0V. An attempt by the circuit to adjust this voltage below −2.5V (beyond the point of complete shut-off) would indicate that the AGC can't provide gain, so the monitor circuit would increase the PGA102's gain. At the other extreme, a positive voltage on the capacitor indicates that the circuit can't shunt enough signal, so the monitor reduces the PGA102's gain.

Another way to provide digital control of current gain is to configure the PGA102 as a current amplifier.[3] You modify the feedback network by adding a sense resistor R_1 and a gain-setting resistor R_2 to the PGA102 (Figure 4a). This combination causes the amplifier and its feedback circuit to float on the load voltage. The input current (I_{IN}) develops a voltage on R_1 that drives the PGA input independently of signal current in the load resistor.

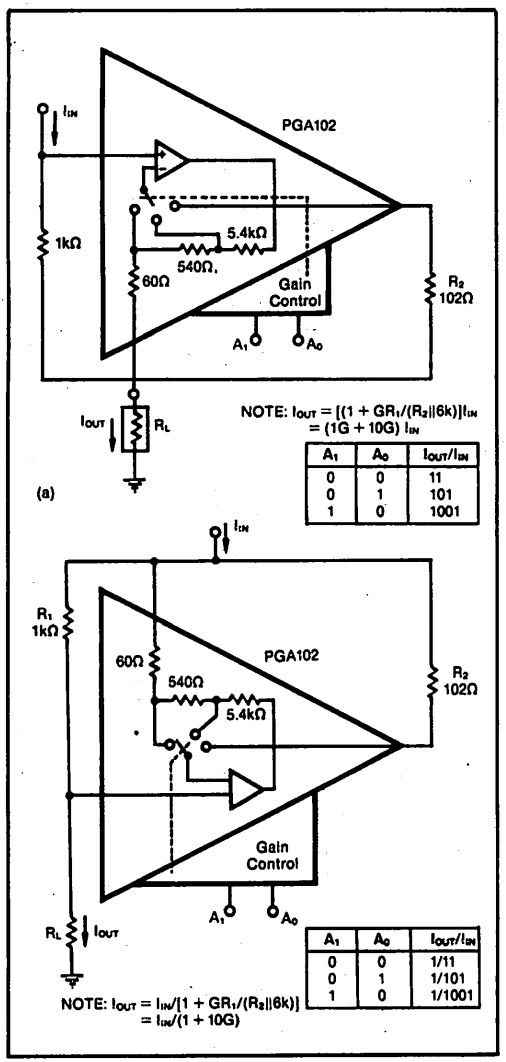
LOAD CURRENT HAS THREE SOURCES

The load current (I_{OUT}) is the sum of I_{IN}, the current from the PGA's internal feedback network, and the current from R_2 (an amplified replica of I_{IN}). The circuit's transfer function is a linear relationship between the input and output currents with a gain value that's established by the PGA102's gain setting. For resistor values shown in Figure 4a, the relationship is simply $I_{OUT} = (1 + 10G)I_{IN}$, where G is the PGA102's gain.

You choose the resistor values for R_1 and R_2 by making a compromise between the need for DC accuracy and several other (conflicting) requirements. For example, for the PGA to receive an input signal that's large compared to its input offset voltage, R_1 should be large. A large input signal, however, is inimical to output-voltage compliance, gain accuracy, and the avoidance of slew-rate limiting. Because the R_1 voltage floats between the signal source and load, this voltage reduces the range of output swing or compliance. Also, the PGA's output swing must, of course, remain within the constraints imposed by the power-supply and load voltages, and the output frequency must not exceed the value imposed by slew-rate limiting.

CHOOSE LOW-VALUE EXTERNAL RESISTORS

Because of the absolute tolerance of the PGA102's internal feedback resistors, you'd do well to choose low values for the external resistors. Although the internal ratios are closely trimmed for gain accuracy, their absolute values may vary ±2%. A small R_2 will minimize the



A1	A0	IOUT/IIN
0	0	11
0	1	101
1	0	1001

A1	A0	IOUT/IIN
0	0	1/11
0	1	1/101
1	0	1/1001

FIGURE 4. You can achieve digital control of current amplification (a) or attenuation (b) by connecting an external current-feedback network around the PGA.

effect of this variation. Further, because R_2 is in parallel with the total 6kΩ of feedback resistance, a small value for R_2 has little effect on the feedback network. You can omit R_2, however, as long as you can accept a 20% tolerance on the output voltage. If you omit R_2, load current will be limited to 1.5mA.

With the R_2 and R_2 values shown, the circuit in Figure 4a can accurately accommodate a 200:1 range of input current: The high end of this range is limited by the PGA102's 5mA output-current rating. The low end of the range is limited by the combined effect of its input bias currents and input offset voltage. Input bias current contributes no more than a 50nA error to the input current; the high-gain offset voltage (200μV) translates to as much as 200nA of error, based on the 1kΩ value shown for R_1. When you combine these errors, you can see that the circuit can handle input currents as low as 25μA with no more than 1% of offset error. Further, the voltage dropped across the selected resistors reduces the output-voltage compliance by only 0.5V.

CIRCUIT TRANSLATES IMPEDANCES

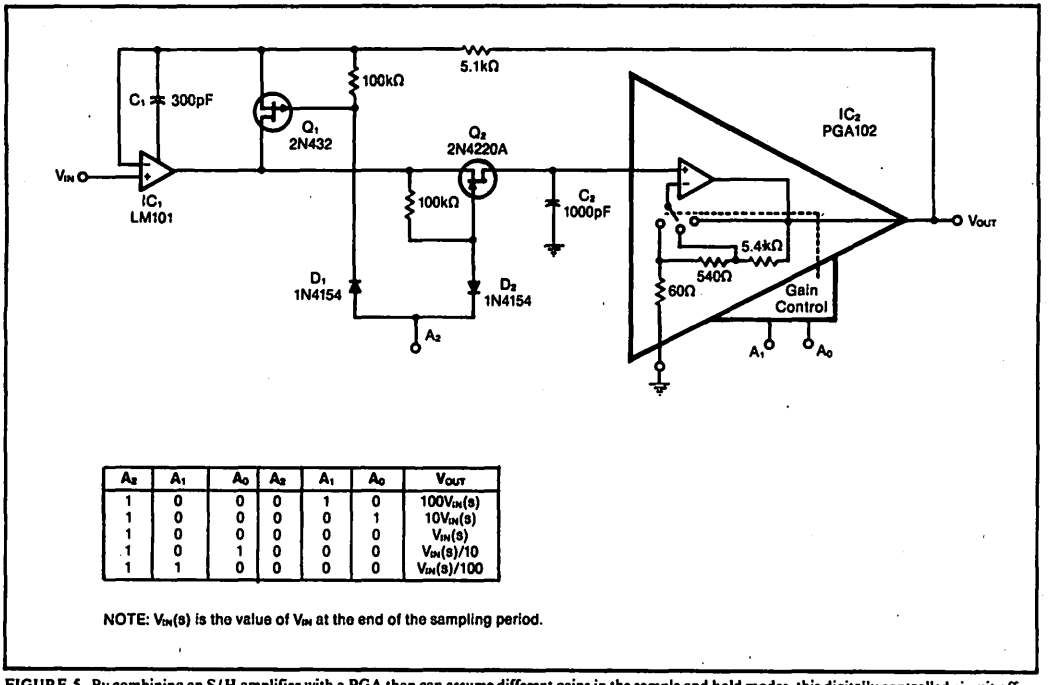
The low signal amplitude across the PGA also enables the PGA to realize its full 250kHz bandwidth without slew-rate limiting. In addition, the low resistance in R_2 minimizes the effect of tolerance variations in the PGA102's internal resistors, restricting gain error to 0.3%. The circuit's port impedances are analogous to those of a common-emitter transistor, in which source and load impedances reflect to load and source terminals (respectively) and are scaled in proportion to the current gain. In other words, the input impedance is the product of the load impedance and the current gain, and the output impedance is the result of dividing the source impedance by the current gain.

CONTROL CURRENT ATTENUTATION

The inverse of the current amplifier in Figure 4a is the current attenuator in Figure 4b. Because of bidirectional current-flow properties, the circuits for amplification and attenuation are similar. The input and output roles, however, are reversed so that the PGA absorbs part of the input current instead of supplementing it. The feedback operation of the attenuator is similar to that of the amplifier, except that all of the input current (I_{IN}) does not flow through R_1. Instead, current flow in that resistor causes feedback to initiate other current drains at the input. The transfer function is linear, and the PGA102's gain setting controls the output/input current scaling. however, the attenuator's gain is the reciprocal of the amplifier's gain; the output/input relationship is $I_{OUT} = I_{IN/(}+10G)$.

Errors and other performance characteristics for the attenuator are similar to those of the amplifier. The attenuator accepts input currents as high as 5mA, and the maximum output offset current is 250nA for the resistor values shown. The circuit's output compliance is reduced by only 0.5V, the PGA retains its full 250kHz bandwidth, and gain error caused by the PGA102 is no higher than 0.3%. The input impedance is the product of the load impedance and the attenuation factor, and the output impedance is the result of dividing the source impedance by that factor.

By combining the digital-gain-control function with an S/H or V/F function, you can realize simple circuits with few error-producing components. For example, you can build a gain-ranging S/H amplifier that has a 10,000:1 gain range (Figure 5). In the circuit, two amplifiers are connected either in a common feedback loop, to sample the signal, or via independent feedback connections, to hold the last signal sample.[4] Unless you require greater speed, you'll find this configuration useful for implementing both S/H amplification and signal amplification/attenuation.



A_2	A_1	A_0	A_2	A_1	A_0	V_{OUT}
1	0	0	0	1	0	$100V_{IN}(s)$
1	0	0	0	0	1	$10V_{IN}(s)$
1	0	0	0	0	0	$V_{IN}(s)$
1	0	1	0	0	0	$V_{IN}(s)/10$
1	1	0	0	0	0	$V_{IN}(s)/100$

NOTE: $V_{IN}(s)$ is the value of V_{IN} at the end of the sampling period.

FIGURE 5. By combining an S/H amplifier with a PGA than can assume different gains in the sample and hold modes, this digitally controlled circuit offers a gain range that is the square of the PGA's gain range.

Further, by using a PGA102 as the output amplifier, you can enable the circuit to sample at one gain level and then switch to another gain while in the hold mode. (Otherwise, the output amplifier would be a voltage follower that provides unity gain in both modes).

Digital input A_2 selects either the sample (high) or hold (low) mode of operation. When the circuit is in the sample mode, A_2 applies reverse bias to diode D_2, which allows Q_2 to turn on and complete a feedback loop common to the two amplifiers. The high level on A_2 also creates forward bias across D_1 and turns off Q_1; Figure 6a gives an equivalent circuit for this condition. In the equivalent circuit, Q_2 is represented by its on-resistance, R_{Q2}, which provies phase compensation in conjunction with C_2.

While this circuit is in the sample mode (IC_2 has unity gain), the common feedback forces V_{OUT} to track V_{IN}; C_2 charges to V_{IN} as well. C_2 also charges to V_{IN} when the PGA is set for unity gain. When the PGA is set for a higher gain, however, C_2 must charge to a lower voltage to satisfy the feedback constraints. By changing the PGA gain after the circuit switches to the hold mode, you can achieve either amplification or attenuation.

A transistion to low on A_2 turns Q_1 on and Q_2 off, thereby switching the circuit to the hold mode; the equivalent circuit for this condition is shown in Figure 6b. Switch Q_1's on-resistance shunts IC_1's feedback, preventing IC_1 from saturating and thus delaying overload recovery. Now, V_{OUT} depends only on the voltage stored on C_1 and the PGA's gain. The PGA does double

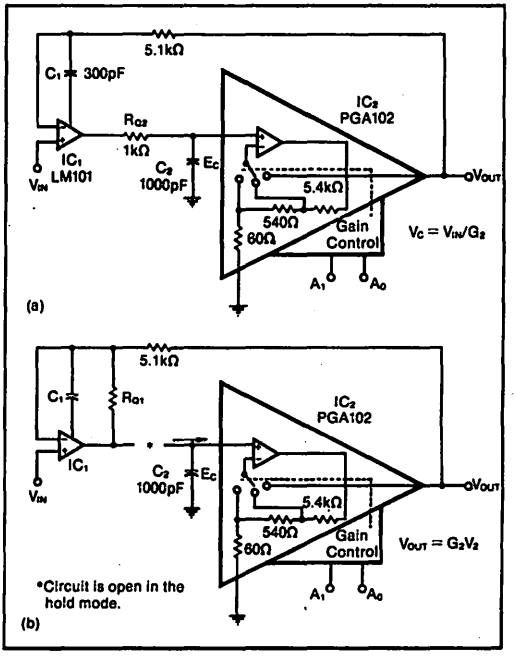


FIGURE 6. This circuit provides attenuation while it's in the ample mode (a) and amplification while it's in the hold mode (b).

duty, providing attenuation in the sample mode and amplification in the hold mode. Therefore, the S/H amplifier's net gain range is 10,000:1, which is the product of the ranges in each mode (or the square of the PGA's range). Using the table in Figure 5, you can calculate the net gain, which you can set from 0.01 to 100 in decade steps.

As you can see from Figure 5, the amplifiers' DC errors, the overall bandwidth, and the PGA's gain error all affect the S/H amplifier's accuracy, Further, the net error generally consists of a combination of different gain-error values from both the sample and hold modes of operation. IC_1 contributes almost no gain error because its high open-loop gain provides ample feedback correction within the circuit's bandwidth. The maximum gain error, therefore, equals the worst-case combination of two gain states for the PGA102, or 0.08%.

The DC performance of Figure 5's circuit is limited by the amplifiers' offset-voltage errors and the hold-mode voltage droop produced by IC_2's input bias current. (Droop, which occurs during the hold mode, is a slow discharge of the hold capacitor, C_1, caused by error currents. For the components shown, droop is no greater than $50\mu V/\mu s$.) Although the circuit's offset will change because of contributions from different gains, the net effect is less than 0.01% of full scale.

You can determine the bandwidth of this common-feedback type of S/H amplifier by using the Miller-effect phase-compensation technique. Although the common-feedback configuration lets you use the PGA's gain-ranging feature in both sample mode and hold mode, the configuration does entail multiple response limitation in the common loop. In the sample mode, for example, each amplifier contributes a pole, and the R_{Q1}-C_2 combination contributes a third pole. To be stable, the circuit must have a dominant-pole response for frequencies below the unity-gain crossover frequency. Capacitor C_1, connected to IC_1's phase-compensation terminal, provides this dominant-pole response. C_1 introduces a frequency rolloff that crosses unity gain at 150kHz, just where R_{Q2} and C_2 create a second pole. Furthermore, the 5.1kΩ feedback resistor introduces a zero in this region to cancel the C_1 pole and extend the single-pole response beyond 150kHz.

To preserve the stability-compensation scheme described above, you must use the Miller-effect phase-compensation scheme. Without the Miller-effect technique, switching the PGA gain would change the loop gain in Figure 6a, thus shifting the unity-gain crossover frequency and disturbing the loop's stability. The Miller effect of capacitor C_1, however, varies according to the amount of gain between its terminals. As a result, this changing phase compensation counteracts the destabilizing effect of gain-switching in the PGA, so the unity-gain crossover doesn't move; that is, the circuit's bandwidth remains fixed at 150kHz.

For lower-speed data-acquisition systems using a V/F converter for A/D conversion, you can peform gain ranging at the V/F converter instead of at the S/H amplifier. Charge-balancing V/F converters let you connect the PGA102 in a manner that produces differential inputs. For example, the VFC320 V/F converter lets you simply replace its gain-setting resistor with a PGA102 (Figure 7).

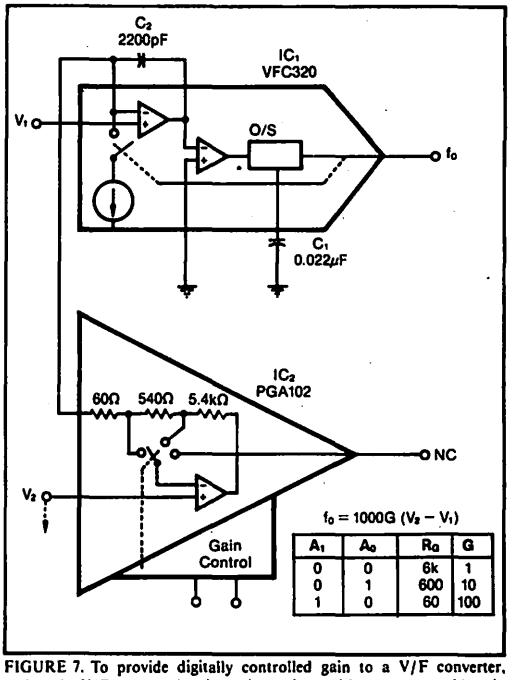


FIGURE 7. To provide digitally controlled gain to a V/F converter, replace the V/F converter's gain-setting resistor with a programmable gain amplifier.

The circuit in Figure 7 creates a virtual ground at the PGA's inverting input by grounding the V_2 terminal. The PGA then switches the virtual ground to various taps on its feedback network, thus supplying the V/F converter with gain-setting resistors of 60Ω, 600Ω, or 6kΩ. With these resistor values and the other component values shown, the V/F converter can offer a 4kHz full-scale-frequency response for inputs of 40mV, 400mV, and 4V.

By applying a signal to the V_2 terminal instead of grounding V_2, you can obtain a high-impedance differential input without adding an instrumentation amplifier. The differential signal $V_2 - V_1$ will then be impressed across the switchable gain-setting resistor, yielding a proportional output frequency f_O, which is equal to $1000G\ (V_2 - V_1)$, where G is the gain of the PGA102.

CIRCUIT HANDLES COMMON-MODE VOLTAGE

Common-mode signals shift the V/F converter's integrator output, but have little effect on current in the gain-setting resistor. Because integration over successive cycles of the V/F converter's operation reduces the effect of common-mode changes, little shift occurs in the average output frequency. Common-mode rejection is 60dB for the circuit shown. The VFC320's special-purpose integrator amplifier, however, limits the circuit's

common-mode voltage range (−10V to +1V).

Although the circuit in Figure 7 is simple, it has several limitations. First, the V/F converter's gain-setting resistors are confined to the values available from the PGA's feedback network. Further, those resistors have a 20% tolerance that appears directly as gain error, and you must adjust a capacitor value (C_1) to compensate for this error. What's more, the integrator amplifier's gain-bandwidth product at higher gain levels limits high-frequency operation. The integrator must produce a sharp triangle wave to avoid timing errors, but with increased integrator gain, less loop gain is available to preserve the triangle wave's integrity. As a result, the maximum full-scale frequency is 10kHz.

You can overcome the limitations of Figure 7's circuit by adding an op amp (IC_1 in Figure 8). The op amp buffers the normally grounded feedback return of the PGA102, so the PGA now drives an external V/F converter's gain-setting resistor. You can select that resistor value for the more conventional 10V FS inputs, and you can adjust the resistor value to remove gain errors. Because the gain-setting resitor is no longer switched, the integrator's feedback factor remains constant, so the V/F converter's gain-bandwidth requirement doesn't change. The PGA has a varying feedback factor, but it only has to process the low-frequency input signal. In short, you can set the circuit's full-scale frequency as high as 1MHz, which is the VFC320's upper limit.

Like the circuit in Figure 7, this circuit has high-impedance differential inputs. With its various gains, the PGA presents a prescaled signal to the V/F converter's gain-setting resistor (R); the common-mode signal characteristics remain the same as in Figure 7. The circuit's nonlinearity is 0.015%, and you can trim its input offset error to 0.5mV.

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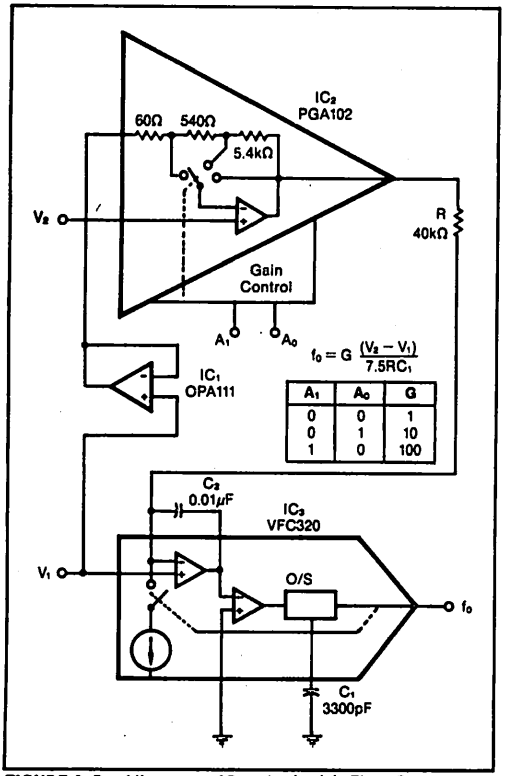

FIGURE 8 .By adding op amp IC_1 to the circuit in Figure 7, you create an instrumentation-amplifier input without affecting either the circuit's frequency range or its digital-gain-control capabilities.

DIGITAL GAIN CONTROL WINS OP AMP A NICHE IN MICROPROCESSOR SYSTEMS

A 2-bit input puts the first monolithic op amp with programmable gain under digital control for fast gain adjustments for many of the device's usual roles.

As digital control extends its influence, even analog circuits must fall in with its dictates. Gain control, in particular, is important in data acquisition systems. An associated microprocessor, if assigned that duty, will maintain the high-level signals that vastly expand a system's dynamic range.

Amplifiers have been available for some time in programmable versions that a supervisory system can instantly tailor to changing gain requirements. But in a gain-switching device, good DC characteristics conflict with the needs of speed. To date, hybrid op amps have traded speed away in favor of good DC input accuracy.

The first monolithic programmable-gain op amp, the PGA102, manages to preserve both virtues by separating them. It makes a ten-to-one speed improvement over hybrid devices, but then relegates DC input accuracy to one of the many instrumentation amplifier chips capable of meeting that requirement at low cost. In addition, the new device creditably performs numerous traditional op amp functions.

The monolithic realization of the PGA102 hinges on a new switching method. Amplifier gain has typically been controlled by switching resistors into and out of the feedback path. However, when switches are connected to that path, their on-resistance causes gain error and drift. Although the switches can be placed in an amplifier's input lead, where there is little current flow, even there on-resistance would introduce noise. Bipolar transistor switches are not the answer either, because of their inherent offset voltage in the on state. FETs, when designed for a low on-resistance, present prohibitively large die areas.

BORROWED TECHNIQUE

To avoid those problems, the gated-amplifier approach was borrowed from the pioneer analog computer days. The technique uses paralleled amplifiers that are switched on and off via a common signal path. If only one of the amplifiers is turned on, it supplies the only gain from input to output. Thus the feedback circuit connected to that amplifier determines the overall circuit's gain. Conserving hardware, the design needs just a switch to control the amplifier's internal biasing (Figure 1a). Only the input devices of a particular feedback channel need be enabled or disabled to connect feedback elements.

The control logic connects a biasing current source to one of the three differential pairs at any one time. Switching, or more aptly current steering, is a long-perfected trick used in digital-to-analog converters and is nicely handled by small bipolar transistors.

Basically a noninverting amplifier, the PGA102 can also be used in inverting, attenuator, or instrumentation applications. To adapt the chip to a particular job, its several control pins are configured to select the right combination of gain and performance (Figure 1b). For example, one 2-bit digital code applied to the gain-control inputs selects A_1, an amplifier with a short-circuited feedback path. Because of its unity gain, the amplifer can serve as a voltage follower. Amplifer A_2 can be selected for its gain of 10 and, if required A_3 will

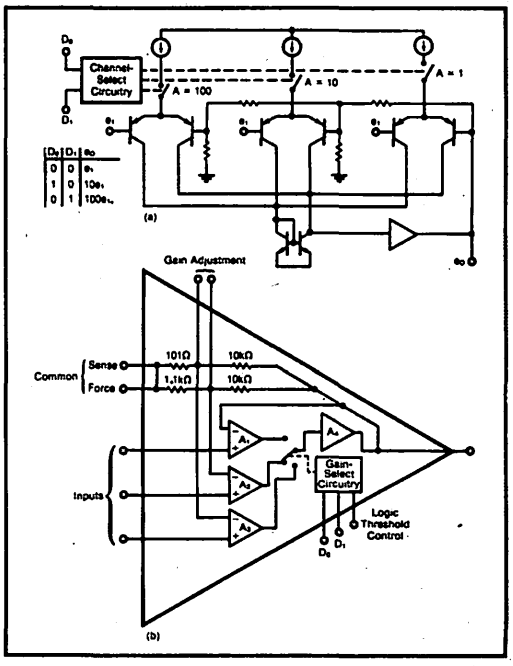

FIGURE 1. Current switching and a simplified gated-amplifier design give the PGA102 op amp its programmable gain feature (a). Control signals select one of three input stages to activate a feedback path and to set gain (b).

give its user a gain of 100. Although they would generally be connected to the same signal source, each of the amplifiers can be fed with separate inputs for multiplexing applications.

Other connections on the chip provide similar ways of modifying performance. Thus the Force and Sense pins can be used to remove the gain error and drift that might otherwise be introduced by wirebound resistance in the common feedback path. And because connections to the internal gain-adjustment resistors are brought out to external pins, trimming resistors can be added in parallel to fine tune the gain.

Even the gain select pins can be customized by applying the correct voltage to the Logic-Threshold Control pin (LTC). The gain select pins switch at 1.4V above the voltage applied to the LTC pin. (For TTL control, LTC would be grounded.)

ACQUIRING DATA

A data acquisition system is a typical application for the programmable op amp (Figure 2). There, an instrumentation-amplifier preamp, with a gain set somewhere between 10 and 100, provides initial high-precision gain. Then the op amp adds further gain as dictated by control feedback from a microprocessor.

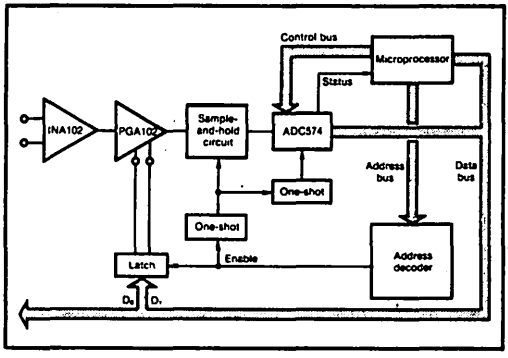

FIGURE 2. In a data acquisition system, a monolithic instrumentation amplifier ensures the required DC input precision while the programmable gain amplifier supplies the high-level signals needed by the sample-and-hold circuit and the analog-to-digital converter.

Because it can be readily scaled, the signal fed to the succeeding states—in this case, a sample-and-hold device and an analog-to-digital converter—can be kept at a consistently high level. Doing so reduces the effects of input error on those devices and makes their speed as attractive as their accuracy. It also effectively expands the dynamic range of the entire system by more than six bits (e.g., a 12-bit system can be boosted to 18-bit performance).

The analog-to-digital converter has a three-state buffer output to connect directly to the bus. It also has control inputs and a status output, the latter to signal the end of a conversion. The microprocessor checks the converter's output signal level against range limits. If it falls outside that range, a new gain-control code is sent along the data bus to the inputs of a 2-bit-wide latch—the 74LS74 D-type flip-flop in the example.

The address bus also carries a signal that serves as both a latch enable and a trigger for a one-shot that causes the sample-and-hold device to sample until it and the programmable-gain op amp have settled. At the end of the delay, the first one-shot triggers a second one that holds the converter's buffer in the acquisition mode for a required settling time. In that manner, the net input gain is set before every measurement, ensuring consistently high signal levels.

If its input and common connections are reversed, the op amp can serve as an inverting amplifier. The input signal is applied to the feedback networks instead of to the noninverting inputs. In this mode only two channels are available, since one will have no feedback return to common. The two channels achieve gains of 9 and 99, but for convenience they can be adjusted to 10 and 100 by means of the gain-adjustment pins.

A programmable attenuator is formed simply by using the PGA102 in the feedback path of another op amp (Figure 3). There it amplifies the other op amp's output so that a smaller signal will be needed to satisfy feedback requirements. When the programmable op amp's gain is increased, the main device's output drops in direct proportion. Since the basic connection is for an inverting op amp, the output will be a negative replica of the input, scaled according to the PGA102's truth table.

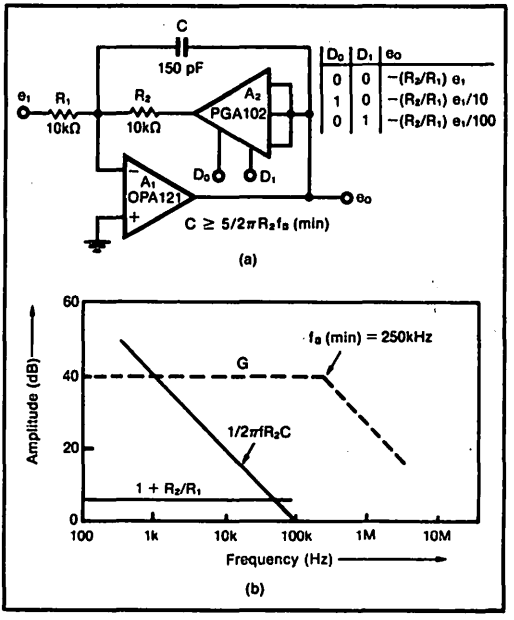

FIGURE 3. A programmable attenuator is created simply by placing the chip in another op amp's feedback path (a). Frequency stability is maintained through the use of feedback bypassing, which reduces feedback gain to unity before the bandwidth limitations of the PGA102 are reached (b).

The choice of external feedback resistors determines circuit operation, according to the formula:

$$e_O = -(R_2/R_1)(e_I/G)$$

where G is the operating gain of the PGA102. To retain

accuracy, the ratio of R_2 to R_1, plus their temperature coefficients, must be tightly controlled. Also, the circuit's output is limited by that of the programmable op amp. Because the PGA102's output is amplified to a greater level than that of e_o, the latter will be limited to $e_o \leq 10\ V/G_2$ for 15V supplies.

The resistor values shown produce attenuation factors of −1, −0.1, and −0.01. Different scaling produces other attenuations. For example, if $R_2 = 10R_1$, the net circuit gains would be −10, −1, and −0.1. In that case, the circuit would amplify for one digital control code, be neutral for another, and attenuate for the last.

ATTENUATING CIRCUMSTANCES

An op amp of this type calls for other considerations in addition to resistor values. Because there are two amplifiers in the feedback loop, extra phase compensation is needed. Without it, the circuit would be plagued by additive phase delays of sufficient amplitude to cause oscillation. A dominant pole must be developed in the feedback loop with the aid of a capacitor, C. That part bypasses the programmable op amp at high frequencies, reducing the feedback around the other op amp to the level of an integrator. As long as the frequency response plot of the integrator intercepts a line—prescribed by $1 + R_2/R_1$—at a point well below the PGA102's roll-off, the circuit will function well. Because the PGA102's minimum bandwidth, or f_B min, is 250kHz for a gain of 100, values of 10kΩ for resistor R_2 and 150pF for capacitor C will meet the stability requirement at one-fifth the roll-off point. The resulting attenuator bandwidth will be 50kHz.

Gain and DC errors also delimit attenuator operation. The gain errors that result from the ratio of R_2/R_1 and the PGA102 itself appear at the output, as does the input offset voltage of the programmable device; that of op amp A_1, however, will be first divided by the PGA102's gain.

Other types of circuits can take advantage of the one-chip op amp's programmability. A voltage or current source fitted with the op amp, for example, gives the user digital control of those values. That can be especially handy in an automated test system.

When the op amp is used in an instrumentation amplifier, it lends the circuit a tenfold improvement in settling time and slew rate over prepackaged programmable amplifiers. In a conventional three-chip circuit, the settling time is as low as 3μs to 0.01% and the slew rate is 9V/μs (Figure 4). The bandwidth is determined by the PGA102 because it is the only device connected for high gain. However, it will be no less than 250kHz.

In the circuit, the PGA102 serves as a noninverting amplifier, A_1. Another noninverting amplifer, A_2, helps develop an appropriate signal for differential amplifier A_3 and also affords a measure of common-mode rejection. A_2 is connected as a voltage follower to sense and drive the common point of the PGA102, bootstrapping it to remove common-mode signals from the feedback path.

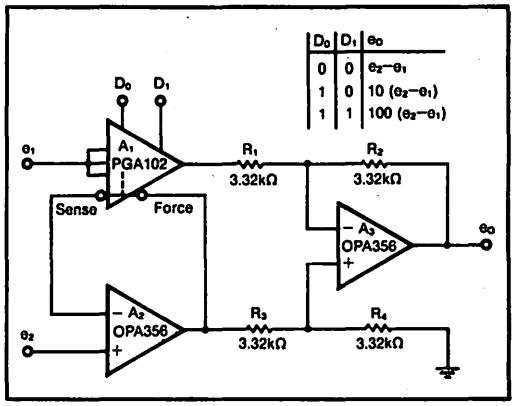

FIGURE 4. A three-chip instrumentation amplifier uses the PGA102 as a programmable element on one side of the differential input.

The user controls the circuit by adjusting the gain of the difference signal between the inputs of the PGA102 and the voltage follower. To optimize the circuit in other ways, the resistance ratios of the two resistor pairs can be accurately trimmed to improve gain accuracy and common-mode rejection. The latter will be no more than twice the reciprocal of the ratio mismatch. For example, if the mismatch is 0.1%, the CMRR will be 2000 or less, or about 66dB.

MATCHMAKING REQUIRES ADJUSTMENTS

For a very finely adjusted match, at least two of the resistors should be paralleled by trimming resistors. Initial adjustment should minimize the gain error; subsequent adjustment is aimed at improving the CMRR. Such tweaking can bring the gain error to as little as 0.05% and the CMRR to as much as 90dB. Of course, to retain the performance over time, the resistors must have a very-low temperature coefficient. The feedback path of the voltage follower is connected through the Force and Sense pins of the PGA102, establishing, in effect, a Kelvin sense. In addition to preserving gain accuracy, that connection avoids gain error due to signal drop in the internal wire bonds of the feedback common return path. By sensing at the internal common point, associated error is removed from the input circuit and transferred to the output without gain. The connection prevents the wire bond alone from introducing a gain error of as much as 0.2% at a gain of 100. Although the initial error would be removed by careful gain adjustment, a significant thermal drift error would have been created because of the 4000ppm/°C temperature coefficient of the wirebond resistance.

The force and sense error reduction technique can be applied to most other applications of the monolithic op amp. The input shown connected to the voltage follower is then simply grounded.

Two other parameters benefit from adjustment: input and output offsets. Because this example uses OPA356 op amps for their speed, both offsets are larger than

usually desired. The input offset should be adjusted first, at the highest gain level, using the offset trim adjustment of A_2. Then, at minimum gain, A_3's offsets can be reduced to less than 100μV.

Although most of the adjustments can be avoided with a pretrimmed difference amplifier, that solution sacrifices the speed advantages of the OPA356. Gain scaling is also a factor that encourages building, rather than buying, a difference amplifier. Thus while the PGA102 sets the circuit at gains of 1, 10, and 100, changing the gain of the difference amplifier affects the overall circuit gain. A pretrimmed difference amplifier does not allow that flexibility.

BUILDING BRIDGES

The output signal of a bridge is proportional to the current flowing in any of the legs. The current, in turn, is directly related to the bridge's bias voltage. For that reason, a highly accurate and stable bias supply is necessary, or alternatively, periodic corrections must be made under software control.

The multiplexing capability of the PGA102 comes in handy for a dual assignment: monitoring the bridge's output and periodically checking the bias level for calibration purposes. In a representative circuit, the op amp serves as a programmable-gain block to boost the output of an instrumentation amplifier (Figure 5). The unity-gain input of the op amp is connected directly to the bridge bias supply instead of to the instrumentation amplifier.

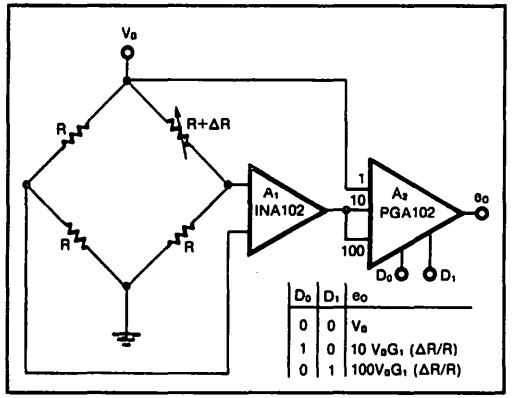

FIGURE 5. Independent gain channel inputs multiplex between bridge-output monitoring and bias measurement.

When the unity-gain channel is deactivated, signal eo on the output line of the op amp is the amplified bridge output. When the unity-gain channel is active, the level of bridge biasing is transmitted instead. The bias can be either DC or AC, depending on the subsequent signal processing. A DC signal can be applied directly to an analog-to-digital converter. AC biasing would require the addition of an AC/DC converter. Or, a sample-and-hold circuit in a data acquisition system could be used to acquire the signal envelope.

The bridge bias can be calibrated in software to within 0.006%; the measurement will be affected by both the gain error and offset voltage of the op amp. The gain error of the unity-gain bias-monitoring channel will bottom out at 0.003%—or more precise calibration than the bridge output measurement channels would provide. The input offset voltage is higher on the monitoring channel, but its contribution to total error, in view of the high level of bridge bias, is not significant. Lower offsets are introduced in the bridge output sensing channels, where much lower signals are measured. Once again, the relative error in the calibration channel is much smaller.

Although it might be considered a nuisance, the bridge's sensitivity to biasing voltage can actually be put to good use. Instead of switching amplifier gain, the apparent gain of the bridge can be changed by simply switching the level of bridge bias. Since the bridge's output is directly proportional to the bias, the net circuit response would be correspondingly scaled.

A programmable attenuator circuit (Figure 6) illustrates how the PGA102 can affect bridge biasing. The circuit is equipped with a transistor to boost the current over the bridge. For precise, consistent bias voltages, the REF10 voltage reference is added as well. It sets the scaling standard by virtue of its 0.05% initial accuracy and 1ppm/°C drift. That precision is met with compatible performance from the op amp, but the other components must be carefully selected to ensure a high level of accuracy for the entire circuit.

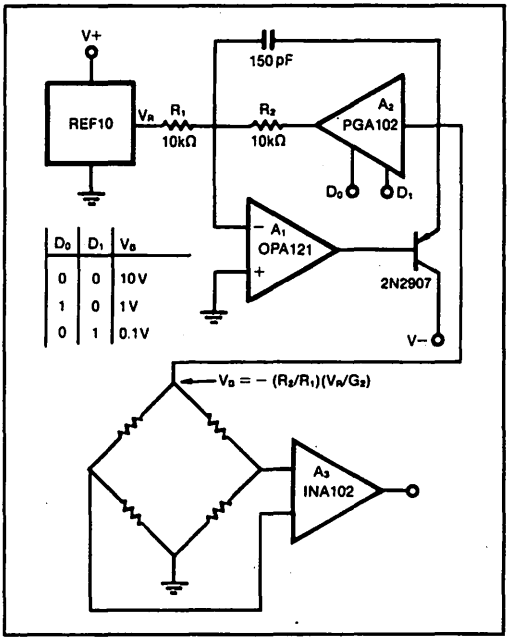

FIGURE 6. Rather than boosting a bridge's output, the programmable-gain amplifier controls bridge biasing and, in effect, the output gain range.

Because switchable gain is not needed in this circuit, the output amplifier can be an economical monolithic device, such as the INA102 or a similar type. The REF10, which develops a DC bridge bias, can also be

replaced by an AC reference if current-boosting at the op amp output is made bipolar.

A decided advantage of controlling the bias voltage, rather than switching output gain levels, is the opportunity to avoid thermal drift of bridge elements caused by self-heating. High bridge currents, although desirable for greatest bridge sensitivity, result in higher internal power dissipation and therefore heat. In fact, the problem can be so severe that it is necessary in some circuits to turn off the bridge bias except when a measurement is actually being made. That incurs a delay problem: The circuit must then settle to the degree necessary to ensure circuit accuracy.

The circuit shown obviates the need for large biasing currents, facilitating routine alarm checks against excessive output from the bridge circuit. Because little heat is generated, the bridge can remain on, available for interrogation by a microprocessor system. Such a feature is especially important in an industrial system that requires frequent safety or process-control monitoring of a measurement bridge circuit.

CIRCUIT APPLICATIONS FOR A 12-BIT ECL DAC

There are several reasons why a D/A converter using emitter-coupled logic, such as the DAC63, will have superior performance as compared to a T^2L DAC. Briefly, ECL has lower logic delay than T^2L, is less noisy, and the data registers have low data skew. In addition, the circuit structure of ECL naturally lends itself to cleanly driving lines free of reflections and over-shoot. This Application Note will show how these desirable properties can benefit the user in a particular application.

ECL VERSUS T^2L

When the clock rate is greater than 10MHz, it becomes difficult to isolate digitally generated noise from the analog circuits and ECL circuitry starts to have advantages. This section will focus on comparing ECL vs T^2L with respect to data skew, ground currents, line driving and receiving capability. In particular, the impact as to how these characteristics affect the generation of analog waveforms will be shown.

DATA SKEW AND GLITCH

Data skew occurs when all the digital inputs do not change at exactly the same time and is defined as the difference between Tpd(+) and Tpd(-). Tpd(+) is the positive going propagation delay while Tpd(-) is its negative counterpart. As an example of the phenomenon, consider the major carry change to a 12-bit DAC. For a 1LSB change around the MSB, the code would change from 0111 1111 1111 to 1000 0000 0000 under ideal conditions. With the presence of data skew all bits might not change at the same time and an intermediate code could exist. As an example of this phenomenon, consider what would happen if the MSB changed more rapidly compared to the rest of the bits, so that the code transition pattern would be

011111111111	111111111111	100000000000
Code before change	Intermediate code	Code after change

See Figure 1 for a timing diagram showing data skew.

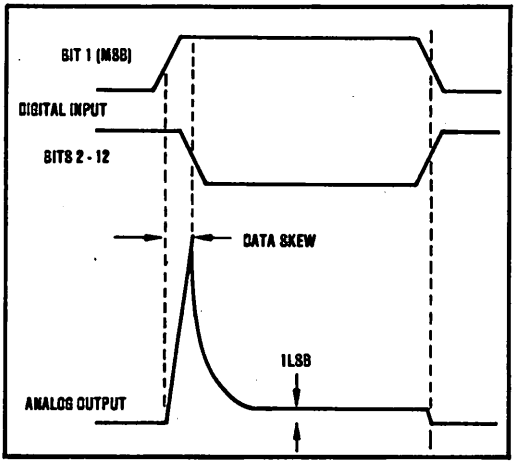

FIGURE 1. Response of Digital-to-Analog Converter in Presence of Digital Data Skew.

Therefore, for a period of time equal to the data skew, the D/A converter output would start to head in the direction of an output that was considerably different than a 1LSB change from the previous code. The phenomenon that is created by data skew is often referred to as a D/A output glitch. A convenient way to specify the glitch is by measuring the area of the glitch in units of LSB-nsec. Some manufacturers specify the glitch in units of mV-nsec or mA-nsec but for purposes of comparing one D/A to another using the units of LSB-nsec is the preferred way.

Tpd(+) and Tpd(-) tend to match within 0.2nsec for ECL as compared to about 2nsec for T^2L. Therefore, due to this characteristic, data skew will be reduced by an order of magnitude.

Applications such as displays and precise amplitude or phase synthesis required in digital TV are adversely affected if the glitch is too large. For these situations ECL will yield performance superior to that of T^2L.

Glitch performance of 250LSB-nsec is obtainable with 12-bit ECL DAC's without the need for deglitchers. See Figure 2 for a test circuit that displays the glitch characteristic.

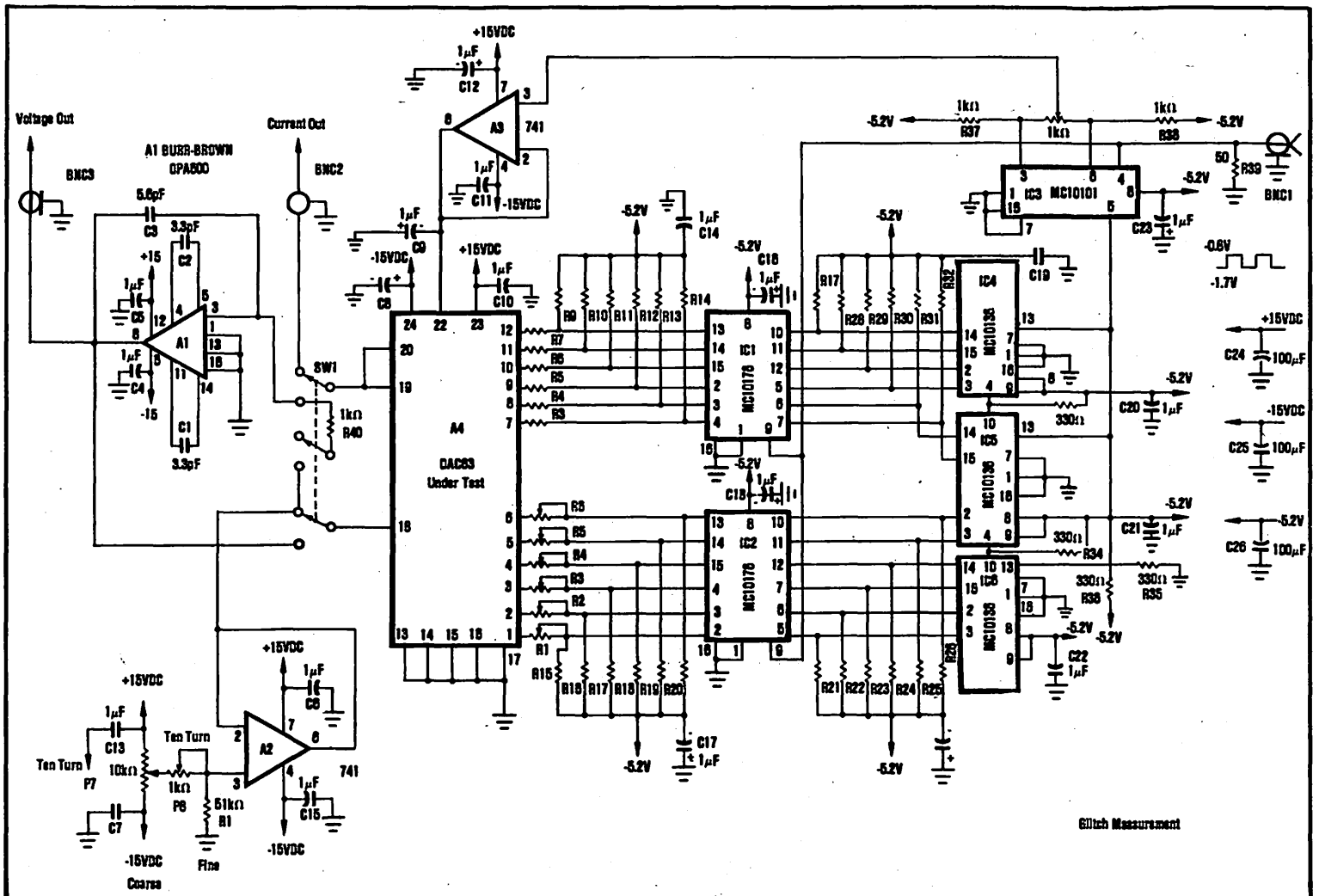

FIGURE 2. Circuit Using the DAC63 to Generate a Staircase Waveform which can be Examined to Evaluate the Glitch Performance.

The circuit in Figure 2 uses the DAC63 to generate a staircase waveform which can be examined to evaluate the glitch performance. Digital data is generated by a counter comprised of IC4, IC5 and IC6. IC1 and IC2 are data registers that are strobed at the proper time to enter low skew data into the DAC. Variable resistors R1 through R6 have the function of adjusting the data delay to reduce the glitch size. IC6 buffers the clock input and generates the proper logic threshold voltage for the DAC. Op amp A1 can be used to increase the output voltage if necessary.

When the clock increments the counter a staircase-like waveform will be observed at the output of the DAC. Within the DAC63 there is a 1k resistor that is driven from the output of A2 so a current, which is the negative of the current of interest, is created. The coarse and fine adjustments are used for convenience when viewing the output on an oscilliscope. See Figure 3, which shows an oscilliscope picture of the staircase output of the DAC.

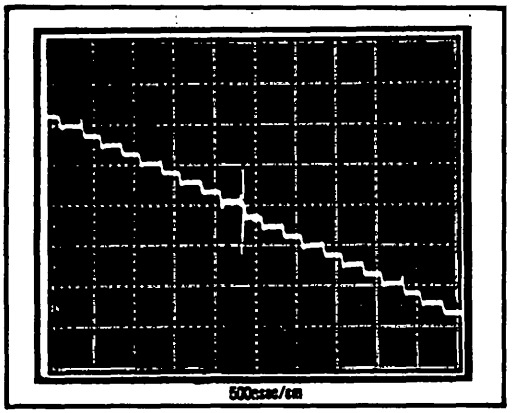

FIGURE 3. Staircase Output of DAC.

The area of the glitch can be minimized in the following manner: variable resistors R1 through R6 in association with the input capacitance of the DAC form an adjustable delay from 0 to 500psec; resistors R7 through R12 are set at 240Ω which is about the midpoint of the 500Ω variable resistor.

Starting with the major carry transition around the sixth bit, R6 would be adjusted for minimum glitch. In a similar manner successively higher order bits can be adjusted until the entire converter is trimmed. If the adjustment is made in this manner, the interaction between trims will be held to a minimum. As previously explained, adjusting the coarse and fine resistors will allow examination of the bit transition in question. Figure 4 illustrates the type of performance that is obtainable after the delays are adjusted.

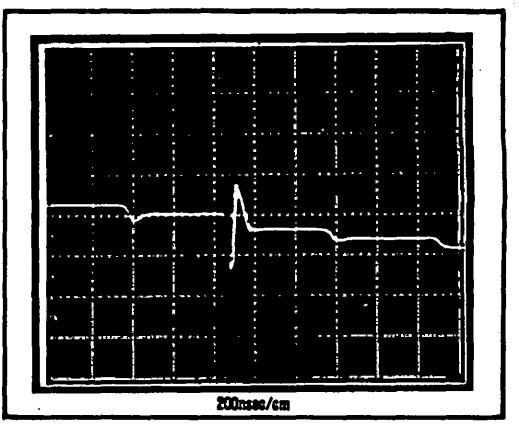

FIGURE 4. Detailed Picture of Glitch.

Considering the simplicity of a DAC with low glitch as compared to a DAC with a deglitcher, the ECL DAC is an attractive alternative to consider. Another reason why an ECL system is superior is that the rise and fall time of ECL is the same since the logic elements are non-saturating. Schottky clamped logic is also nonsaturating but the mechanism that causes the negative and positive propagation delays are different.

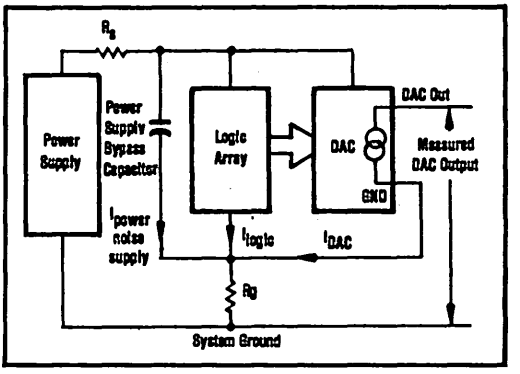

FIGURE 5. Ground Loop Interference Between DAC, Logic and Power Supply.

NOISE

Emitter coupled logic tends to have constant power supply drain and consequently ground loops or ground induced noise are minimized. In a practical system it is often very difficult to isolate digital and analog grounds; therefore, the constant power supply feature of ECL becomes very important. Refer to Figure 5 for a diagram depicting a ground loop that could exist between the digital logic and a digital-to-analog converter. As seen in Figure 5, the voltage drop in Rg can be a source of interference as it is in effect in series with the analog output. The advantage of ECL in this situation is that I_{logic} tends to be constant and $I_{power\ supply\ noise}$ is lower, thereby resulting in a less noisy analog output.

Another source of interference is when some part of the digital signal capacitively couples into the analog output. As with ground induced noise, in a practical layout, it is often difficult to prevent this from happening. Here again, ECL performance is superior to T^2L.

LINE DRIVING CAPABILITY

One clear advantage of ECL, compared to T^2L, is the ability to drive lines. The ECL circuit structure naturally lends itself to driving lines as a typical ECL gate has a low output impedance and a high input impedance. A high speed DAC, such as the DAC63, is capable of settling to ±1/2LSB of accuracy in 35nsec for full scale changes. To achieve this type of settling, it is important that the signal driving the DAC be clean, which means free of overshoot and reflections. If one of the digital lines driving the DAC is improperly terminated, the ringing effect is liable to recross the logic threshold which would have the effect of changing the state of the DAC (see Figure 6). ECL drive tends to be free of this effect once the input lines are either extremely short or are terminated. If a proper pull-down resistor is used with ECL, the line can be terminated in its characteristic impedance thereby eliminating ringing effects caused by reflections on the line.

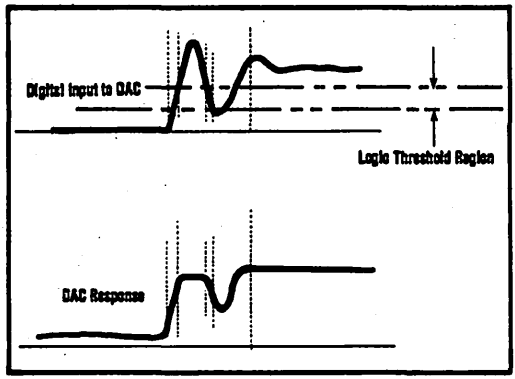

FIGURE 6. Noisy DAC Output Caused By Ringing of Digital Inputs.

APPLICATIONS OF A HIGH SPEED DAC RECEIVING DATA TRANSMITTED FROM A REMOTE LOCATION

Any time a requirement dictates that digital data be transmitted with the use of cable, especially at high speeds, line drivers and receivers are needed to preserve the bandwidth or data rate. A complex display system is an example of a situation where this might arise. All circuitry needed to generate the display cannot be located in the same area because of the quantity of all the digital processing involved. It is also important to locate the CRT drive circuits as close to the CRT as possible to obtain a clean display. Consequently, it is not hard to imagine that the digital input to the DAC could be located several feet away from the DAC. Large, high resolution displays require both high resolution and high speed to achieve these goals. The technique chosen to transmit high speed data, both analog and digital, will determine the success of such systems. A good way to determine if it is necessary to use terminated coaxial cable is when the rise time or pulse width that is necessary to be maintained is low compared with the delay between the sending and receiving circuits.

Figure 7 shows a block diagram of a system that is capable of preserving a high data rate from a remote location and generate a clean analog signal. It should be noted that even when the entire digital process is T^2L oriented, an ECL DAC provides an economical solution to this type of processing problem.

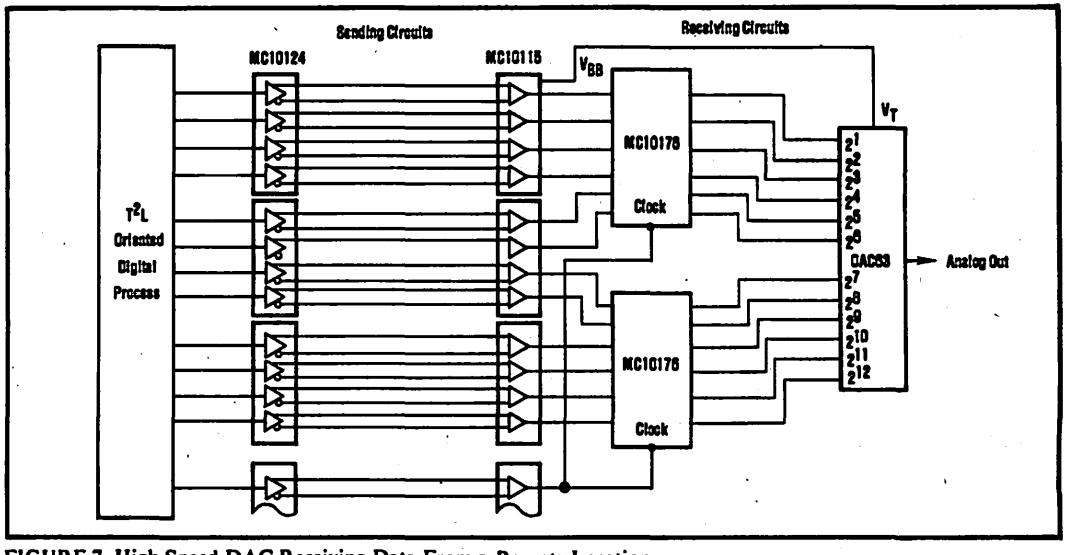

FIGURE 7. High Speed DAC Receiving Data From a Remote Location.

Prior to sending the digital data down the line, the data is converted to an ECL format by the use of the MC10124 which is a quad-differential T^2L to ECL translator. Transmitting the data differentially, as shown in Figure 7, maintains the correct logic threshold in spite of cable losses and temperature differences between the sender and the receiver. The data is received by the use of the MC10115 which is a quad-differential line receiver. At this point, the data is resynchronized with the MC10176, a hex data register. As previously pointed out, data skew can create a noisy analog signal which the data register can substantially reduce.

PRECISE AMPLITUDE AND PHASE SYNTHESIS OF AN ANALOG WAVEFORM

Another use of a high speed digital-to-analog converter, such as the DAC63, occurs when the application calls for precise generation of amplitude and phase for an analog waveform. While there are many ways to accomplish this with lower frequency circuitry, the use of a high speed DAC is an attractive alternative. A high frequency DAC, such as the DAC63, is capable in the small signal mode of being updated at a 50MHz rate which will substantially ease the subsequent analog filtering requirements.

Figure 8 shows an arbitrary analog waveform that needs to be synthesized. If the waveform were sampled at periodic intervals, the synthesized waveform would result. This synthesize procedure would consist of mathematically computing the closest 12-bit approximation at each sample point which would be used to generate the encoding table for the ROM. Refer to Figure 9 which shows a block diagram of an actual system that will generate a high speed synthesized waveform.

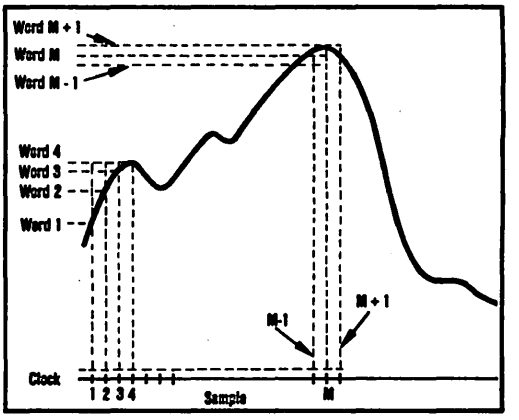

FIGURE 8. Arbitrary Waveform To Be Synthesized.

The sample points would correspond to the ROM address while the ROM output would be the associated code at each one of these addresses. The block diagram shown in Figure 9 has the capability to create a waveform with 256 sample points and can generate a waveform with an effective sampling rate from 25 to 50MHz. The block diagram shown in Figure 9 is attractive because of the simplicity with which it can be designed. Another approach could be to use bit slick hardware which is microprogrammed.

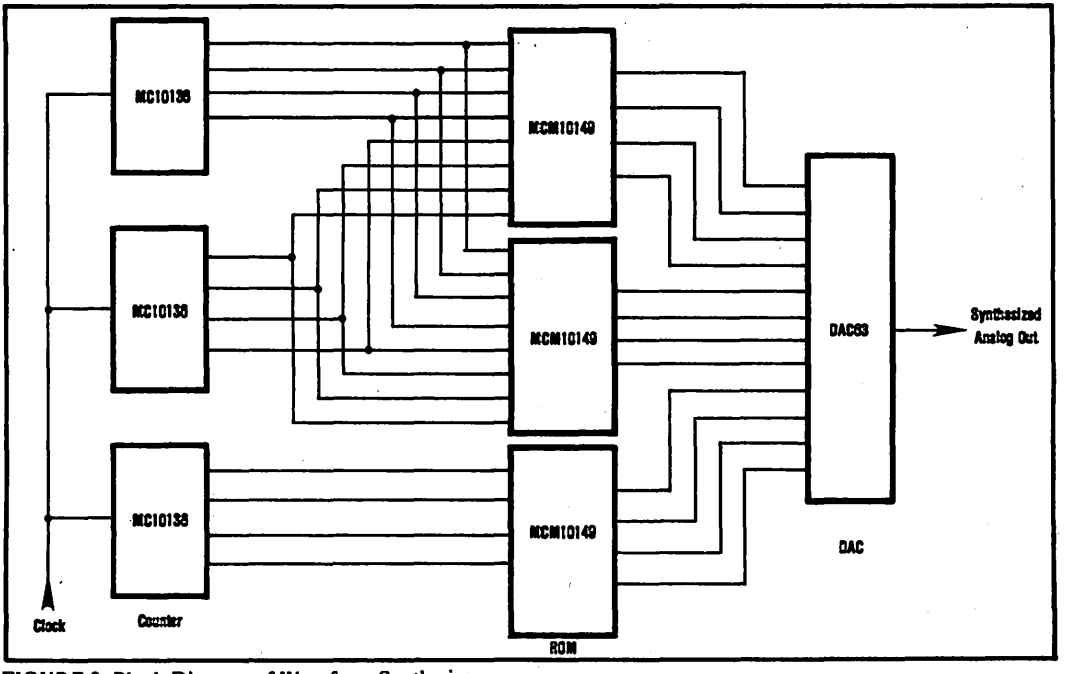

FIGURE 9. Block Diagram of Waveform Synthesizer.

12-BIT 250nsec ANALOG-TO-DIGITAL CONVERTER

See Figure 10 for a block diagram of a 250nsec, 12-bit analog-to-digital converter. This converter can be implemented at a cost in the neighborhood of $800. When a designer is faced with a "make or buy" decision, this would represent another way to go.

The block diagram works in the following way. At the beginning of the conversion interval, flash encoder 1 samples the input but can only resolve the signal to 6 bits.

The first 6-bit approximation is then converted back to analog form with the DAC and subtracted from the original analog input. It is very important that the digital-to-analog converter have 12-bit accuracy and precise settling time as it will not be possible for the A/D converter to achieve 12-bit performance o'..erwise.

After the 6 bit approximation is converted back to analog form, it is subtracted from the input signal and amplified. The output of the subtracting amplifier then drives flash encoders 2, 3 and 4. The function of flash encoder 3 is to provide the fine resolution that flash encoder 1 was not able to achieve. Flash encoders 2 and 4 serve the purpose of handling the over or under flow that could be generated as a result of the subtraction that was previously mentioned. The over and under flow result from the fact that flash encoder 1 will not have 12-bit accuracy and the residue signal that appears at the output of the amplifier will be the sum of the offset and gain error of flash encoder 1 in addition to the quantizing error. The output of all the flash encoders are then fed into a two's complement adder so that final 12-bit word can be created.

If the gain of the amplifier is set high enough, the block diagram just described is not sensitive to any of the offset and gain errors associated with the flash encoder.

It should be noted that since most flash encoders have ECL outputs, having a fast settling ECL DAC provides a natural interface in this application. The analog-to-digital converter shown in Figure 10 is a very effective architecture because the only component that needs 12-bit accuracy is the DAC. Errors of the Flash Encoders will have a negligible effect.

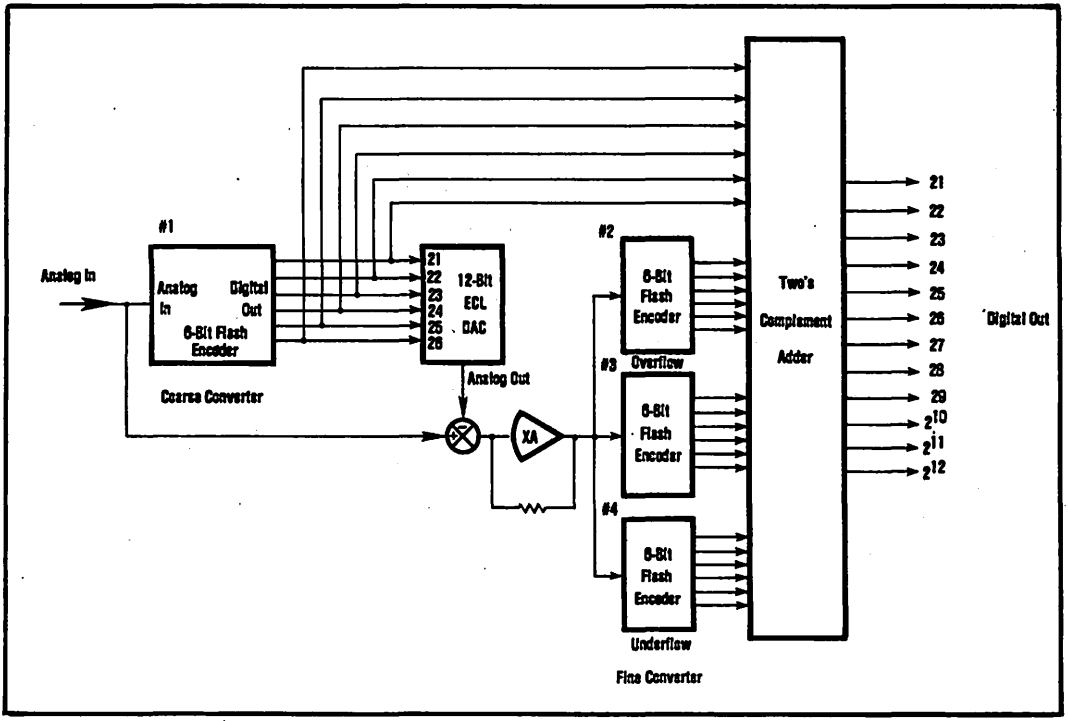

FIGURE 10. Block Diagram of 250nsec Analog-to- Digital Converter.

A HIGH SPEED PEAK DETECTOR

The circuit shown in Figure 1 will capture and hold the peak value of fast-changing analog signals.

The occurrence of a peak is detected by the diode-clamped differentiator circuit, which is built around an OPA600 op amp. When the input voltage reaches a peak and begins to decrease, the current in capacitor C1 reverses, causing the op amp to switch rapidly from its negative to its positive output state. Comparator 2 detects this change and switches the SHC804 into the "HOLD" mode, freezing the peak value. At the same instant, the PEAK DETECT signal goes low, which can be used to initiate a reading of the peak value by an A/D converter (such as the model ADC803).

In many applications, it is desirable to establish a threshold level such that the peak detector operates only for signals above a preset limit. This prevents false triggering on low level noise peaks. In order to accomplish this, comparator 1 is used to keep the SHC804 in the "SAMPLE" (track) mode as long as the input is below the threshold (see Figure 2). This level is set by the 5kΩ potentiometer.

If the RESET function is used, it should normally be held low. This causes the circuit to latch in the "HOLD" mode on the first peak. Bringing RESET high momentarily will return the SHC804 to the track mode, ready for the next peak. If the reset function is not used (RESET left high), the circuit will hold the peak only until the input signal falls below the threshold or starts to rise again to a new peak.

The 3553 input buffer is used to isolate the source from the large input capacitance of C1.

As shown, the circuit is configured to detect positive signal peaks over a ±10V input range. Note, however, that the output will be inverted due to the −1 gain of the SHC804. If a careful layout and a good ground plain are used, the circuit will maintain high accuracy even for very small signals. To use the circuit for negative-going signal peaks, simply reverse the input polarity on both the comparators.

Key SHC803/804 specifications:

Acquisition time..... 350ns, max
Sample-to-hold
settling time ..... 150ns, max for ±0.01% throughput nonlinearity
Aperture "jitter"..... 10ps, typ

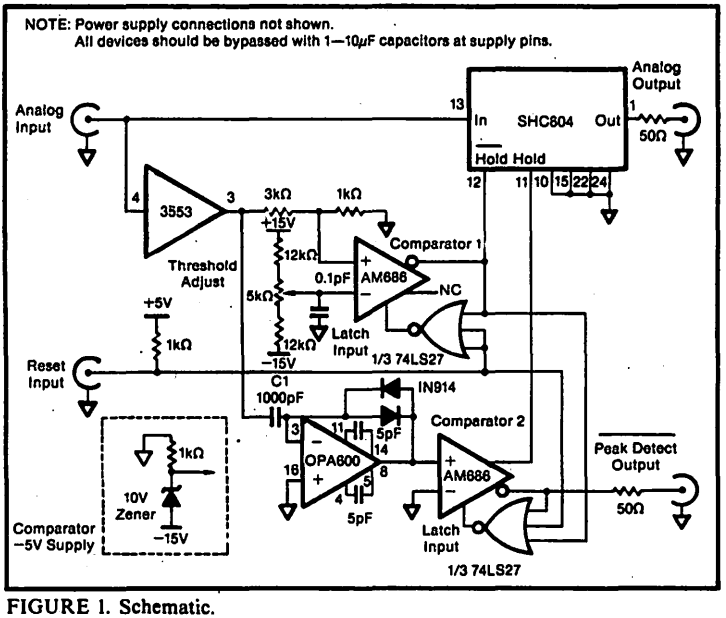

FIGURE 1. Schematic.

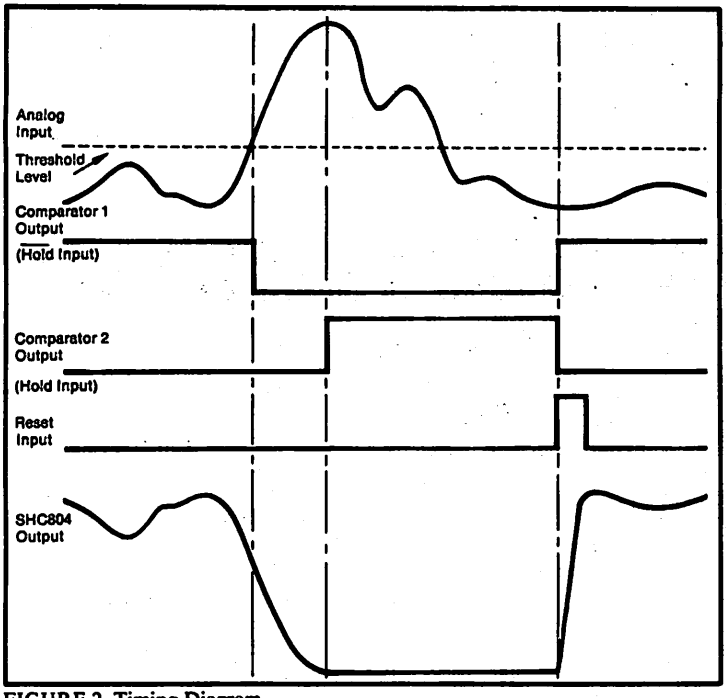

FIGURE 2. Timing Diagram.

A WAVEFORM DIGITIZER FOR DYNAMIC TESTING OF HIGH-SPEED DATA CONVERSION COMPONENTS

A sampling waveform digitizer is suitable for production testing of high performance analog and data conversion components. Completely automated dynamic performance characterizations of sample/hold amplifiers and fast digital-to-analog converters, including accurate measurement of settling time, have been implemented with this technique.

One of the most challenging requirements facing a supplier of high speed, precision data-conversion components is the accurate and efficient measurement of dynamic performance parameters. Important dynamic characteristics are usually determined via rather painstaking laboratory evaluation of a few randomly selected devices. Often the procedure involves the use of several different fixtures, requiring a skilled technician to operate the instruments and record the results properly. The performance specifications are then published as "typical" or "guaranteed but not 100% tested," neither of which is very satisfactory from the customer's point of view.

Some measurements, such as settling time of a fast current-output digital-to-analog converter (DAC), are traditionally so difficult to perform that the published specification is in fact only a "best guess," which the customer must verify by observing the device's apparent performance in his particular circuit. Therefore, it has become increasingly desirable to perform these difficult dynamic measurements on a production basis, as well as in the design laboratory. This requires that several different characteristics (e.g, settling time, slew rate, bandwidth, time delay) must be tested quickly, reliably, and with minimal socket changing or operator intervention.

These requirements became especially clear during the early development of a family of high speed data-conversion components, namely two fast-settling DACs and a high speed sample/hold amplifier. The DACs (both ECL and TTL input versions) were required to settle to 0.01% accuracy in 40ns; the sample/hold had to acquire a 10V signal to the same accuracy in approximately 250ns. Because the most important design choices were those that affected the speed/accuracy performance, it was necessary to be able to measure the dynamic parameters reliably and verifiably. Also required was a technique suitable for medium to high volume production testing, as well as one that customers could use for performance evaluation and incoming inspection.

This application note presents a highly accurate and flexible measurement technique which achieves previously unattainable results in the measurement of settling time, and also meets all the essential requirements of a production tester. The system can easily be adapted to measure the dynamic characteristics of op amps, DACs, sample/hold amplifiers and other analog system components. In addition, its flexibility makes it suitable for testing the dynamic switching characteristics of digital logic circuits.

The measurement system is essentially a sampling waveform digitizer which operates under computer control, enabling digital storage of time and amplitude points for software analysis. It employs a synchronous sampling detector consisting of a latching comparator with integrator feedback. This sampling technique meets the critical requirements of a high accuracy, high speed digitizer: wide analog bandwidth, very short aperture time, high linearity, and low noise.

ALTERNATE APPROACHES

Before adopting the technique described herein, several alternate approaches were considered. These include: high speed clipping amplifiers with oscilloscope viewing of the output, sampling oscilloscopes, window comparator techniques, and commercial waveform digitizers.

Conventional wideband oscilloscopes are suitable for measuring dynamic characteristics to only one or two percent accuracy. Precise settling time measurements cannot be made directly because the very large dynamic range of the signal overloads the oscilloscope amplifiers. Therefore, test circuits have been developed specifically to prevent overloading in the oscilloscope.

By clipping the test waveform with diodes or special "clipping amplifiers," it is possible to display the waveform on the most sensitive scale without severe overloading. However, the measurement accuracy still depends on several high speed, open loop amplifiers between the signal source and the display screen. The clipping circuit and amplifiers are themselves prone to thermal tails, ground loops and signal distortion.

Another technique to prevent oscilloscope overloading is to sum the settling waveform with a step generator of the same amplitude but opposite polarity, so that the large signal excursions are cancelled out.[1] This method requires that the settling time of the step generator itself be

significantly shorter than that of the device under test, presenting a problem of test verification. If the settling characteristic of the step generator could be measured, the capability of making the original settling time measurement would already exist. Therefore, the step generator is assumed to settle well based on theoretical circuit calculations rather than experimental verification.

Signal clipping and step generator techniques have been used successfully to measure current-mode DAC settling up to twelve-bit resolution, but a high level of expertise and engineering art is required to implement them properly. Interpretation of the displayed waveform is subject to operator error, and the test fixture is limited to settling time measurement. Evaluation of other parameters still requires an assortment of fixtures and equipment hookup configurations.

Sampling oscilloscopes have very high bandwidth and avoid the overload problems of conventional types, but the accuracy of the internal diode sampling bridge is limited to one or two millivolts. Also, there are numerous practical problems in attempting to drive the low input impedance.

An interesting method of testing settling time on a production basis is presented by Whealler[2]. This system uses a window comparator with adjustable thresholds. Once the DC final value of the waveform is determined, a system of DACs sets the reference levels at the positive and negative limits of the error band. The test stimulus is then applied to the DUT, and the window comparator output is enabled after the allowable settling time has elapsed. If the DUT output then exceeds the error band, the comparator triggers a flip-flop to indicate a settling time failure.

The window comparator is suitable for pass/fail production testing of moderately high speed waveforms. However, it does not lend itself to laboratory development or characterization work, because it gives no information about the actual shape of the waveform.

To meet the needs of both the development laboratory and the production floor, a system which permanently records the detailed waveshape is required. In other words, the ideal system is an accurate, high speed waveform digitizer.

Recognizing this, test equipment manufacturers have developed digitizers in various forms. Waveform recorders, transient recorders and digital oscilloscopes are all designed to capture and store a set of time-amplitude points in digital form. Once the signal has been digitized, it is equally useful for production pass/fail decisions as for detailed engineering analysis.

While the digitizer concept is attractive, commercially available units do not yet offer the combination of bandwidth and resolution necessary for the type of high accuracy measurements under consideration.

DESCRIPTION OF THE SAMPLING DIGITIZER

Figure 1 is a block diagram of the digitizer. The waveform under test is fed to the inverting comparator input. The comparator's digital output is integrated by op amp A_1 and fed back to the noninverting (reference) input.

The latching comparator is functionally equivalent to a conventional comparator whose output is latched with a "D" type flip-flop. The comparator's strobe input corresponds to the clock input of the flip-flop (Figure 2).

In a true latching comparator, however, the latching action occurs in the analog input stage[3] which has only moderate gain but very high bandwidth. Therefore, propagation delay and bandwidth limitation in the high gain output stages do not affect the accuracy of the measurement. Because the latching event is edge-triggered, the effective aperture time is well under 500ps.

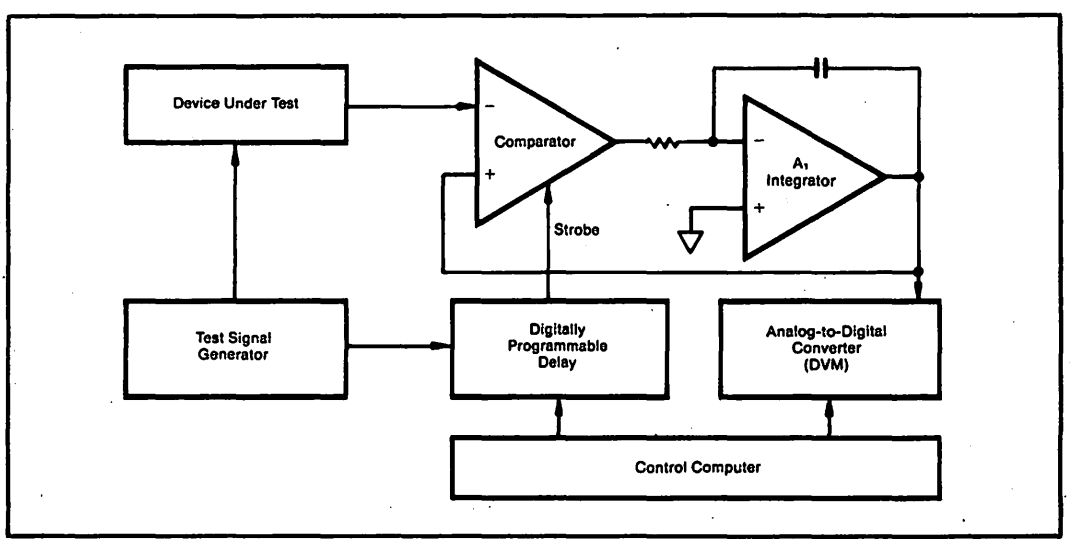

FIGURE 1. Block Diagram of the Sampling Waveform Digitizer.

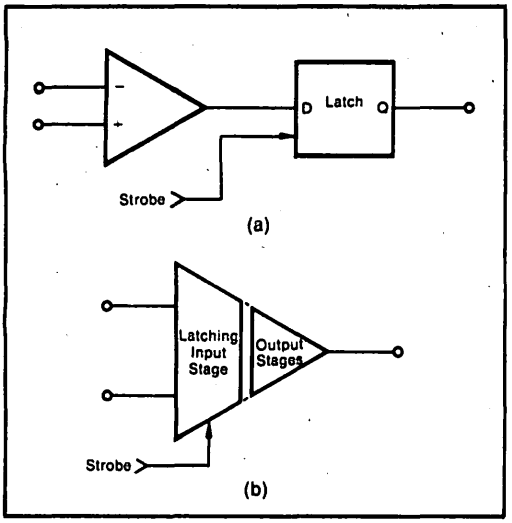

FIGURE 2. (a) Logical Equivalent of Latching Comparator; (b) Latching Actually Occurs in the First Stage.

Figure 3 is an illustration of the sampling/digitization process. Sampling of the waveform under test is accomplished by repeatedly strobing the comparator at a selected time point, until the integrator feedback forces the comparator reference input to equal the sampled value of the input signal. In effect, the comparator/integrator loop forms a bang-bang servo in which the equilibrium condition results when the integrator output oscillates about the sampled value. Once the loop settles, this value is read by the analog-to-digital converter and sent to the computer. The sample point is computer controlled via the programmable delay.

ADVANTAGES OF SYNCHRONOUS SAMPLING

The repetitive sampling technique (sometimes referred to as "equivalent time sampling") has several important advantages over transient recorders or window comparator methods. First, random noise in the system is averaged out by the op amp integrator. The effectiveness of this noise averaging is determined by the integration constant and the number of samples taken at each time point. This is in contrast to the single-shot "transient recorder" type of digitizer, in which the sample/hold acts as a peak detector for system noise.

Second, the op amp integrator operates at very low frequencies (essentially DC) relative to the waveform under test. Only the comparator input circuitry is required to track the input waveform. There is no need for a precision high speed amplifier, which is a significant limitation in conventional sampling systems.

A third important advantage of this repetitive sampling technique is that the measurement resolution is not limited by the comparator's tendency to oscillate for very small differential input voltages. In other systems, this "oscillation band," which is typically 1-5mV for high speed comparators, is a significant resolution limit. The oscillation can be prevented by adding positive feedback, but the resultant hysteresis around the comparator trip point is also detrimental to system accuracy.

In the sampling waveform digitizer, this oscillation is prevented by strobing the comparator with a narrow pulse (5-10ns wide). This enables the feedback loop to track the sampled value with far greater precision than the "oscillation limit" would suggest. In the author's system, the resolution limit is approximately 50μV, or roughly 50 times more precise than the comparator alone.

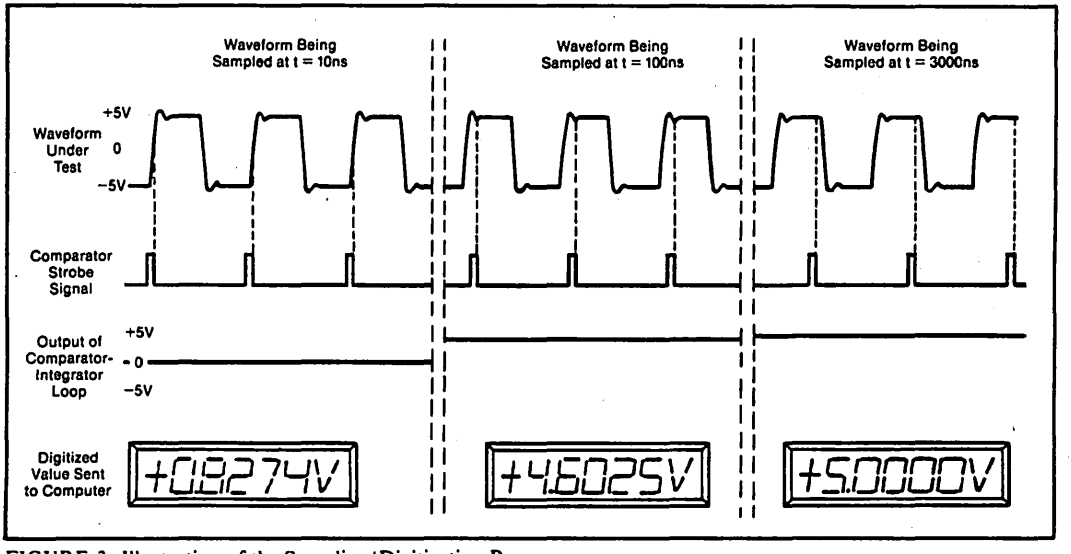

FIGURE 3. Illustration of the Sampling/Digitization Process.

SELECTION OF INTEGRATION CONSTANT

To maintain this resolution, the integrator output slope must be small enough that the integrator output changes by a negligible amount between samples.

$$dV_{Out}/dt = I_{In}/C_F$$

One sample is taken per cycle of the input waveform, so the time between samples is equal to the period To: period To:

$$t_{Between\ Samples} = To = 1/fo$$

If ΔV_{Max} represents the largest allowable integrator error, then the maximum slope is calculated by

$$dV_{Out}/dt = \Delta V_{Max}/To = I_{IN}/C_F$$

where I_{In} is determined by the value of the integrator input resistor R_{In} and the magnitude of the comparator's output voltage (assuming that it swings symmetrically about ground). Figure 4 is an illustration of the integrator error calculation. Note that the correct sampled value will not necessarily equal the average value of the integrator output, but may lie anywhere between the positive and negative limits. Thus, it is important to select a small enough ΔV_{Max}. For example, if the waveform under test has a frequency of 1MHz and the maximum allowable error is set to be 50μV, the integration constant will be:

$$I_{IN}/C_F = \Delta V_{Max}/To = 50\mu V/\mu s$$

In the case of a lower frequency waveform which must be measured to very-high accuracy, the I_{IN}/C_F ratio will become much smaller. As the output slope decreases, it may begin to take an intolerably long time for the comparator-integrator loop to acquire a full-scale step change. In that case, the integrator can be designed with a variable I_{In}/C_F: large to allow fast acquisition of large changes in the sampled value, and small to allow precise tracking.

SELECTION OF SAMPLING INCREMENT

Because the digitizer operates in the synchronous sampling mode rather than in real time, the timebase resolution can be arbitrarily small. The programmable delay line used in the present system is variable in 1ns increments, yielding a maximum effective "sampling rate" of 1GHz. This allows for accurate delay and risetime measurements, but it does not imply that the system can digitize 1GHz waveforms. The bandwidth of the comparator input stage is limited to about 100MHz, which is adequate for the devices under consideration. If it became desirable to accurately digitize higher frequency components, a latching comparator with a 1GHz input stage and 1–10ps aperture time would be required.

Although the system is capable of sampling the waveform in 1ns steps, the actual time increment used depends on the parameter under test. For example, the measurement of signal delay to 1ns accuracy requires waveform digitization of only two points that may be tens or hundreds of nanoseconds apart. To make the test run quickly, it is desirable to take as few time-amplitude points as possible without compromising the validity of the measurement.

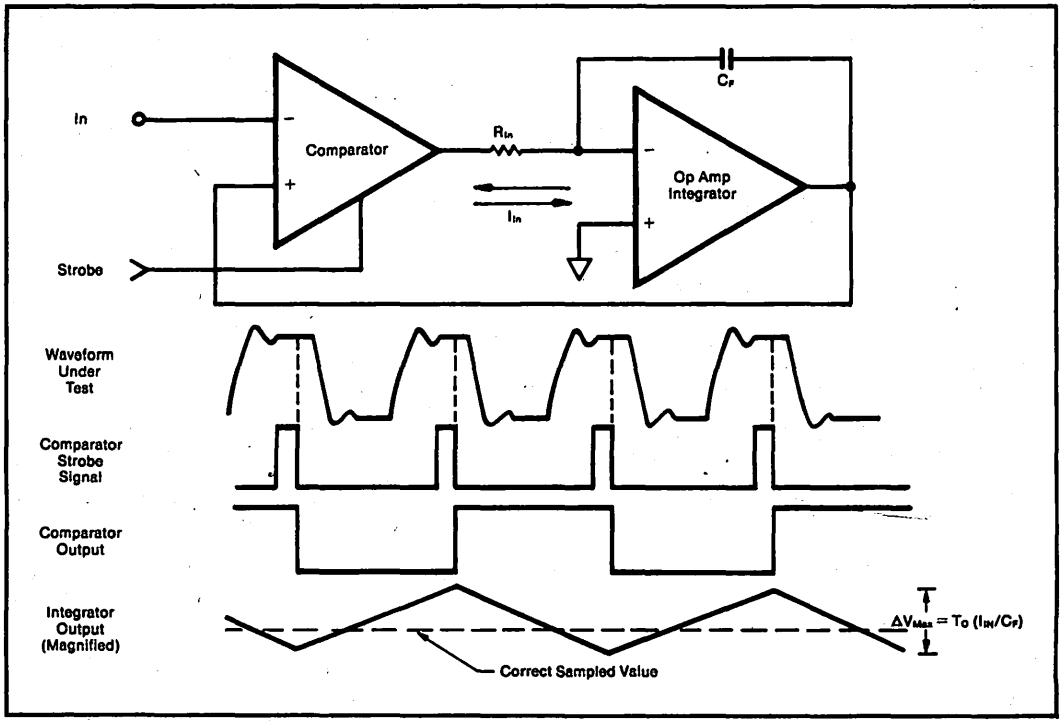

FIGURE 4. Integrator Error Calculation.

For settling time measurements, the required timebase resolution is not immediately obvious. If too few samples are taken over the period of interest, it is possible that the waveform could exceed the error band between samples. To illustrate this, consider the case of an oscillatory settling response (Figure 5). If the sampling increment is an integer multiple of the oscillation period, the sample points may easily coincide with the zero crossings of the wave. In that case, the measured settling time would be very much shorter than the actual.

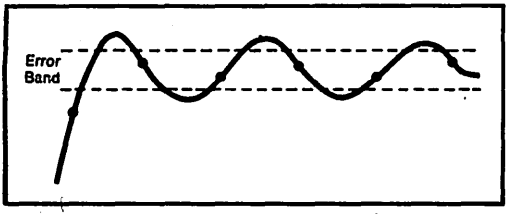

FIGURE 5. Incorrect Selection of Sampling Interval.

One way to prevent this type of error is to apply the Nyquist sampling criterion:

$$T_S < 1/2\, f_{Max}$$

where T_S is the sampling increment and f_{Max} is the highest frequency component of the waveform. However, strict use of the Nyquist rate is required only when the signal to be digitized is completely random or completely unknown. Because the settling waveform is not entirely random, reasonable assumptions may be made to reduce the number of sample points and thereby speed up the test.

DESCRIPTION OF THE PRESENT SYSTEMS

So far, two types of automated benchtop testers have been implemented with this technique. The first is used for measuring the settling time of a 12-bit DAC whose current mode output reaches 1/2LSB accuracy in under 40ns. The second is a dynamic tester for sample/hold amplifiers which measures acquisition time, sample-to-hold settling time, aperture delay, glitch area and slew rate.

DAC Tester

Of the two, the DAC tester is a more basic implementation of the block diagram shown in Figure 1. Nonetheless, it is noteworthy because it allows reliable and verifiable production testing of current-mode DAC settling, which has been one of the most difficult measurements to perform under any circumstances.

A simplified schematic of the DAC tester is shown in Figure 6. The test stimulus signal is provided by IC1, a TTL oscillator set to run at approximately 1MHz. IC2 is an 8-bit programmable delay line which is adjustable from 0–255ns in 1ns steps. The delay is computer controlled using a general purpose parallel output port.

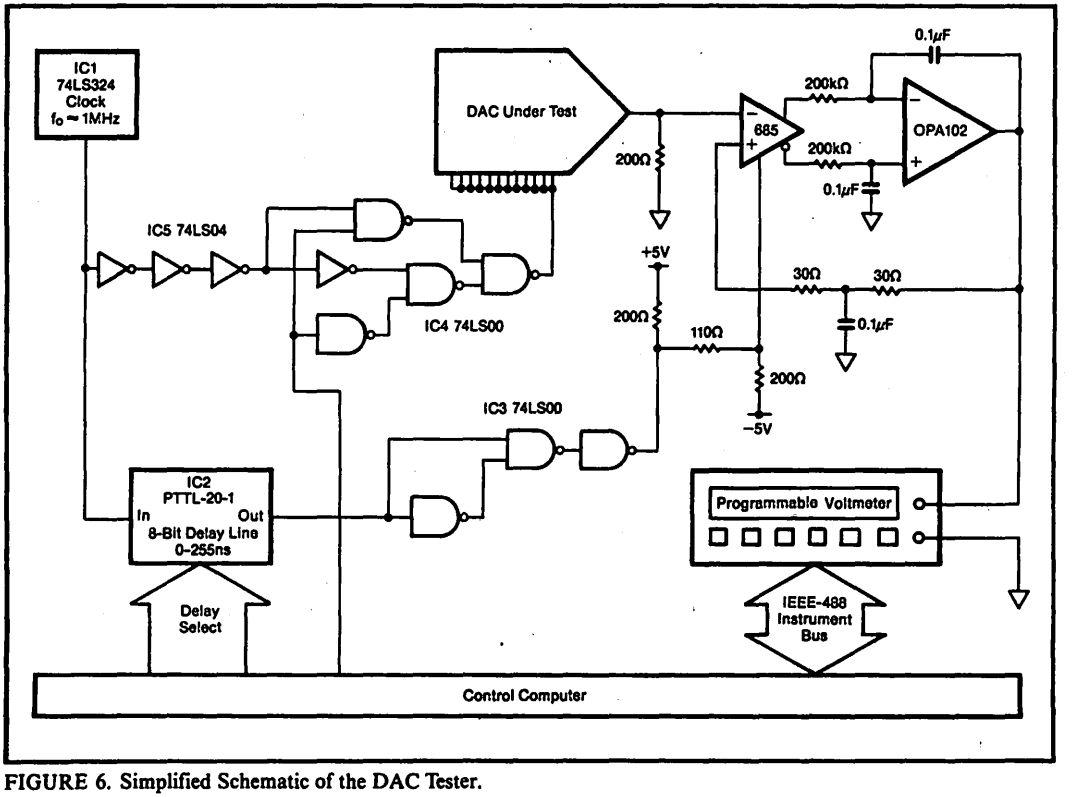

FIGURE 6. Simplified Schematic of the DAC Tester.

The rising edge of the delay line output is converted to a positive pulse (approximately 7ns wide) through the TTL "differentiator" circuit formed by IC3. This TTL pulse is translated to ECL levels with a resistor network and becomes the comparator strobe signal.

The original clock signal is also used to switch the DAC under test between zero and full scale, with the polarity selected by the computer via IC4. To ensure that the comparator can sample at the actual transition time of the DAC, IC5 is used to add delay. This compensates for the built-in strobe delay through IC2 and IC3. The computer can thus calibrate itself to the "time zero" point of the DAC output waveform by digitizinag both before and after the transition.

The 0-10mA DAC output is converted to a voltage by the 200Ω shunt resistor. Thus, the value of the least signficant bit is:

$$LSB = 2V/2^{12} = 2V/4096 \approx 0.5mV$$

or roughly ten times greater than the minimum system resolution.

IC6 and IC7 form the comparator-integrator feedback loop. Note the "T" filter network which isolates the comparator reference input from the integrator output. This is required to prevent the comparator input current, which switches on and off at the clock frequency, from causing a disturbance at the integrator output. The DC output is sent to a digital voltmeter which communicates with the computer over the standard IEEE-488 instrument bus.

Sample/Hold Tester

Shown in Figure 7, the sample/hold tester extends the capabilities of the basic digitizer by employing three separate comparator/integrator loops—one each for input, output, and amplifier error signal (false summing node). A fourth latching comparator, without an integrator, is used to detect the exact timing of the hold-to-sample and sample-to-hold transitions at the hold command input.

All comparators are latched simultaneously by the variable delay circuit, which is programmable in 1ns increments from 0–64μs. The exact value of the delay is set by placing a 16-bit control word on one of the computer's parallel output ports.

The timing circuit uses a 4MHz crystal-controlled clock to allow 256 "coarse" delay settings from 0–63.75μs. The clock signal increments an 8-bit binary counter every 250nsec. The counter value is compared with the upper 8

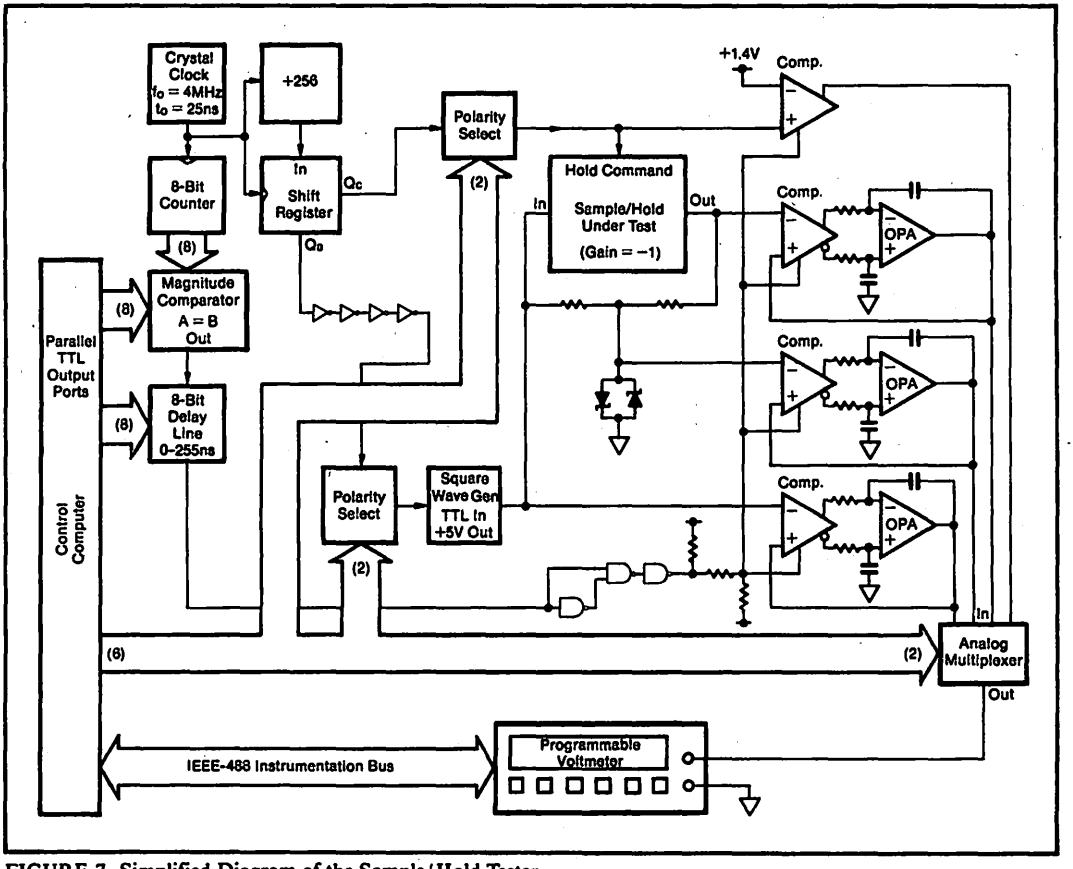

FIGURE 7. Simplified Diagram of the Sample/Hold Tester.

bits of the "delay select" word from the computer. When the two numbers are equal, the output of the 8-bit magnitude comparator goes high. This rising edge is sent through the 0-255ns delay line, which adds the "fine" delay value as selected by the lower 8 bits of the control word. The delayed signal is then converted to the comparator strobe pulse by a differentiator/level shifter circuit similar to the one described above for the DAC tester.

The test stimulus signal is created by dividing the 4MHz clock frequency by a factor of 256, giving a square wave with a period of 64μs. The sample/hold itself is driven by a fast settling generator which converts TTL levels to ±5V. The generator can be set under software control to follow the test stimulus, to invert it, or to ignore it. In the last case, the generator output can be fixed at ±5VDC for observing the final value.

The TTL hold command signal is controllable in the same way as the generator input, except that it is delayed by 500ns through a shift register.

By independently controlling the polarities of the generator and the hold command signal, the tester can be configured to measure acquisition time (hold-to-sample settling time), sample-to-hold settling time, sample-to-hold offset (pedestal), glitch amplitude, aperture delay time, hold mode feedthrough rejection, risetime, and slew rate. The analog multiplexer determines whether the voltmeter reads input, output, false summing node or hold command.

For acquisition time measurements, the familiar "false summing node" method is used. Because this technique reproduces the error signal of the internal amplifier in the sample/hold, it automatically compensates for slow settling tails in the signal generator. This was convenient since the sample/hold in question is based on an inverting amplifier. However, it should be noted that noninverting amplifiers and sample/holds can be measured just as accurately by digitizing both input and output signals. In that case, software calculations would compensate for any imperfections in the test signal generator.

Acquisition, sample-to-hold settling and aperture delay are defined with respect to the time of the hold command transition. Therefore, the hold command signal is fed to a latching comparator whose reference input is tied to +1.4V, the TTL switching threshold. The voltmeter reads the comparator output directly; no integrator is required because the shape of the wave is not critical.

In searching for the exact time of the signal transition, the computer operates in "successive approximation" fashion. First, the comparator is strobed at a particular time point and its output is digitized. Next a different time point is selected. If the comparator output switches, the computer tries a value midway between the first two. The process continues until the switching time point is found, and all subsequent measurements are referred to that value.

Figure 8(a) is a computer printout of the measured acquisition time characteristics, in which t = 0 corresponds to the hold-to-sample transition. Figure 8(b) shows the detailed settling characteristics as measured at the false summing node.

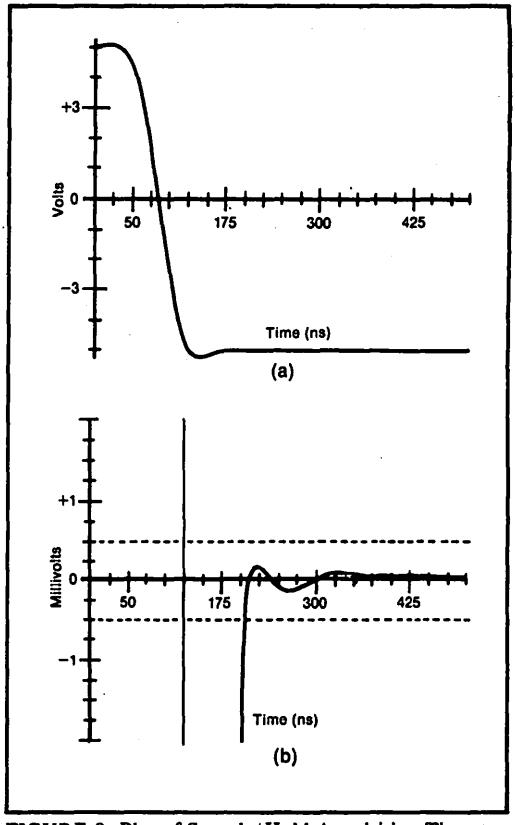

FIGURE 8. Plot of Sample/Hold Acquisition Time.

CALIBRATION STANDARD

With any measurement technique, it is desirable to have a calibration standard to validate the results. Although it is impossible to generate a "perfect" voltage step (i.e., zero risetime and zero droop or ringing), a close approximation can be realized with a network of Schottky diodes as shown in Figure 9(a). The theoretical turnoff time of this network is dominated by the RC time constant, and may be calculated as follows:

$$C_{Node} = C_{Diode} + C_{Comparator\ Input}$$

$$RC = 200\Omega \times 5pF = 1ns$$

Settling to 200μV for a 2V step (0.01% settling requires that

$$V(t_s) = 200\mu V = V(O)\,(1 - e^{-t_s/RC})$$

Solving for t_s gives $t_s = 9.7ns$

In practice, the settling time is also affected by ringing due to lead inductance and imperfect grounds. Figure 9(b) is a computer plot of the Schottky diode turn-off waveform as measured on the digitizer system. The measured settling time to ±200μV is within 7ns of the theoretical.

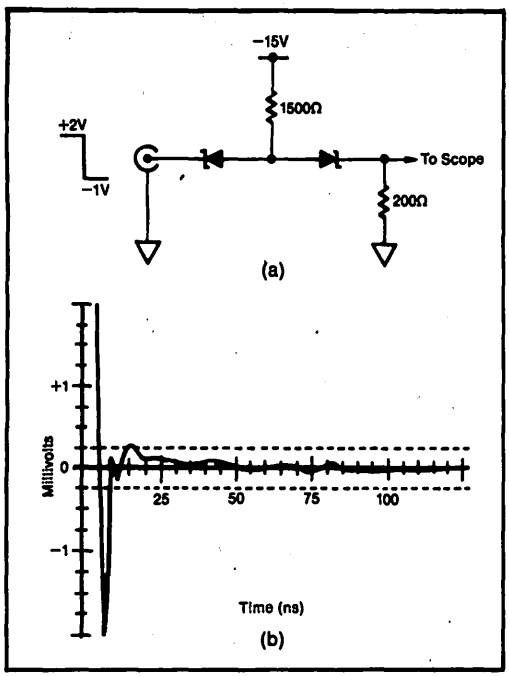

FIGURE 9. Schottky Diode Test Circuit and Resultant Plot.

DETERMINING THE FINAL VALUE

In the specification of settling time, it is important to be clear about the meaning of the term "final value." For example, an amplifier output may appear to settle very quickly to a particular error band when viewed in the 1-10μs time frame. When observed over a period of milliseconds, however, it may also exhibit a thermally induced "tail" which causes it to drift out of the prescribed error band. Whether or not the device can still be called a "fast settling amplifier" depends on the particular application, but a rigorous definition of the final value would probably disallow the claim.

There are two ways to determine the true final value using the sampling waveform digitizer. The first is simply to extend the maximum delay of the programmable time base to some reasonably large value, enough to allow thermal tails and other long term effects (such as dielectric relaxation of capacitors) to settle out. One consequence of extending the time base is that the repetitive sample pulses are spaced further apart, requiring that the integrator output slope become very small to preserve system accuracy. In that case, the integration constant could be variable as described above.

Another way to determine the final value is to program the test stimulus generator for a DC output while still strobing the comparator repeatedly. Thus the device under test can reach its equilibrium state, and the computer will read the DC final value after a programmed waiting time.

Again the Schottky diode turn-off waveform serves well to verify the final value measurement. The network in Figure 9(a) settles exactly to ground independent of heating effects in the diode or resistors.

FUTURE IMPLEMENTATIONS OF THE DIGITIZER

The basic concept of the sampling waveform digitizer can be implemented in a variety of ways, depending upon the desired application.

For engineering design and development work, the system could be configured as a digital sampling oscilloscope. This would combine direct viewing of the signal with digital waveform storage for software analysis. The comparator-integrator sampling circuit would probably be located at the probe tip rather than inside the oscilloscope, thus avoiding the problem of accurately driving a terminated cable. For probing custom-built test fixtures, the sampling circuit need not even be attached to the probe. It is inexpensive enough to be incorporated at one or more test points in the layout of the fixture itself, minimizing probe lead length and grounding problems.

In a production environment, it may be advantageous to incorporate the digitizer into a test head which connects to existing automatic test equipment. The time base (programmable delay function) and sampling circuit would reside in the test head itself; some degree of local computer intelligence might also be useful to avoid overloading the central system processor with details of running the test.

Further improvements in bandwidth and resolution will depend almost entirely on the design of faster and more accurate latching comparators, barring the development of even more precise ways to sample high speed signals. One of the limitations of any production test is the requirement that the DUT must be easily inserted and removed from the tester. Any kind of socket tends to be detrimental to the performance of high speed devices, which are designed to work best when soldered onto a circuit board with a good ground plane. Some work has been done to create a zero insertion force socket with short, low-inductance connections, but much more remains to be done before the socket becomes a negligible factor.

CONCLUSION

Designers, manufacturers, and users of modern data conversion components require accurate and reliable methods to measure dynamic performance characteristics. Existing test methods are sometimes inadequate, often difficult to perform and tend to be specific to a particular category of tests.

A sampling waveform digitizer is proposed as a highly accurate and generally useful technique for dynamic testing and characterization. It is relatively inexpensive and is well suited for both production and design engineering environments.

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SUBRANGING HIGH-SPEED MODULAR ANALOG-TO-DIGITAL CONVERTERS

The objective of this development was to create a 10MHz, 12-bit analog-to-digital converter (ADC) that offers improved performance over similar products that already exist in the marketplace. In addition, it was recognized that an important part of the market is price elastic, so a great deal of effort was directed toward optimizing cost, performance, and reliability. A modular design approach was adopted to reduce the development risk associated with heat-related packaging problems and also to manage efficiently the design of the individual subassemblies. Once it was determined that a modular design approach was necessary, it became apparent that the modules had to be designed so that they could be manufactured, adjusted, and tested individually. This allowed a system to be assembled without the need for selecting associated groups of modules. This program objective, dictated by reliability requirements, was important because the design does not make use of any potentiometers. All critical accuracy and timing adjustments are performed on the module level, so that when random modules are plugged into a printed circuit board, the system specification is achieved with high yield. A photograph of the 12-bit, 10MHz ADC, the ADC600, is shown in Figure 1. The ADC measures 0.25 by 3.75 by 4.5 inches. The ADC characteristics are shown in Table I.

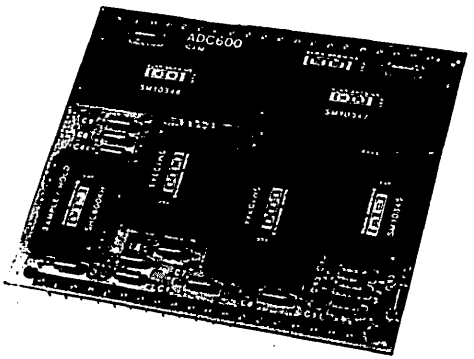


FIGURE 1. 12-Bit 10MHz ADC600.

SYSTEM ARCHITECTURE

The ADC employs a two-step, subranging architecture with digital error correction. This architecture was selected since it provides the best compromise between system performance and system complexity. An ADC employing the successive approximation algorithm is simple, due to its serial nature. For this type of design the conversion rate is N times that of an individual bit decision. A bit decision is determined by the settling time of a DAC and the response time of the associated logic and comparator. For an ADC with 12 bits of resolution, 0.6–1μs represents the minimum conversion time using successive approximation. At the other extreme, the flash converter technique has a very short conversion time. Only a single cycle of a comparator and logic is needed, and there is no digital-to-analog converter (DAC) at all. While this technique is quite fast, the speed is achieved at the expense of increased circuit complexity. Flash converters with 8 bits of resolution and conversion rates to 100MHz represent the limit that can be achieved with a monolithic approach. Emitter-coupled logic (ECL) was chosen as the logic type to attain high speed and low noise. In addition, some of the key components, such as the flash encoders and the DAC, are ECL-compatible. The design approach used existing proven technologies, configured in moduar hybrid fashion to reduce development risk while still achieving a significant advance in terms of system performance at a low cost. At final assembly, working modules are plugged into a four-layer printed circuit board. Each layer serves a specific function. There are separate layers to route the analog, digital, and power connections. The fourth layer shields the digital and analog signals from each other.

TABLE I. Characteristics For 12-Bit, 10MHz ADC600.

Analog Input Range	±1.25V
Input Impedance	±1.5MΩ
Gain Error	±0.1%
Offset Error	±2.5mV
Integral Linearity (at 200Hz)	±1.0LSB
Differential Linearity (at 4.8MHz)	±0.5LSB
Harmonic Distortion (at 4.8MHz)	71dB below full scale
Aperture Time	6ns
Aperture Uncertainty	±5ps
Input Bandwidth	70MHz
Sampling Rate	10MHz
Gain Drift	±30ppm/°C
Offset Drift	±25μV/°C
Power Consumption	8.5W
Size	0.25 × 3.75 × 4.5 inches
Temperature Range (K)	0°C to 70°C
(B)	−40°C to +85°C

A TWO-STEP ANALOG-TO-DIGITAL CONVERTER

See Figure 2 for a block diagram of the modular 12-bit, 10MHz ADC600. The analog signal is initially sent to a sample/hold to reduce the aperture jitter of the system to 5ps. The output of the sample/hold, the SHC600, is then sent to two places: to a 7-bit flash encoder module and to a subtraction circuit. An important feature of the sample/hold design is that the sampling switch is buffered by a fast-settling closed-loop amplifier. This allows the gain of the entire ADC to be predetermined at the modular level to a typical accuracy of 0.1%.

A diode bridge switching arrangement was chosen for the sampling switch because it offers the best solution to the conflicting requirements of accuracy and speed demanded by the ADC. The input to the sampling bridge is driven by a high-input-impedance, low-capacitance buffer to ease the ADC interfacing requirements. Another important feature of the sample/hold architecture is that only the holding capacitor need acquire the signal to the rated accuracy in 25ns. Due to the fact that the capacitor is not in the feedback path, the output amplifier has only to settle to 7-bit accuracy in 25ns. The digital correction circuitry is capable of correcting this error, as long as the amplifier settles to 12-bit accuracy by the time the second encoder is strobed. Therefore, an additional 60ns can be tolerated when settling to 12-bit accuracy. In a similar fashion, the effects of capacitor droop can be tolerated and will create only an offset error, not a linearity error. After the acquisition time of 33ns has elapsed, an additional 18ns is allowed before the first 7-bit flash encoder is strobed.

This first encoder determines the initial coarse approximation of the input signal. Two 7-bit flash encoders were chosen for the MSB and LSB encoders. These provide adequate resolution, accuracy, and range to allow the digital correction circuitry to assemble the final 12-bit word properly. More detail explaining the operation of the digital correction circuitry is given later in the text. The flash encoders are ECL-compatible to attain minimum throughput delay while minimizing power supply noise. The digital output from the first flash encoder is sent to the Subtracting DAC module.

There, the initial approximation to the analog signal is converted back to analog form and subtracted from the input signal for further processing. The Subtracting DAC module is composed of four main sections: the reference generator, a 7-bit DAC with 14-bit accuracy, a FET switch, and a high speed amplifier. The reference generator supplies a 10V DC level, which is used by the DAC and by the two flash encoders. Since there is a

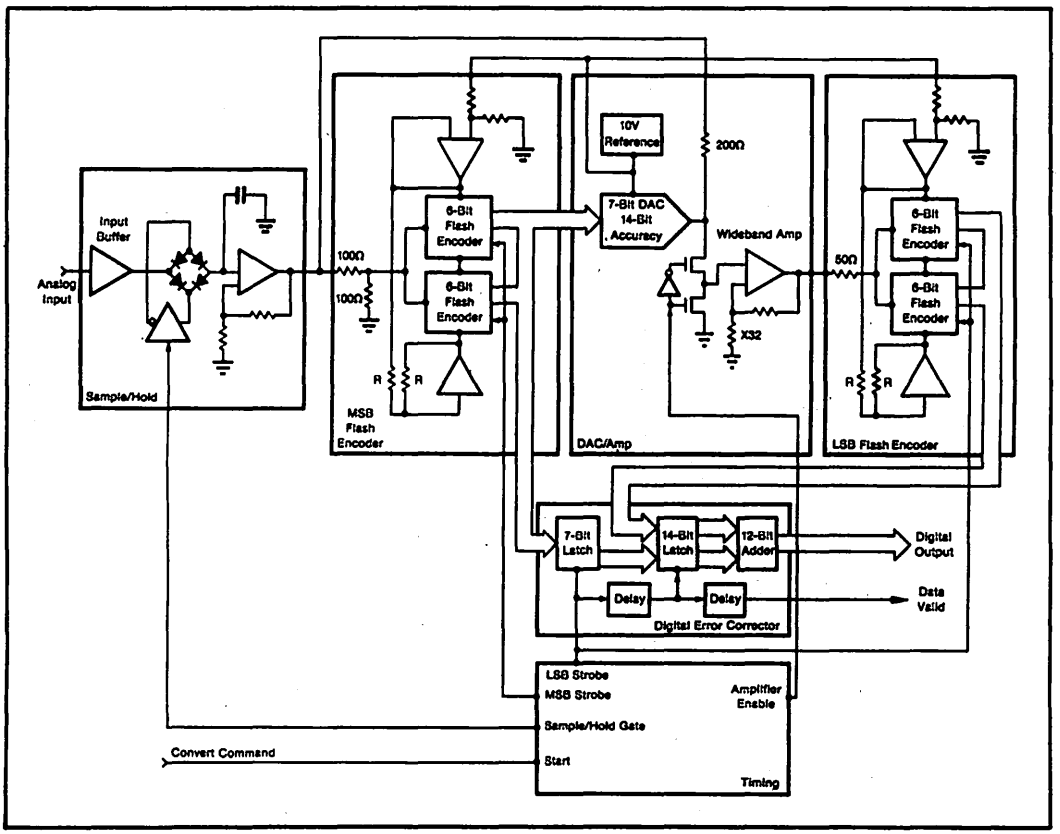


FIGURE 2. Block Diagram of 12-Bit 10MHz ADC600.

single reference, changes in this voltage only affect the overall gain and not the linearity. The reference was placed in the DAC module to achieve system simplicity along with attaining highest accuracy when the DAC is undergoing final laser trim. The DAC itself is ECL-compatible and achieves 14-bit accuracy with a settling time of 25ns.

The output from the sample/hold is subtracted from the DAC output by means of a resistive network. The output of this resistive network is then amplified by a high speed gain-of-32 amplifier to attain the proper range before being applied to the final flash encoder. By examining the system block diagram, it should be noted that before the subtracted signal is actually amplifed, the difference signal is passed through an FET gating switch. This is done to prevent the amplifier from overloading during a time when the sample/hold is processing a new signal and the MSB flash encoder is still holding data from the previous sample. The output from this amplifier is sent to another 7-bit flash encoder that is similar to the previously mentioned encoder that quantizes the most significant bits.

From the manufacturing point of view the two encoders are identical, the difference being that the gain of the MSB encoders is 0.5, while that of the LSB encoder is 1.0. That was done to use the same reference voltage without having to double the gain of the high speed amplifier that is used to drive the LSB encoder. Operating this amplifier at a lower gain allows it to have a greater bandwidth, which implies a reduced settling time. The settling time of this amplfier is 25ns, which is important in meeting the throughput requirements of the ADC. Once the data in each of the encoders has been latched, it is then sent to the Digital Error Correction module to be assembled into the final 12-bit word.

This module contains buffer latches, as the data from each encoder is not available for a sufficient length of time to assure that the data will completely propagate through the adder. Digital correction is achieved by adding the data from each encoder in the proper manner. Most of the circuitry in this module is contained within an ECL gate-array. Even though the first flash encoder determines the signal only to 7-bit accuracy, it is still possible to achieve 12-bit performance providing that the DAC has the necessary accuracy. The output of the subtraction circuit contains the difference between the output of the sample/hold and the analog equivalent of the first 7-bit encoding process. If the 7-bit encoder was more than 12-bit accurate it would only be necessary to have a 5-bit encoder to quantize the residue without digital correction. Since the first encoder is typically only 7-bit accurate, it is necessary that the second encoder have two additional bits to handle the larger difference that could result. The final 12-bit word is then developed at the output of the 12-bit adder. An analysis of the operation of how digital correction works is shown in Figure 3. The final module of the set supplies the necessary timing signals to various parts of the system. Refer to Figure 4, which shows all the timing waveforms that are required for operation of the converter.

The conversion process is initiated by bringing the convert command signal high. At this same time, the sample/hold is placed in the hold mode. After a delay of 18ns, to allow for sample-to-hold settling, an 8ns pulse is generated which is used to strobe data into the first flash encoder. 22ns is allowed for the latched data to become available to drive the DAC. At about the same time that the new data is presented to the DAC, the Amplifier Enable signal permits the amplifier to be switched back into the active mode. After the output of the amplifier has settled, another 8ns strobe pulse is generated which latches the ouptut of the lower 7-bit converter. This same strobe pulse is also used to transfer the output of the initial 7-bit converter into a buffer latch to avoid critical

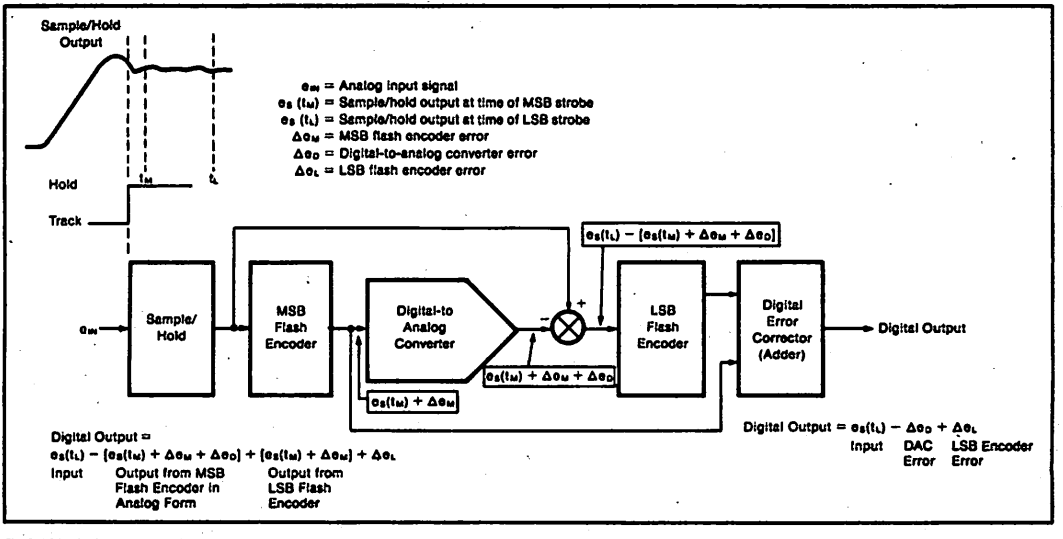


FIGURE 3. Operation of Digital Error Correction.

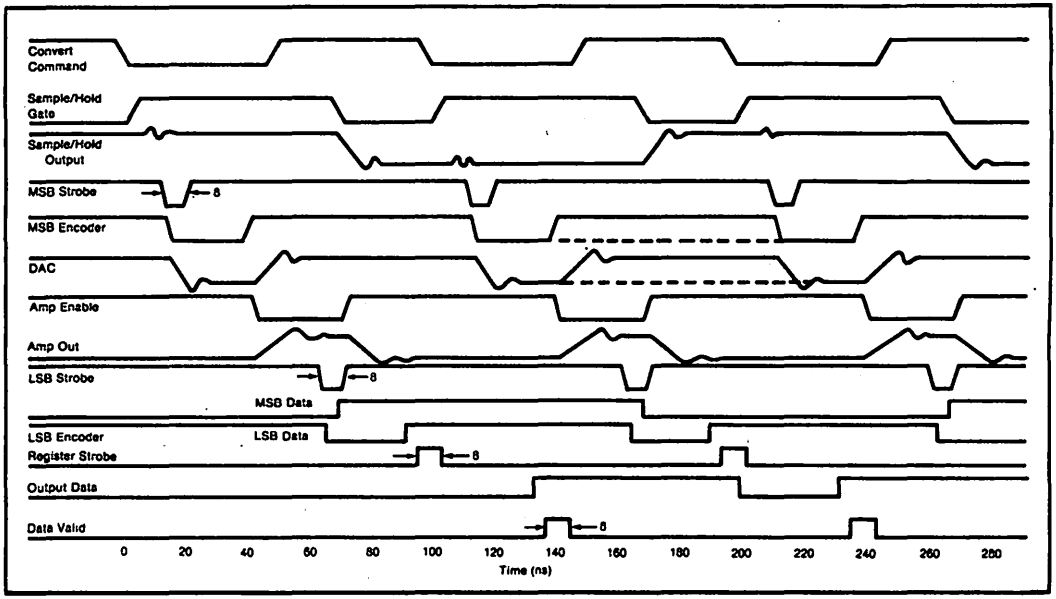


FIGURE 4. Timing Diagram of 12-Bit 10MHz ADC600.

timing problems. Once the data representing the conversion is stored in digital form, the sample/hold is placed back into the sample mode. For similar reasons, the data output from both encoders is stored in a 14-bit latch. A pulse derived from the LSB encoder strobe occurs 22ns later to enter data into this 14-bit latch. A final pulse, called Data Valid, is generated to indicate when the digital data is stable at the output of the converter. For ease of signal routing, these final timing signals are located within the Digital Error Correction module. The various timing pulses are laser trimmed to 1ns accuracy.

ADC MODULES

Sample and Hold—The sample/hold, the SHC600, acquires input step changes of 2.5V to 0.1% accuracy in 30ns. The aperture time of the sample/hold has been measured to be 5ps, with a small signal bandwidth of 75MHz. Table II summarizes the other characteristics of the sample/hold. Figure 5 shows a simplified schematic of the sample/hold. One of the unique features of this design is the use of a closed-loop FET operational amplifier to buffer the hold capacitor. There are several benefits that result from the use of a feedback amplifier in this application as compared to an open-loop buffer that is commonly found. Due to the fact that the operational amplifier is connected as a voltage follower, the output impedance of the buffer is 0.25Ω, as opposed to 5Ω that is typical of an open-loop buffer. This simplifies the interface between the sample/hold and the rest of the system, as the other system components (such as the subtraction amplifier and the flash encoder) do not require high impedance inputs. The sample/hold can drive low impedances, which results in reduced settling times when terminated signal lines are used. Since the gain of an operational amplifier is set by external resistors, it is possible to then laser-trim the gain of the entire sample/hold to a precise value. In addition, provision is made to trim both the offset and offset drift of the entire sample and hold by trimming those parameters at the amplifier level. Initially, measurements are made to determine the untrimmed offset and offset drift. It has been determined that the sensitivity of offset is 3μV/°C/mV for the entire sample/hold. Therefore, once the untrimmed drift has been measured, changing the offset by trimming either R1 or R2 nominally sets the voltage offset drift to zero, R1 and R2 being the emitter resistors of the current sources that set the current in the input FET stage that affects both the offset and the offset drift. R3 and R4, the source resistors associated with the FET Q1 and Q2, are then adjusted to bring the overall offset to zero, as these resistors do not affect the offset drift.

The sampling function is performed by switching the bridge of hot carrier diodes CR1 through CR4 from the "on" to the "off" state. The bridge bias current is generated in current source FETs Q3 and Q4. During the sample mode this current is steered through the diode bridge by turning on transistors Q5 and Q8. The bridge is returned to the hold mode by turning Q5 and Q8 off and turning Q6 and Q7 on. The action of turning Q6 and Q7 on creates a negative bias on the anodes of CR1 and CR2 and a positive bias on the cathodes of diodes CR3 and CR4. Since the bias voltages are referenced to the output, creating a "bootstrap effect," the reverse bias voltage that diodes CR1 through CR4 experience becomes independent of signal level. This is an important aspect of the design, as this action prevents the charge offset pedestal from becoming a non-linear function of signal

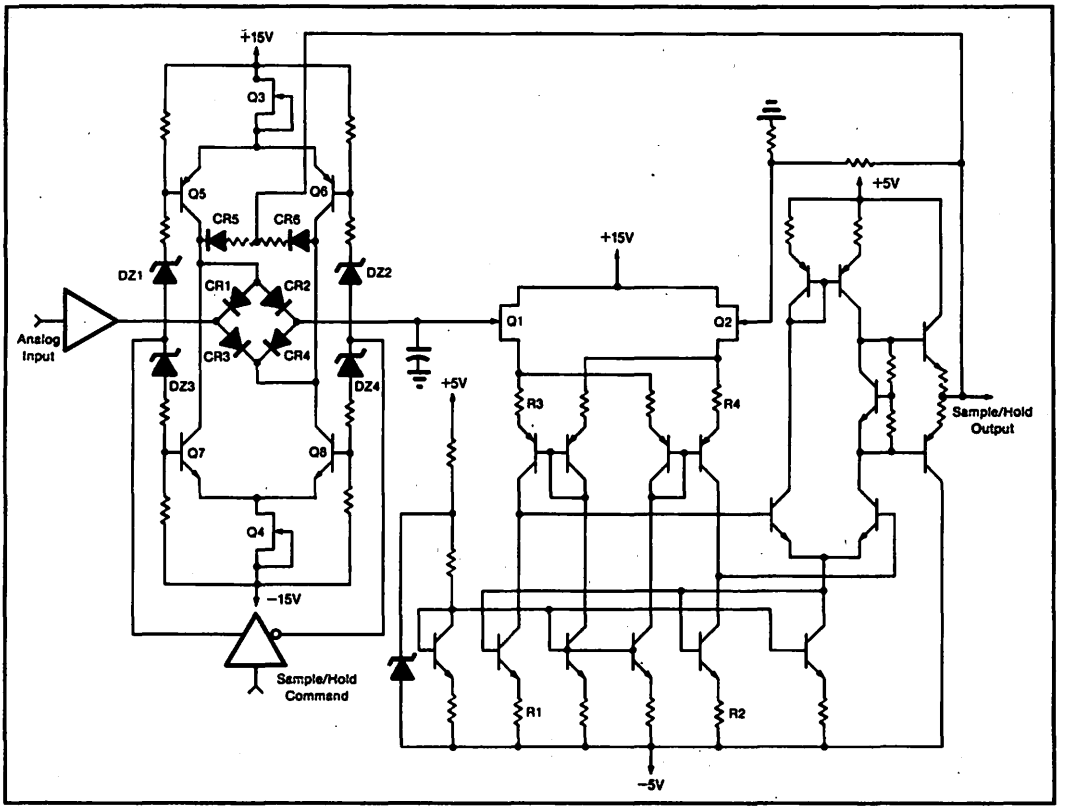


FIGURE 5. Schematic of Sample/Hold SHC600.

level. An ECL signal is coupled to switching transistors Q5 through Q8 through matched level translating zener diodes DZ1 through DZ4. The sampling bridge is isolated from the analog input signal by a high-speed open-loop buffer. To obtain the optimum mix of manufacturing simplicity and circuit performance, the sample/hold employs a thin-film-on-ceramic substrate. Thin film resistors are capable of being laser trimmed, which is required to achieve low values of voltage and pedestal offset in addition to 0.1% gain accuracy.

TABLE II. Characteristics for High Speed Sample/Hold SHC600.

Acquisition Time (2V step): to ±1.00%	20ns
to ±0.10%	30ns
to ±0.01%	40ns
Sample-to-Hold Settling (to 1mV)	12ns
Sample-to-Hold Transient	12mV
Aperture Delay Time	6ns
Aperture Uncertainty	5ps
Slew Rate	±300V/μs
Small Signal Bandwidth	70MHz
Harmonic Distortion (2V p-p at 5MHz)	−70dB below full scale
Hold Mode Feedthrough Rejection (at 1MHz)	62dB
Output Current	50mA
Output Impedance	0.25Ω
Noise (BW = 5MHz)	50μV
Power Dissipation	1.3W

7-Bit Encoder—The 7-bit encoder is formed by parallel connecting two 6-bit ECL flash encoders. See Figure 6 which depicts how this is done. The encoders that process the most significant bits and the least significant bits are substantially the same. The MSB encoder has an attenuator of 0.5 in front of the actual encoder to interface properly with the sample/hold. The input 100Ω resistors, in the MSB encoder, form an attenuator, reducing the input voltage swing to 1.25V. Each encoder accepts a 10V reference signal from the DAC module. IC1 buffers the reference, applying it to the flash encoder as the positive reference voltage. This same voltage is also applied to a unity gain inverter, IC2, which supplies its output to the flash encoders as the negative full-scale reference voltage. Offset adjustment is achieved by trimming either R3 or R4. Adjusting these resistors compensates for the difference in ladder impedance that may exist between the two 6-bit flash encoders that comprise the 7-bit encoder. If left uncorrected, this difference in ladder impedance creates an offset. 22ns after the trailing edge of the strobe, output data is presented to the DAC and to the digital error corrector for further processing.

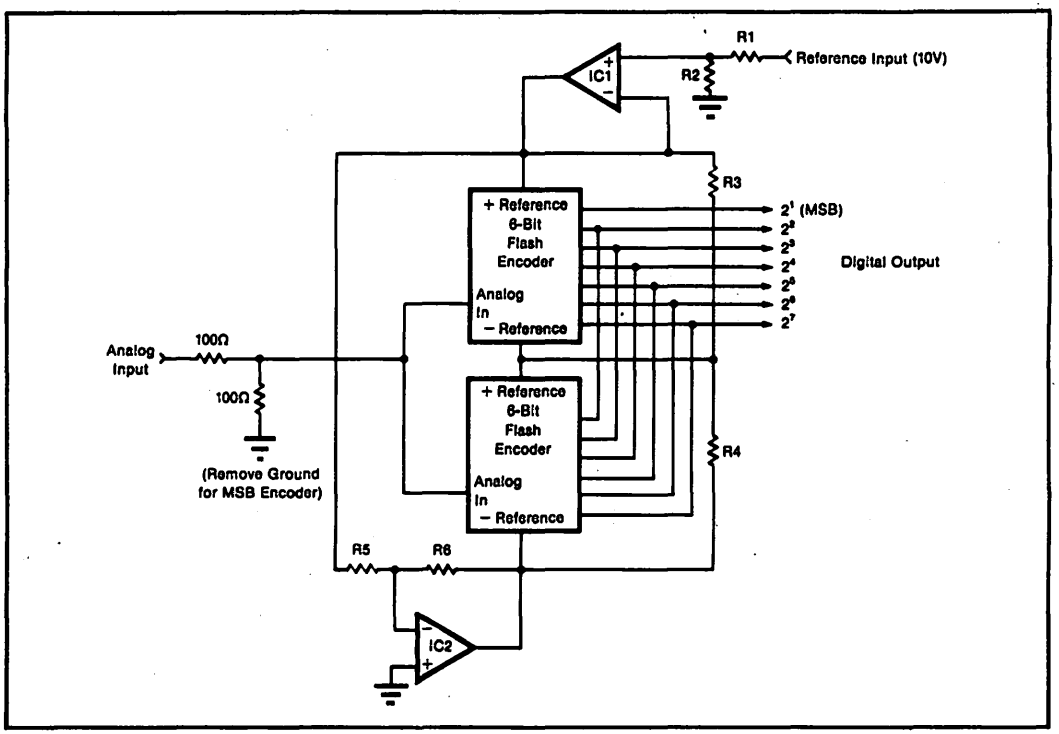


FIGURE 6. 7-Bit Flash Encoder.

Digital-to-Analog Converter/Amplifier Module—This module contains four main sections: a DAC, a reference generator, an input switch, and an output amplifier. The DAC accepts as its input the output from the MSB flash encoder. The DAC is capable of settling to 14-bit accuracy in 25ns in response to full scale input changes. The weighting of each bit current is determined by the feedback action of op amp IC2 (see Figure 7) on the current sources whose collectors are connected to the emitters of the actual switching pair. IC2, in conjunction with resistor R1 and transistors Q3 and Q4, establishes the correct operating conditions so that the reference current of 1.5mA that flows through R3 is created in each of the bit switches. A greater degree of accuracy is maintained by passing only the lower order bit inputs through the ladder. The MSB current is created by placing four switches in parallel, while the second MSB has two switches in parallel and the third MSB is a single switch. The remaining 4-bit currents are passed through the R-2R ladder to binarily weight the other current sources. The reference voltage is created by the circuitry associated with op amp IC1. Transistors Q1 and Q2 are used to isolate the offset current that flows through R4 from IC1. This is done to prevent the changing DAC or sample/hold signal from feeding back into the reference. This offset current is necessary to create a bipolar DAC voltage to match the bipolar sample/hold output. The reference circuit supplies a 10V output that is used for the rest of the system along with a 1.5mA current that is used by the DAC.

The residue or difference signal is created by resistively subtracting the DAC output from the sample/hold input. Before the difference is amplified, it is passed through a network of FETs to prevent the amplifier from overloading during the period of time when the sample/hold is processing new data and the MSB encoder output has not been updated yet. Figure 3 shows a timing diagram illustrating the period of time when the potential for overloading the amplifier exists. When the sample/hold begins to acquire the next analog sample, the MSB flash encoder still has its output latched with the analog data from the previous sample. Therefore, for a period of time extending from the beginning of the sample/hold acquisition time to the time when the digital output of the MSB flash encoder has been updated, the potential for overloading the amplifier exists. The amplifier is prevented from overloading by switching FET Q5 off and FET Q6 on. This places the amplifier output at 0V, which is optimum to allow the shortest settling time to the next value. The state of switches Q5 and Q6 is reversed after the MSB encoder is strobed, and the latched encoder output is then available as the digital input to the DAC. The difference between the sample/hold and DAC output is amplified by a low drift gain-of-32 amplifier with a 65MHz bandwidth. The combination of low drift and wide bandwidth is achieved

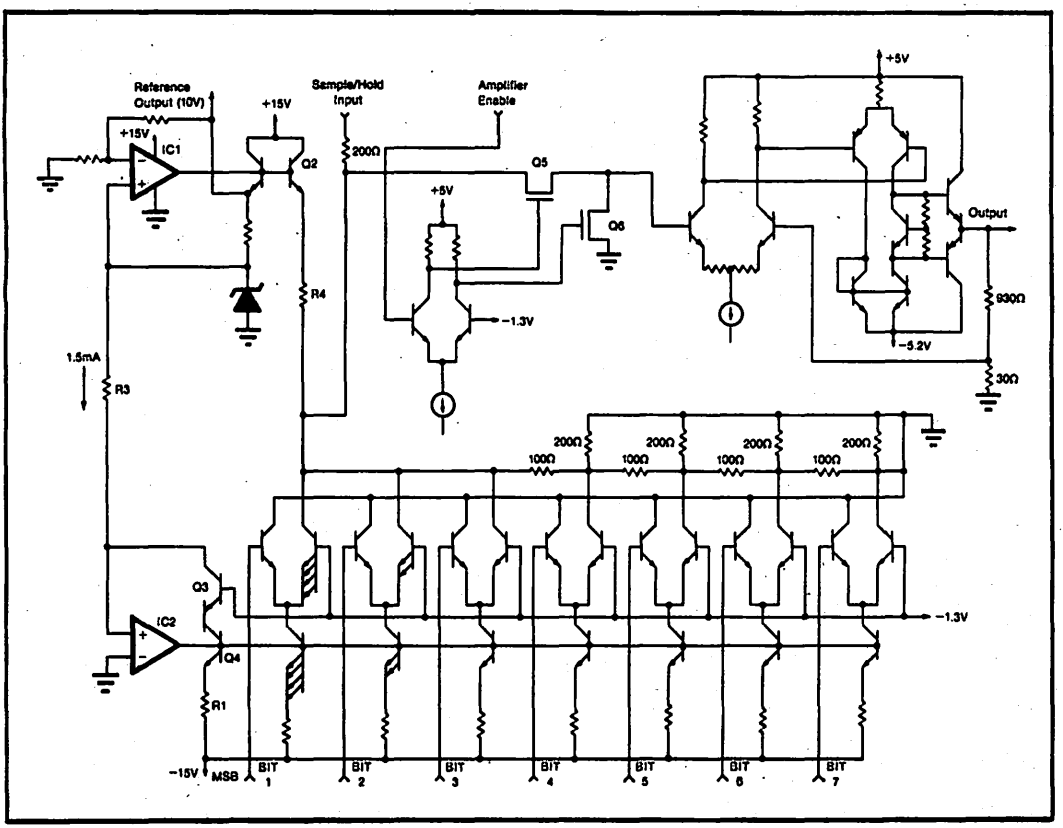


FIGURE 7. Schematic of DAC/Amp Module.

by using a monolithic front end with 3GHz transistors and 5GHz NPN and PNP transistors for the remainder of the amplifier.

Timing Module—The timing module supplies all the critical timing signals necessary for the operation of the ADC. Several noncritical timing signals are generated in the Digital Error Correcting Module. The circuitry within the timing module is designed so that both the delay and the pulse width of each timing signal are capable of being laser trimmed to a pre-set standard. The delay stability of ECL logic is adequate to generate the necessary timing signal as a combined tolerance of 2% over a 35°C change in temperature and a 5% change in power supply value is achievable. Timing signals are derived by using the output of a three-stage shift register to create unique points in time from which the actual signals can be derived. A synchronized 20MHz oscillator is used to drive the shift register.

Figure 8 shows a simplified schematic of the timing module. The Convert Command Signal is differentiated by IC1 to allow pulses ranging from about 5ns up to a 75% duty cycle as triggers to the ADC. This differentiated signal sets flip-flop IC2, which simultaneously releases the shift register from the reset state, starts the 20MHz oscillator, and is also used to generate the Sample/Hold gate. The other input to IC3 is the output from IC1. This is done to reduce the aperture delay of the system as the output of IC3 is used to place the Sample/Hold in the hold mode at this time. The output of the last stage of the shift register resets flip-flop IC2, which in turn places the Sample/Hold back in the sample mode. The output of the third stage of the shift register is also used as the input to generate the strobe for the LSB flash encoder. IC8 forms a differentiator with R1 and C1. R1 is capable of being laser trimmed so that a precise 8ns pulse is generated. The frequency of the clock ocsillator is adjusted to trim the delay of this strobe pulse. IC4 and IC5 comprise the principal elements of a ring oscillator. R2 and C2 form an additional delay so that when R2 is laser trimmed, the LSB delay can be precisely determined. Amplifier Enable, a signal which is used to switch the input of the final amplifier between its two modes of operation, is generated at the output of the second stage of the shift register. This adjustmet is accomplished by adjusting R3 along with C3, which forms a delay element along with two gates from IC6.

The final signal that is created by this module is the MSB strobe. This signal is generated from the Sample/Hold signal. Provision is made for adjusting the delay and pulse width using techniques previously discussed. It

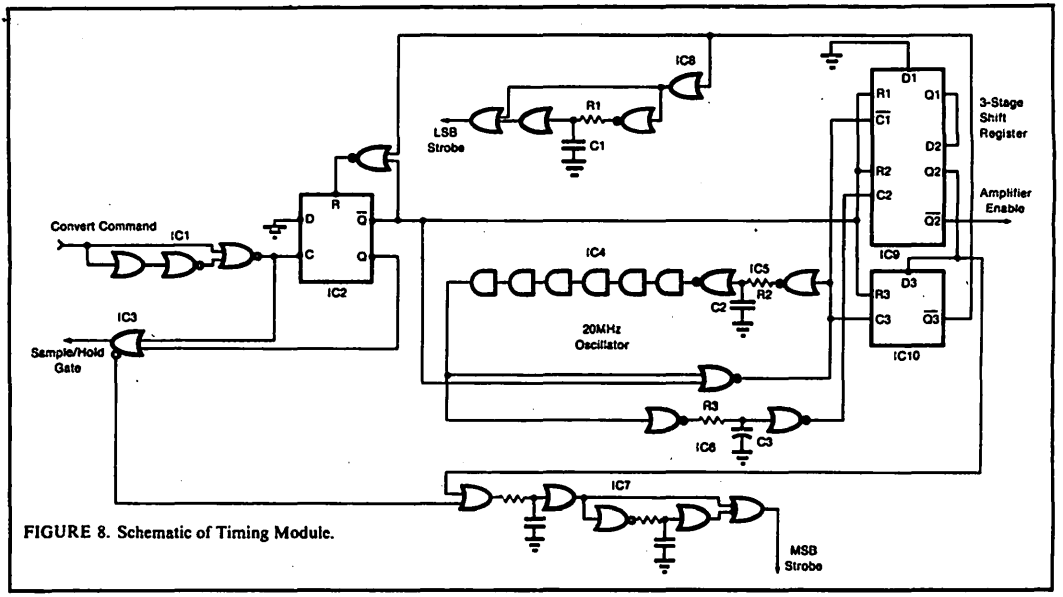


FIGURE 8. Schematic of Timing Module.

should be noted that the width of the Sample/Hold gate is not fixed, but is determined by the difference in time betwen the ADC conversion time, which is fixed at 67ns, and the overall system conversion rate, which is determined by the application. Therefore, ADC conversion rates in excess of 10MHz are achievable, but at the expense of reducing the acquisition time of the Sample/Hold.

Digital Error Corrector Module—The function of the Digital Error Corrector Module is to assemble the 7-bit words from the two flash encoders into the final 12-bit output word. Figure 9 shows a block diagram of this module. In addition, the Error Corrector Module takes the LSB flash encoder strobe and generates the timing strobes for the data registers that are located within this module. A Data Valid pulse is also generated which is used to indicate when the data output can be read into an external register. This pulse comes 5ns after data is present to assure sufficient set-up time for external latch. The output of the MSB encoder is read into a separate

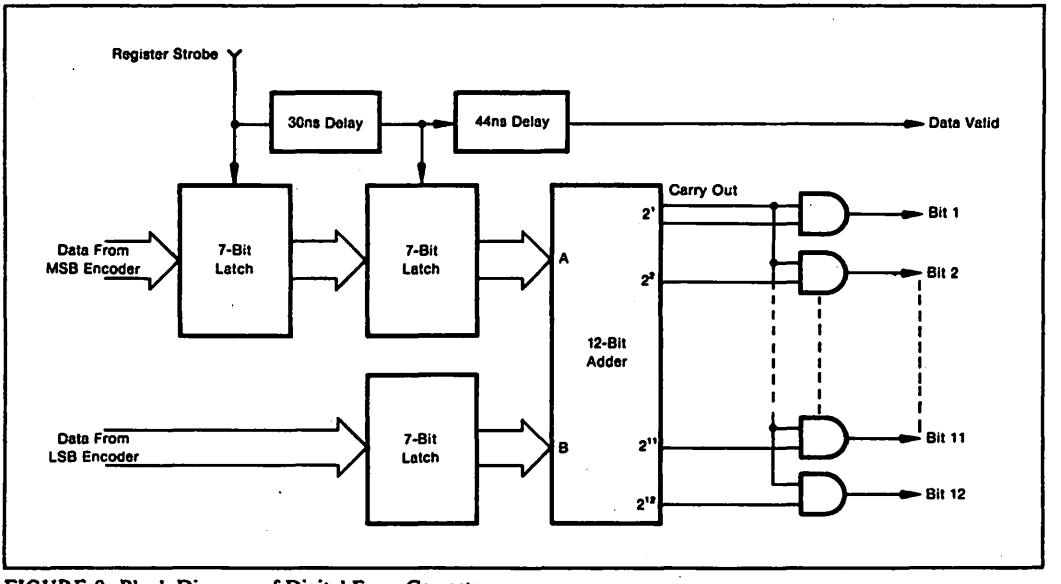


FIGURE 9. Block Diagram of Digital Error Corrector.

7-bit latch at the same time the LSB encoder is being strobed. The output of the latched MSB data, along with the LSB data, is then read into a 14-bit latch 30ns after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. This latch eliminates any critical timing problems that would result when the ADC is operated at its maximum rate. Examination of the system timing diagram, Figure 3, shows that there is inadequate time for the adders to process both encoder outputs. The system of latches eliminates this problem by extending the period of time when both inputs to the adder are present, from 22–68ns.

The output of the register is then sent to a 12-bit adder where the final output word is created. The MSB data is treated as the most significant 7 bits of a 12-bit word, with the last 5 bits being assigned zeroes. In a similar fashion, the LSB data from the least significant bits form the other input to the adder with the first 5 bits being assigned zeroes. Since two 12-bit words are being added, the output of the adder could exceed 12 bits in range; however, the final output is only a 12-bit word, so means must be provided for detecting the presence of the range being exceeded. If the input analog range is exceeded, the desired output should be all ones. Since the 13th bit could go to a one, for the MSB, the lower 12 bits could roll over back to zeroes, thereby creating a false output. To prevent this from happening; the carry-out of the 12th bit is detected and used to assert all ones at the output. The final output ranges from all zeroes (which corresponds to minus full scale) to all ones (which corresponds to plus full scale).

TEST RESULTS

The characteristics of the ADC were experimentally verified using two principal test techniques—histogram and spectrum analysis testing. The histogram test was conducted at both 200Hz and 4.9MHz, the latter being near the Nyquist rate of 5MHz. The performance of a typical ADC600 is shown in Figure 10. A block diagram of the test system used to determine the histogram is shown in Figure 11. Note that both at 200Hz and at 4.9MHz, the typical differential non-linearity is 0.5LSB.

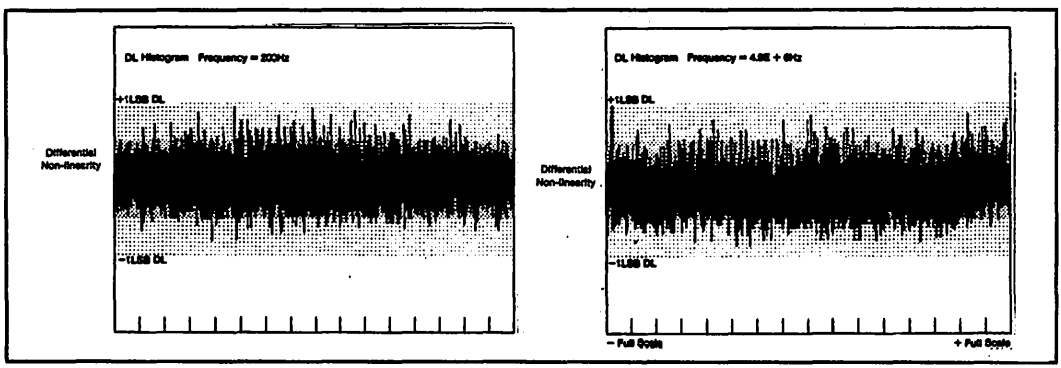


FIGURE 10. Histogram Test Results.

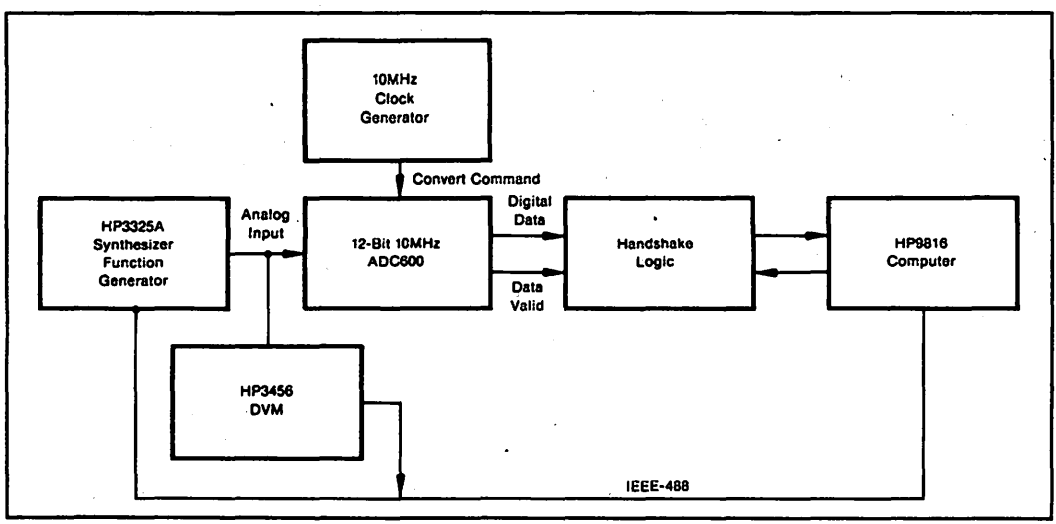


FIGURE 11. Block Diagram of Histogram Test.

There are no missing codes present and the peak differential nonlinearity does not exceed 1LSB. Histogram testing is a very useful performance indicator as the width of all the codes can be rapidly determined. The test system shown in Figure 11 conducts a 100,000-point test in two minutes. A faster version of this test, being more hardware-oriented, is predicted to take 15 seconds.

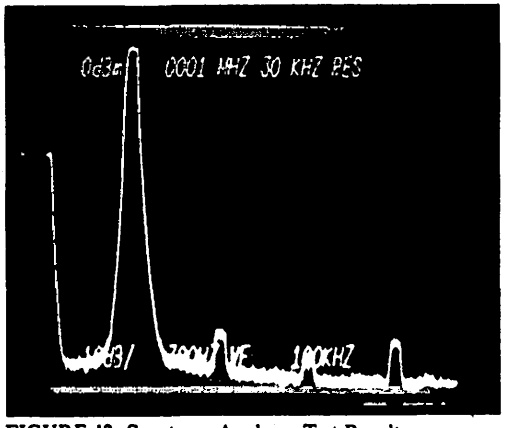


FIGURE 12. Spectrum Analyzer Test Results.

Results of the spectrum analyzer test are shown in Figure 12, with the block diagram of this test system shown in Figure 13. The input test signal was at 4.8MHz to test the 10MHz converter at close to the Nyquist rate. The ADC600 output was demodulated at a 5MHz rate to provide a spectrum analyzer display with greater frequency resolution. With this "beat frequency technique," the effects of the tester's DAC settling and glitches are minimized, as the difference frequency of 200kHz is displayed in place of the actual signal frequency of 4.8MHz. Demodulating the signal at one-half the sample rate still maintains the correct relationship of the harmonics to the fundamental. Only the frequency has been shifted. The harmonic generation of the ADC is estimated to be at least 70dB below the fundamental for a full-scale input signal.[1]

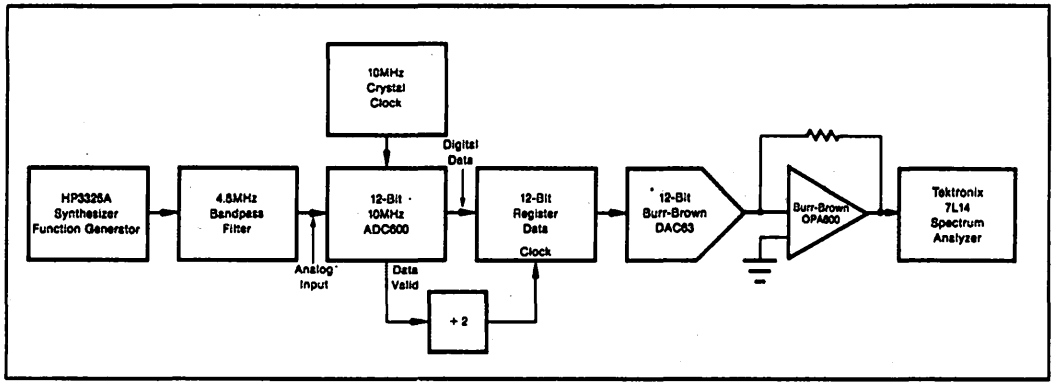


FIGURE 13. Block Diagram of Spectrum Analyzer Test.

NOTE:
1) Additional FFT Spectral information can be found in *Test Report: FFT Characterization of Burr-Brown ADC600K.* Published by Signal Conversion Limited, Swansea, Wales, U.K., February, 1987. Copies available upon request.

GAIN BLOCK REALIZATION USING INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers such as Burr-Brown's INA110 display characteristics which recommend their use as gain blocks instead of conventional operational amplifiers and external networks to achieve better performance or easier design. Some general considerations and specific examples are given.

In the initial stages of system development, circuit functions are defined at the functional or block diagram level. Gains, scaling, signal voltage levels, and circuit functionality are the prime concerns during this phase of the design development. Once this set of considerations is met and the conceptual design accepted and approved, the process of functional realization begins.

When choosing the design for a fixed-gain amplifier, designers frequently turn to discrete solutions using operational amplifiers. This process begins with the choice of a circuit configuration and device(s) whose gross characteristics show promise of meeting the design requirements set forth in the conceptual stage. It ends with a bottom-up design of the gain block, using uncommitted operational amplifiers and external networks. While this approach yields a workable solution, it consumes valuable design effort and overlooks the benefits of the class of solutions offered by certain monolithic instrumentation amplifiers.

These benefits fall into four broad categories: performance, size, simplicity, and cost.

Performance

When very good DC performance is needed and speed requirements increase, the choice of operational amplifiers displaying the desired characteristics quickly diminishes. This fact forces compromise in one or more key parameters or requires external circuitry to compensate for amplifier deficiencies. By combining DC performance* and high speed operation** in a single IC package, the instrumentation-amplifier approach avoids these design compromises.

Size

Additional board space is required to accommodate external gain-setting networks. Use of a single instrumentation amplifier containing all gain-setting resistors in a single package, especially one available in an SOIC configuration, minimizes the space used and allows for more efficient layouts. Power can be an important consideration in high-density boards. Frequently, a single instrumentation amplifier will consume less power than a discrete design of comparable performance.

Simplicity

By using the internal gain-setting networks of an instrumentation amplifier, the designer is freed from the many complications of using external feedback components. Temperature-tracking of external components and thermoelectric effects typically limit the DC performance of operational amplifier circuits. To achieve specified settling times and assure stability, operational amplifier designs often require tailoring of the AC feedback path with additional external capacitors. In some applications, high input impedance requirements force choices of circuit configuration and/or discrete circuit values. These values may be impractically high in a discrete design and contribute to input circuit noise or DC errors, while the circuit configurations may require extra active devices to overcome the limitations of single operational amplifier designs. These sources of difficulty are avoided when an instrumentation amplifier such as the INA110 is used instead of the operational amplifier and its external parts.

Ground-loop currents can also be troublesome sources of error in operational amplifier circuits. Instrumentation amplifiers are designed to exhibit very high rejection of input errors common to both inputs. This characteristic can simplify circuit board layout and improve the probability of moving from breadboard to final design without significant redesign.

Cost

Monolithic instrumentation amplifiers such as the INA110 are priced competitively with single high-performance operational amplifiers, yet do not require the external and frequently expensive precision components to achieve fixed, precision gains. Gains are instead set with internal networks which have been laser-trimmed to very exacting standards and do not require adjustment or selection at board level to achieve specified performance. In addition to the savings in direct component and labor costs, the instrument amplifier approach frequently avoids use of a second device and saves on-board real estate, power-

*Gain accuracy of 0.1%, gain tempco = 20ppm/°C, V_{os} drift = 2.5μV/°C
**Settling time to 0.01% = 4μs

bypassing components, and power supply requirements.

The circuits illustrated in Figures 1 through 6 show some of the performance tradeoffs and benefits in using the instrumentation amplifier as a gain-block element. The following assumptions were used to develop the data accompanying each circuit. Gain is 100V/V; all resistors are 1% tolerance and 50ppm temperature coefficient; source impedance for the signal source is zero. Operational amplifiers are realistically chosen for the applications. The circuits are common operational amplifier configurations and show how certain deficiencies in these circuits might be designed around. Each is shown beside the equivalent IA implementation and pertinent performance comparisons for the two designs are listed. For the reader's convenience, some key INA110 specifications are also given in Table I.

Figure 1 shows a simple inverting amplifier. Note the improvements in gain-related errors, input impedance, and settling time. Figure 2 shows an operational amplifier approach to improve input impedance. Ths design, using an additional op amp and discrete components to achieve the impedance improvement, does offer some improvement over the IA implementation in input offset and offset drift. It also offers a longer settling time and poorer gain error performance at much increased cost.

Figure 3 shows a noninverting configuration offering high input impedance. It offers slightly better input offset characteristics than the IA but poorer gain error and longer settling time than the IA design.

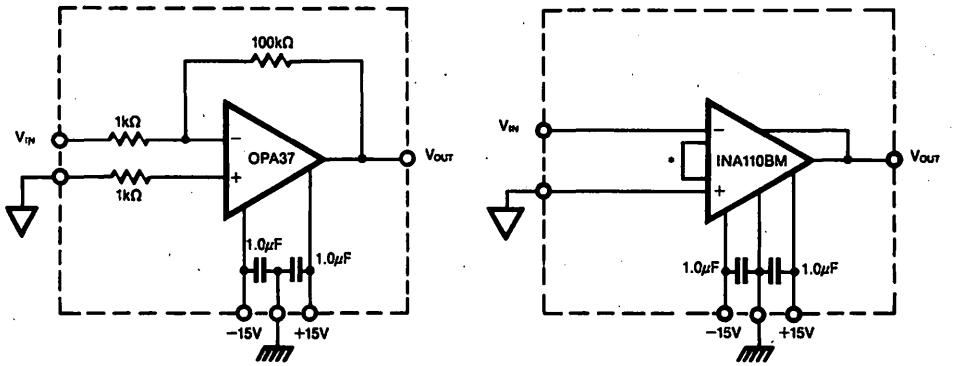
TABLE I. Key INA110 Specifications.

(Gain = 100, T_A = +25°C, ±V_{CC} = 15VDC)	
V_{OS}	280μV, max
V_{OS} versus Temperature	2.5μV/°C, max
I_B	50pA, max
Input Noise Voltage	10nV/√Hz
Gain Error	0.1%, max
Gain versus Temperature	20ppm, max
Nonlinearity	0.01%, max
CMR, 1kΩ Source Imbalance	100dB, min
Gain-Bandwidth Product	47MHz
Slew Rate	17V/μs
Settling Time to 0.1%	3μs
to 0.01%	4μs
Total Harmonic Distortion plus Noise	
V_{OUT} = 6.5Vrms at 1kHz	0.003%
V_{OUT} = 6.5Vrms at 20kHz	0.017%
Supply Current	3mA
Power Dissipation	90mW

Figure 4 illustrates two approaches to differential amplifier design. Because the IA is specifically designed to handle differential signals, it is not surprising that its performance is generally better than the op amp design. What is often overlooked is the superior high-frequency behavior of the IA with respect to CMR. This arises from two factors. First is the initially higher CMR of the IA. Second is the intrinsic effects of stray circuit elements on the final design. The curve given in Figure 4 contrasts the frequency dependence of CMR for the IA and for two values of stray capacitance in the feedback path. This is a simple example, using only one of the several capacitances which exist, but illustrates the dramatic improvements available using the INA110.

Figure 5 is an AC-coupled inverter with a −3dB cutoff at 1Hz. Owing to the high cost and space penalties of large-value capacitors, it is common to limit the capacitor to a smaller value. This requires a high impedance device. Frequently the input impedance problem is addressed with use of a unity-gain buffer. The cost of this additional amplifier must include board space, power, and feedback and bypass component costs. The low value of cutoff frequency and small capacitor values also require larger values of input resistance. As shown in the figure, this has a disastrous effect on the offset and offset drift of the amplifier. Coupled with the high gain of the amplifier, the output offset voltage will be unacceptably high. Overall, the IA design provides a cleaner solution.

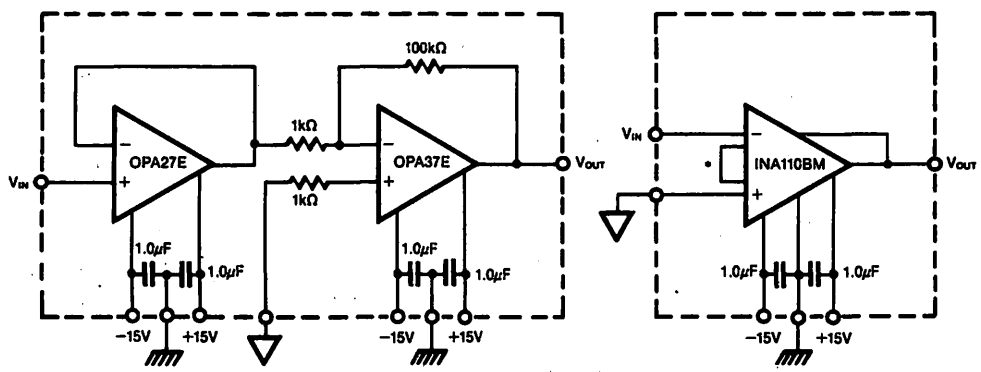
Figure 6 illustrates an attempt to deal with the DC problems encountered in Figure 5. It substitutes a premium FET input (and higher cost) op amp for the industry-standard OPA37E used in Figure 5. This choice improves the DC performance of the op amp implementation, but still does not equal the performance of the IA design, and exhibits a longer settling time than the IA. An additional subtlety arises in this circuit. Like some other premium devices, the OPA111 has a lower output drive capacity than the OPA37E. Thus, the designer was forced to raise the resistance values in the feedforward and feedback paths of the second stage. This imposes a greater sensitivity to parasitic capacitances. Frequency response, which had been better than the IA circut, now is sensitive to these capacitances. The curve in Figure 6 shows this sensitivity for two different values of C_{STRAY} in the feedback path of the second stage. Should similar parasitics exist in the feedforward path, excessive frequency peaking could occur.



*Pin-strapped for $A_V = 100$

	Op Amp Design	INA110 Design
Gain	100	100
Gain Error	2%	0.1%
Gain Tempco	100ppm/°C	20ppm/°C
V_{OS}	60μV	280μV
V_{OS} Drift	1.5μV/°C	2.5μV/°C
Gain Bandwidth	50MHz, typ	47MHz, typ
Settling Time (0.01%)	25μs, typ	4μs, typ
Input Impedance	1kΩ	∞

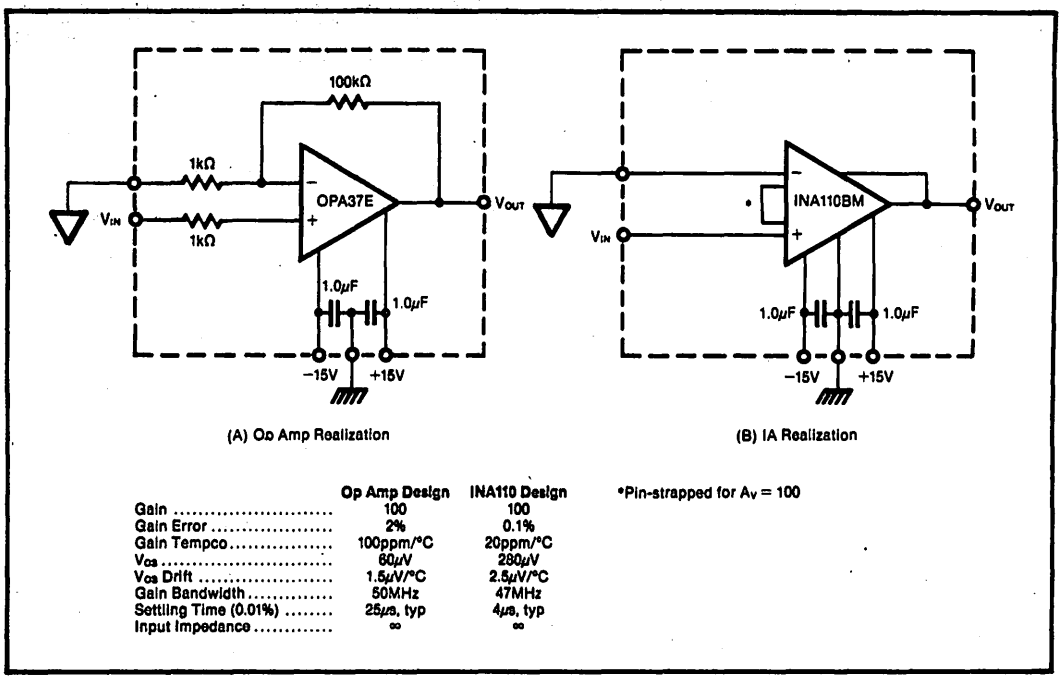
FIGURE 1. DC-Coupled, Inverting Amplifier.



*Pin-strapped for $A_V = 100$

	Op Amp Design	INA110 Design
Gain	100	100
Gain Error	2%	0.1%
Gain Tempco	100ppm/°C	20ppm/°C
V_{OS}	85μV	280μV
V_{OS} Drift	2.1μV/°C	2.5μV/°C
Gain Bandwidth	50MHz, typ	47MHz, typ
Settling Time (0.01%)	35μs, typ	4μs, typ
Input Impedance	∞	∞

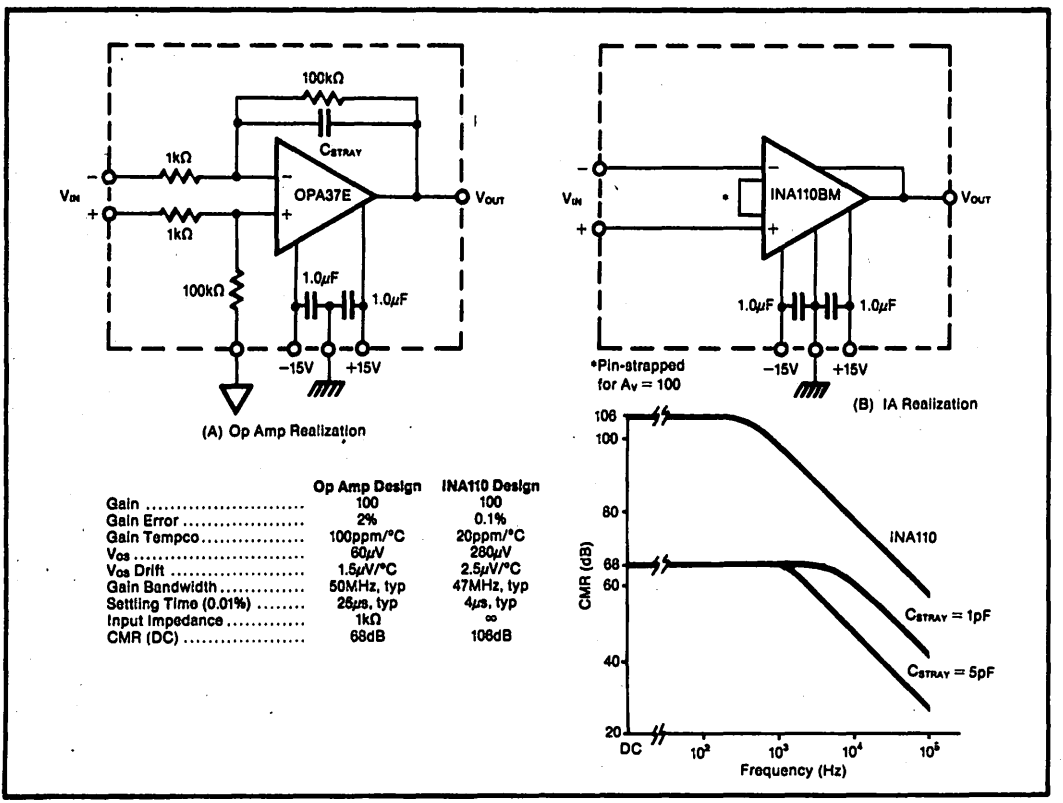
FIGURE 2. DC-Coupled, Inverting Amplifier with Unity-Gain Impedance Buffer.



	Op Amp Design	INA110 Design
Gain	100	100
Gain Error	2%	0.1%
Gain Tempco	100ppm/°C	20ppm/°C
V_{OS}	60μV	280μV
V_{OS} Drift	1.5μV/°C	2.5μV/°C
Gain Bandwidth	50MHz	47MHz
Settling Time (0.01%)	25μs, typ	4μs, typ
Input Impedance	∞	∞

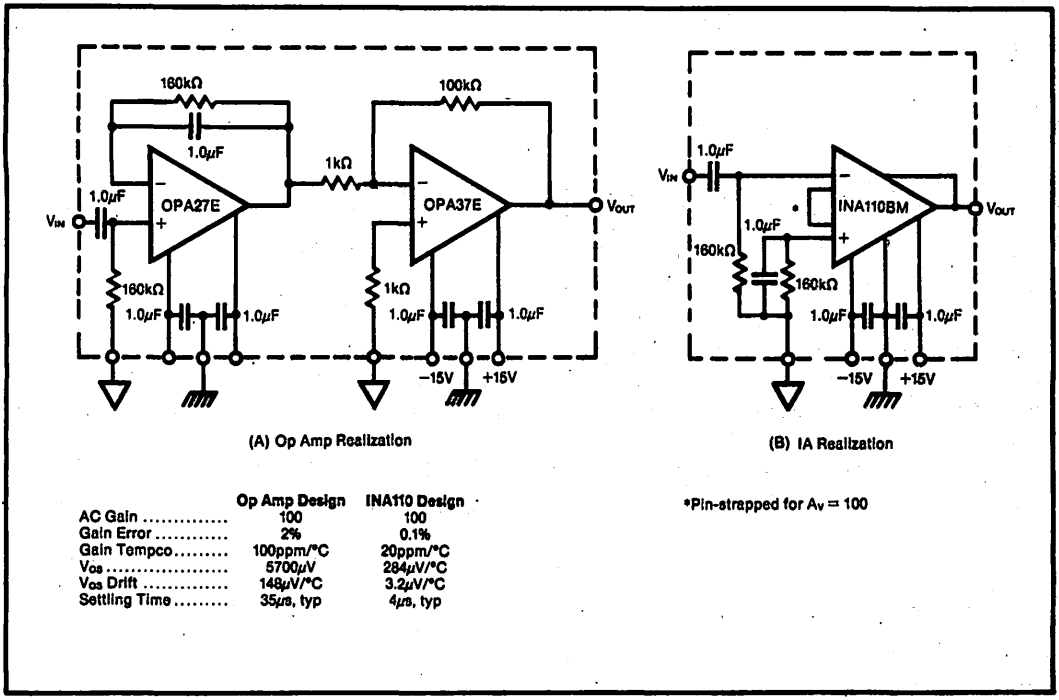
*Pin-strapped for $A_V = 100$

FIGURE 3. DC-Coupled, Noninverting Amplifier.



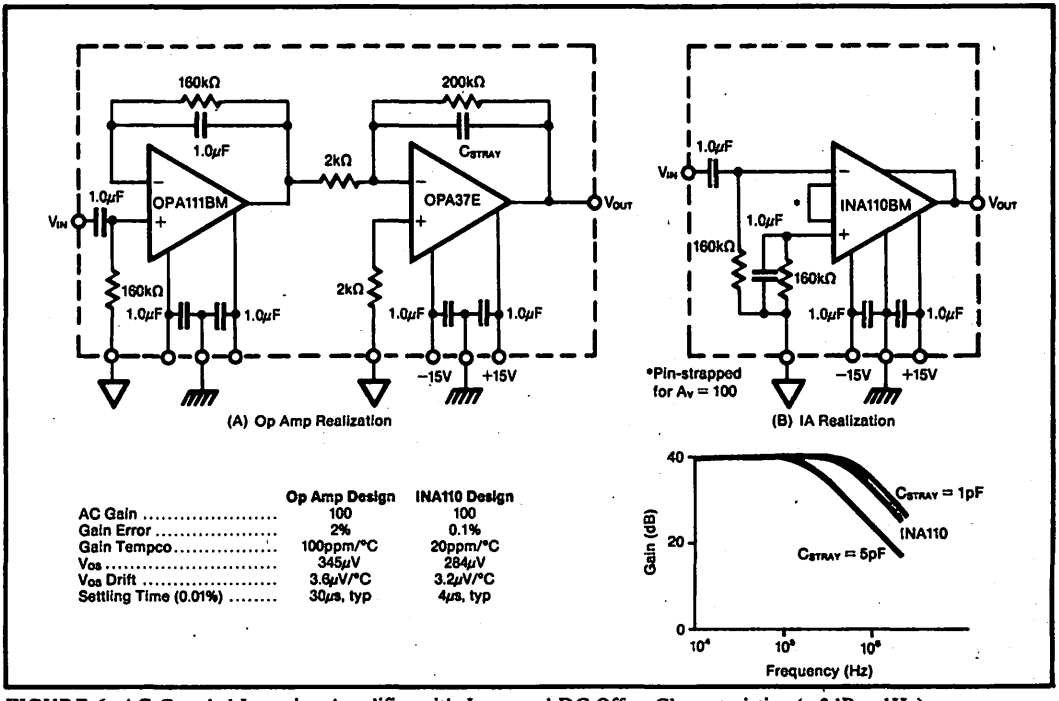
	Op Amp Design	INA110 Design
Gain	100	100
Gain Error	2%	0.1%
Gain Tempco	100ppm/°C	20ppm/°C
V_{OS}	60μV	280μV
V_{OS} Drift	1.5μV/°C	2.5μV/°C
Gain Bandwidth	50MHz, typ	47MHz, typ
Settling Time (0.01%)	25μs, typ	4μs, typ
Input Impedance	1kΩ	∞
CMR (DC)	68dB	106dB

FIGURE 4. Differential Amplifier.



	Op Amp Design	INA110 Design
AC Gain	100	100
Gain Error	2%	0.1%
Gain Tempco	100ppm/°C	20ppm/°C
V_{OS}	5700µV	284µV/°C
V_{OS} Drift	148µV/°C	3.2µV/°C
Settling Time	35µs, typ	4µs, typ

FIGURE 5. AC-Coupled Inverting Amplifier (−3dB = 1Hz).



	Op Amp Design	INA110 Design
AC Gain	100	100
Gain Error	2%	0.1%
Gain Tempco	100ppm/°C	20ppm/°C
V_{OS}	345µV	284µV
V_{OS} Drift	3.6µV/°C	3.2µV/°C
Settling Time (0.01%)	30µs, typ	4µs, typ

FIGURE 6. AC-Coupled Inverting Amplifier with Improved DC Offset Characteristics (−3dB = 1Hz).

INSTRUMENTATION AMP ADDRESSES POWER-MISER CIRCUIT APPLICATIONS

For many applications, designers are now demanding greater IC performance at lower supply-voltage and -current levels. One monolithic instrumentation amplifier can help satisfy these needs. It's an easy-to-use, self-contained precision gain block that can address isolation and other problems.

Designers can take advantage of the high performance available in the INA102 monolithic instrumentation amplifier to handle a host of applications where low power consumption is critical. Typical examples of such applications include remote monitoring stations powered by batteries or solar cells, mobile battery-powered circuits, medical instrumentation, remote transducer amplifiers, pulsed control systems, and data acquisition systems.

Solving Isolation Problems

Figure 1 shows several designs that exploit the INA102's low current requirements to achieve high-performance isolated data acquisition. **Figure 1a** shows a generic data acquisition circuit in which the INA102 interfaces directly with a 3656 module, a unit that combines an isolation amplifier with an isolated switch-mode power supply. The transformer-coupled 3656 features a continuous isolation-voltage rating of 3500VDC.

In **Figure 1b's** circuit, a separate minisupply drives an 8-channel system. Power requirements for the circuit's CMOS multiplexer are minimal, and the OPA21 op amp draws less than 300μA. The ISO100 isolation amplifier requires only 75mW, so total power drain on the isolated power supply is only 325mW. The PWR105 DC/DC converter operates with a 5V input and delivers ±15V at 15mA per channel. The ISO100 employs optical coupling. Its peak continuous isolation-voltage rating is only 750V, and it is not as expensive as the 3656. The circuit shown in **Figure 1c** satisfies applications specifically involving digital signals. The desired channel signal feeds a voltage-to-frequency converter. The V/F converter's output signal is a series of pulses, each of which has a period that's proportional to the input signal. Typically, these pulses are fed to a gated counter to retrieve the original input value.

Although **Figure 1c's** circuit employs a PWR105 isolated power supply, the output power is a function of the V/F converter you use. If you elect to use the system clock to drive the V/F converter, you can use a VFC100. In this case, you'll need an additional digital optical coupler to drive the VFC100's clock input. If synchronization isn't a major concern, you can use a converter like the VFC32. In either case, the full-scale frequency (dynamic range) is dependent on the speed of the optocouplers.

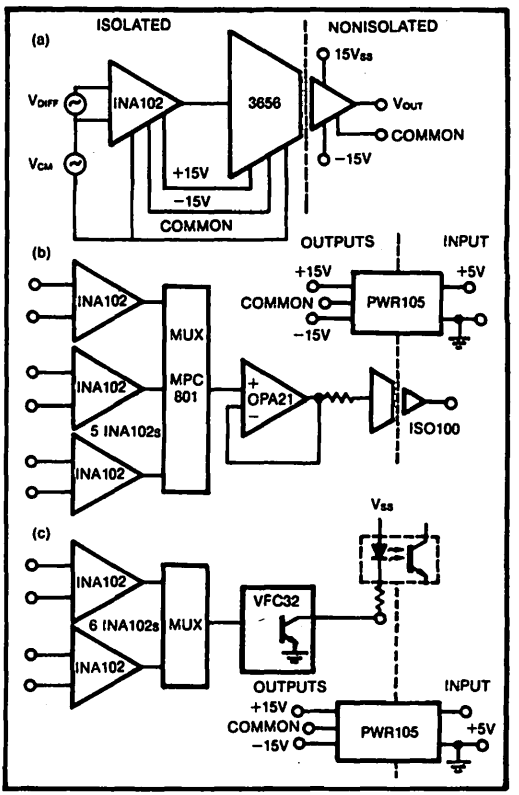


FIGURE 1. You can achieve high-performance isolated signal acquisition by exploiting the INA102's low current requirements. You can interface the INA102 directly to an isolation amp (a) or an 8-channel CMOS multiplexer (b). Another circuit (c) provides an easy technique for analog-to-digital conversion.

A variety of designs can exploit the INA102's low-current requirements to achieve high performance in isolated data acquisition circuits.

If high performance isn't a prime design parameter, you can develop an inexpensive but effective isolation amplifier by modulating the current in an optocoupler (Figure 2). In this case, the INA102 operates as a high-side current monitor; it's powered by a miniature switch-mode power supply, and it floats on the high voltage input of a motor-drive circuit.

The high-side current-monitoring concept is important in this design. A sense resistor in the return path (employed in low-side monitoring) would not detect a short from the motor windings to the motor housing, which is usually grounded. If your design employs a 0.01Ω sense resistor, you can read the monitored current directly as the output voltage of the instrumentation amp if the amp's gain is set for 100.

Although the scheme presented in Figure 2 is quite simple, its precision is not very high. Most optocouplers have a linearity error of about 2%. In addition, the output signal will have an inherent midscale offset that isn't well defined unless you do some trimming. This offset does offer one advantage, however: It allows you to monitor the negative current pumped back into the power supply by the motor.

No discussion of isolation techniques would be complete without a description of a medical-instrumentation application. Figure 3 illustrates a battery-powered, multichannel EEG system that's clocked by low-power

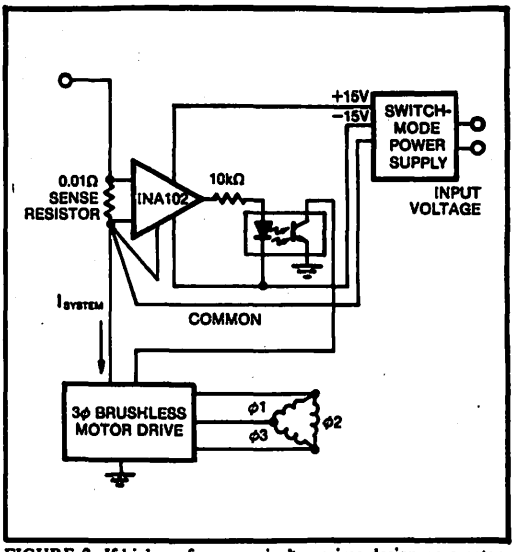


FIGURE 2. If high performance isn't a prime design parameter, you can develop an inexpensive but effective isolation amplifier by modulating the current in an optocoupler.

CMOS circuits. These circuits continuously sweep through the channels. The first channel (pin 4) has a 10kHz square-wave input that identifies channels. This example illustrates a typical application challenge: the measurement of small signals (about 100μV p-p) from high-impedance sources with as much as 1V p-p of a 60Hz common-mode signal. Using 15 INA102s, this circuit will draw only 12mA, including a 1mA current draw for the CMOS circuitry.

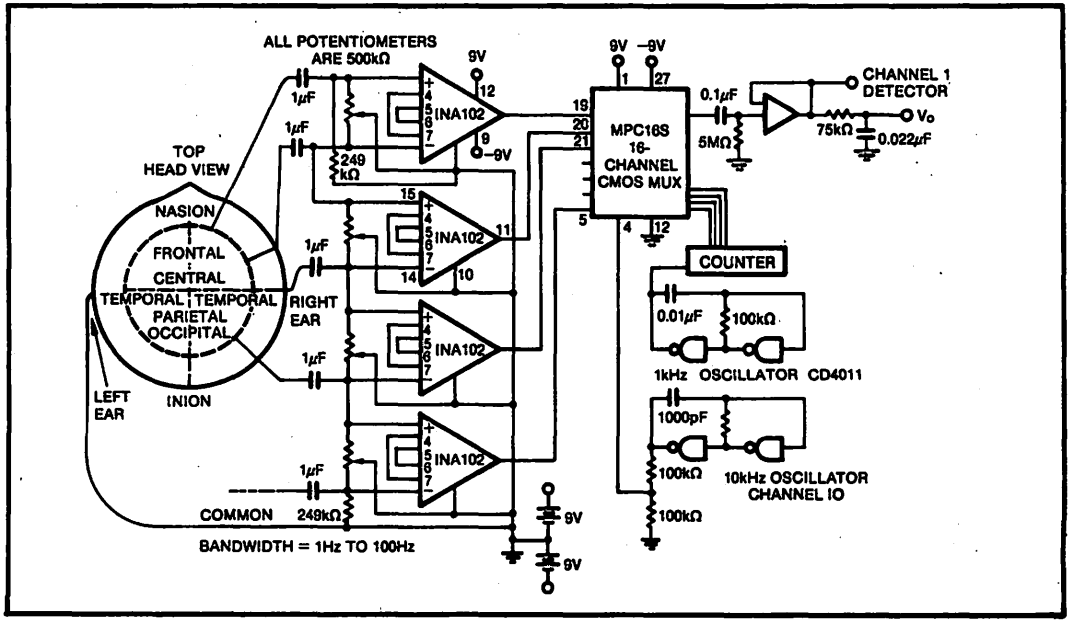


FIGURE 3. In this battery-powered EEG system, low-power CMOS circuits provide the clock function and also continuously sweep through the channels. The circuit employes 15 INA102s and draws only 12mA.

If your isolation design doesn't require very high performance, you can build a suitable isolation amp by modulating the current in an optocoupler.

Save Power In Process Monitoring

Many control schemes don't require continuous monitoring of the process. Samples taken at a regular interval (once per second, per minute, etc.) suffice. You can realize significant power savings by designing a circuit that pulses on for a brief time and then powers down until it's time to take the next sample.

The INA102 is well suited to this type of application. Because of the amplifier's low power requirements, the amount of warm-up heating is very small, and the warm-up time and drift therefore don't compromise performance each time the circuit turns on. Assuming a 70°C/W thermal resistance for a side-brazed ceramic package, the INA102 heats itself less then 2°C, which translates to a worst-case offset warm-up drift of 14μV. Warm-up time is well under 1m. The overall time to acquire a reading after the power comes on will depend on the time constant of the output filter used to set the system bandwidth and on the settling time of the INA102.

Figure 4 shows an example of this type of application. The example could be a handheld instrument with a simple momentary switch to trigger a reading. The two one-shots fire when the switch closes. The first one-shot turns on a pair of CMOS switches; the second triggers the A/D converter to take a reading. After a reasonable amount of time—determined by the warm-up time, the settling time, and the converter's conversion time—the first one-shot turns off. The resulting measurements might go into a memory or to an LCD. Overall time spent in the power-on mode can range from 1 to 10m. At a rate of one sample per second, this circuit can be a real battery saver.

An EEG application illustrates the challenge of measuring small signals from high-impedance sources with as much as 1Vp-p of a 60Hz common-mode signal.

Place Dedicated INA102s Before Mux

The INA102 can also be beneficial in multichannel data acquisition systems by allowing you to achieve higher throughput rates. Standard data acquisition systems generally use a multiplexer, located before the instrumentation amplifier, to monitor several channels. Such design schemes are used to avoid the high costs of using dedicated instrumentation amps on each channel. These costs include the expense of the extra power, the external components, and the extra system board space required to accommodate the dedicated amps.

You can realize a major increase in performance at a reasonable cost by using dedicated INA102s at each

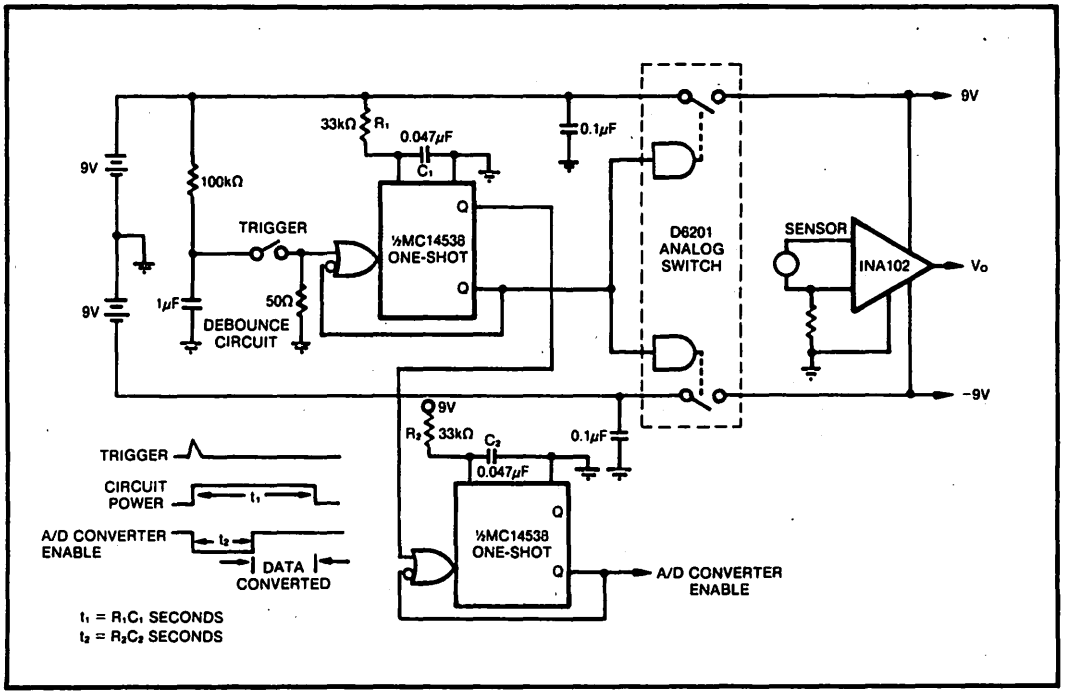


FIGURE 4. To provide significant power savings in process-monitoring applications, this circuit pulses on only when it's time to take a sample measurement.

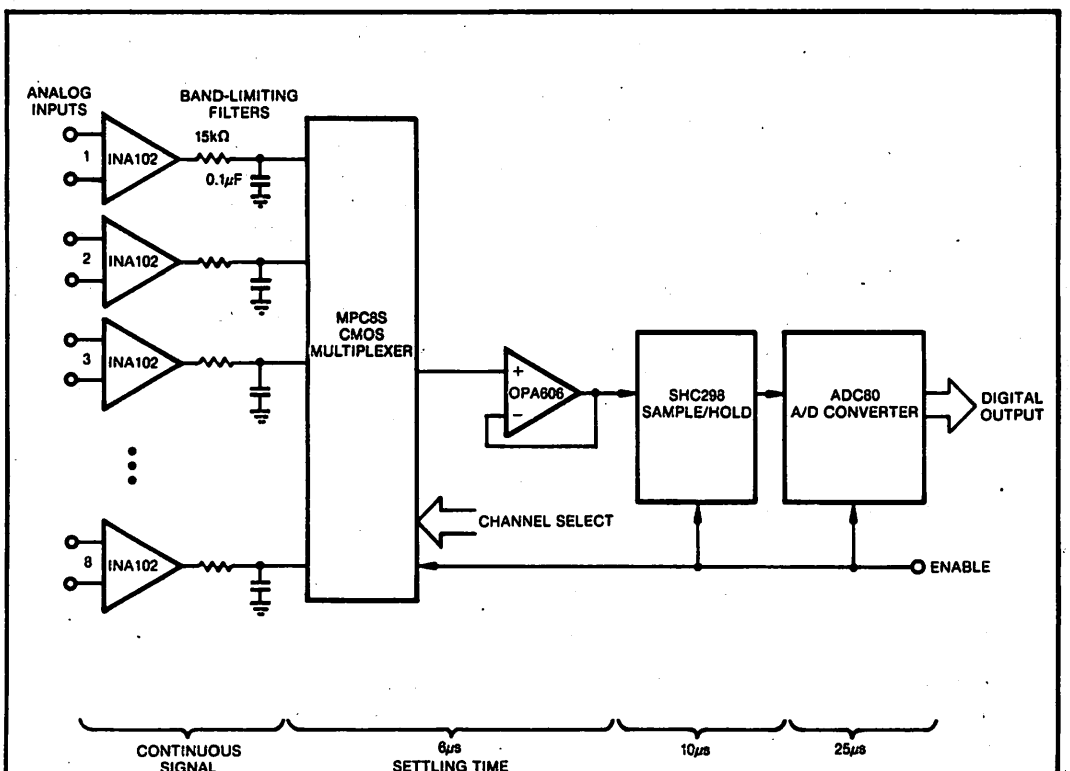
Many control schemes do not require continuous process monitoring; samples taken at regular intervals will suffice.

analog input of data acquisition system (Figure 5). This configuration gives you several dedicated input channels that together require the same power needed to operate one of the older instrumentation circuits. All necessary gain-setting resistors are built in, and users can select the desired gain via jumpers. According to this dedicated concept, the signal is amplified earlier in the system, creating a better signal-to-noise ratio. However, the primary reason for using dedicated input amps is to be able to scan the inputs at a faster rate.

It's important to understand how it's possible to achieve the improved scan rate. No matter which data-acquisition scheme you use, you'll have to reduce your bandwidth in order to reduce input noise. If you use a band-limiting filter, the settling time for signal acquisition will increase. It takes approximately seven time constants for a single-pole filter to settle to 0.1% of its final value. For the 100Hz-bandwidth filters shown in Figure 5, this period comes to almost 11ms. You must therefore achieve a higher scan rate through the careful choice and placement of other components.

Typical sample/hold circuits can settle in just a couple of microseconds, and most successive-approximation A/D converters will also have finished their task of digitizing the input signal in a few microseconds, so these components add no significant amount of time to the sampling process. The critical factor is the placement of the instrumentation amps with respect to the multiplexer. With the more standard approach of using the multiplexer in front of the instrumentation amplifiers, you can expect a throughput rate of only 93 samples-per-second; by placing the dedicted INA102s in front of the multiplexer and thereby eliminating the effect of the instrument amps' settling time, you can approach 24,000 samples-per-second.

Your present power supply is probably adequate to power a 64-channel system. With 64 INA102s operating from a dual 15V supply, power consumption will be about 2W. The INA102 runs cool, so you can increase the circuit board's package density and still not have to employ a fan.



When using this scheme, be sure to consider the output capacitance of the multiplexer. By making the band-limiting capacitor much larger than the mux capacitor, the errors can be minimized, while only moderately increasing mux settling time.

FIGURE 5. You can increase the throughput rate of a data-acquisition system by dedicating an INA102 to each analog input channel. In this example, rates can approach 24,000 samples-per-second.

CHOOSING AN INSTRUMENTATION AMPLIFIER

The best way to do a worst-case amplifier comparison is to analyze all possible error sources. To do so, however, you must be sure that the data sheets you're relying on use consistent units. The most popular error-spec units are parts-per-million (ppm) per full-scale input and percent of full scale (%FS).

Most of the data sheet specs are referred to the input. If they're listed in terms of the output, you can refer the figure to the input by dividing by the gain of the amplifier.

Three Types of Error Sources

You can divide error sources into three categories: gain errors, offset and rejection errors, and noise errors. The total noise and nonlinearity of the amplifier will determine the overall signal resolution. Offset and gain error drifts with temperature will mostly limit the reading accuracy. You can often design around certain error sources (common-mode errors and power supply ripple, for example), and you can null (or at least account for) most voltage offsets. **Figure 6** models the various error sources for an instrumentation amplifier.

The input voltage source (V_D) is the signal you would like to amplify accurately. Unfortunately, the gain equation includes some error components—DC gain error, gain drift, and gain nonlinearity. Spec sheets usually list DC gain error in percentage units. However, you must take care to determine gain at the frequency of interest, because gain rolls off after the amplifier's cutoff frequency.

Gain drift is usually listed in ppm/°C, so you have to multiply the figure by the expected operating temperature range to determine the gain drift referred to the input. Gain nonlinearity is also usually given in ppm/°C, and you simply add this error source to the other figures.

Always Some Residual V_{CM}

V_D is usually riding on some type of common-mode voltage (V_{CM}). Instrumentation amplifiers are designed expressly to reject this common-mode signal, but it will always generate a small output.

Error source V_R combines the effects of the common-mode and power supply rejection ratios (CMRR and PSRR; both are much smaller than unity). Most monolithic circuits have excellent power supply rejection, and you can often ignore this source of error. It can be significant in cases where the supply is not well regulated, however. The common-mode rejection ratio is a function of frequency, and you'll have to check the amplifier data sheet to determine the correct value to use in any analysis. Characteristic PSRR curves are usually similar to the CMRR curves.

There are actually two parts that compose the offset voltage (V_{OS})—input offset and output offset. For reference to the input, V_{OS} is easily grouped and modeled as a single voltage source in series with one of the inputs. V_{OS} has both initial and temperature-dependent parts.

Check Change in Temperature

Input bias currents induce other offset voltages, but they are often negligible. The input offset current is simply the difference between the two input bias currents. R_S represents the Thevenin resistances seen from each input terminal, and ΔR_S signifies the difference between input

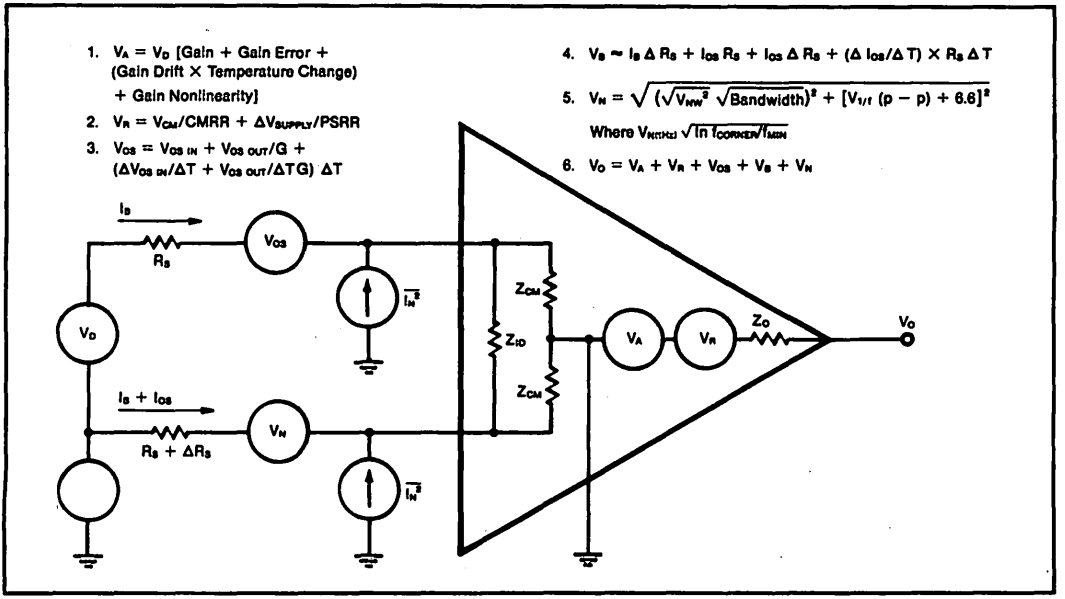


FIGURE 6. You can best compare instrumentation amplifier performance by analyzing all possible error sources. Note that gain and drift errors are referred to the input. V_{NW} is the white-noise magnitude in the white-noise region; the 6.6 divisor in Eq 5 is a crest factor that converts a 0.1%-probable peak value to rms.

source impedances. Though several factors contribute to worst-case offset voltage that can be traced to bias currents, the change in operating temperature is the only significant error source.

Thermoelectric effects at the pins of the amplifier package can create other offset errors. These offsets are most severe when there is a temperature gradient across the package.

One More Error Source

Noise is the final amplifier error source. Other than 60Hz ground loops, the major sources of noise are shot noise, popcorn (or burst) noise, flicker (or 1/f) noise, and thermal noise. Manufacturers' data sheets usually combine these noise sources into three categories: 1/f noise, noise floor (white noise), and current noise.

Current noise is generally negligible for bipolar inputs, and you need only multiply the square root of the system bandwidth by the value of the floor-noise density (listed on the data sheet) for the desired gain. You can often use a crest factor of 6.6 to convert the rms value to a 0.1% probability peak-to-peak value that you can expect to see in any given application. Dividing the 1/f noise by this crest factor will allow you to convert back to an rms value.

To determine the maximum achievable resolution, you'll need to know the noise floor, the system's bandwidth set by the amplifier or filtering, and the 1/f noise (usually given for 1 to 10Hz). Note that the equation for noise voltage assumes that the two noise components are uncorrelated, and that it combines them by taking the square root of the sum of their squares. For example, using the INA102 with gain set for 100 and a 1kHz bandwidth, the input-noise graph on the data sheet shows a 1/f noise figure of $65nV/\sqrt{Hz}$ at 1Hz. In the 1/f range of 1 to 30Hz, the flicker noise is 120nV rms (see Figure 6, equation 5). You'll also need the white-noise value: $30nV\sqrt{Hz} \times \sqrt{(1000 - 30)}$, which equals 934nV. These figures combine to give .94μV rms noise referred to the input. Using a crest factor of 6.6, you can expect to see 620μV peak to peak on an oscilloscope. With the 20V full-scale output, 620μV translates into 31ppm.

The noise-analysis calculation method outlined above is not a rigorous approach; it makes full use of typical amplifier characteristics and provides only approximate results. However, the method does provide a basis for quickly comparing instrumentation amplifiers from different manufacturers.

THE INSIDE STORY

The INA102 consists of a difference amplifier and a pair of noninverting amplifiers, which buffer the signal at each input (Figure 7). With all the gain at the input, the signal is amplified prior to encountering the noise inherent in the difference amplifier and the rest of the system.

All the gain-set and difference resistors are laser-trimmed to provide accurate ratio matching. It is this ratio matching that provides the high common-mode signal rejection (90dB min) and gain accuracy (0.05 to 0.5%, depending on gain). Having all the resistors physically close to each other allows them to track well with changes in temperature, which leads to low gain-drift performance (±5 to ±20ppm/°C, depending on gain).

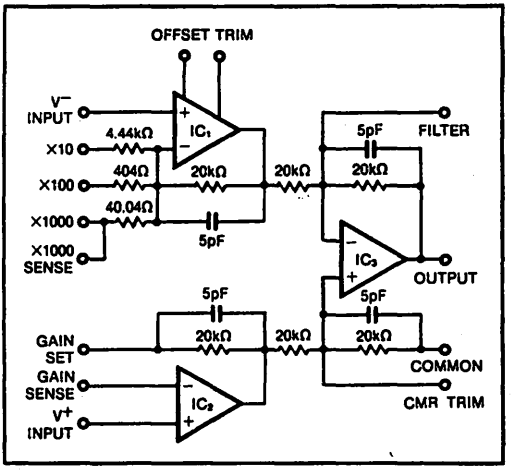


FIGURE 7. The INA102 consists of a difference amplifier and a pair of noninverting amplifiers, which buffer the signal at each input.

Other key specs include a ±3.5 to ±18V supply voltage range, 0.5mA typ current drain, worst-case linearity error (gain = 1000) of 0.05% at 25°C, and an offset voltage of $\pm 300 \pm 300/G\mu V$, where G equals gain. Bias current and offset-voltage drift spec 30nA max and $\pm 2 + 5/G\ \mu V/°C$, respectively. Operating temperature range spans −25°C to +85°C.

The INA102's gain-setting resistors are not trimmed to an exact value; rather, they are trimmed until their ratios with the feedback resistors have the correct value. Note that the feedback resistor of amplifier IC_2 comes out to a pin rather than to the amplifier's inverting input. This scheme decreases the gain errors by referring wire-bond and pin-contact resistance to the feedback resistor instead of the lower-valued gain-setting resistor. And it doesn't take much stray resistance to create problems. If INA102 gain is set at 1000, 0.2Ω in series with the gain-setting resistor will cause a 0.5% gain error. IC_2 senses the gain-setting resistor without including the error caused by the feedback current and the contact-resistance combination.

INSTRUMENTATION AMPLIFIERS SIFT SIGNALS FROM NOISE

Enhancing weak signals at high impedance levels is the instrumentation amplifier's forte. Its differential inputs make most noise pickup common-mode and therefore self-canceling.

Where high common-mode rejection, low signal levels loaded by high input impedance, or ground-line signal immunity must be handled, do not confuse an instrumentation amplifier with a precision op amp. Basically, an instrumentation amplifier is a differential DC amplifier with feedback committed for voltage gain. However, it can be configured for data acquisition roles other than simple voltage amplification.

For example, consider what happens with long input lines where there will be ground-line signals and noise voltages, which are potential error sources (see Figure 1). The error signal is amplified by the operational amplifier. However, with the instrumentation amplifier, the second input is returned to signal ground, making error voltage (e_g) a common-mode signal that is greatly reduced by common-mode rejection. (This is analogous to a power supply's remote-sense connection.) For the INA101 instrumentation amplifier, a 60Hz error signal is attenuated by 106dB.

Of course, an op amp can also be configured to employ common-mode rejection against ground-line noise (see Figure 2). This is the well known difference amplifier. It is well suited to the task, unless high gain and high input impedance are needed together, or where very high common-mode rejection is required. The gain (A) vs input impedance (R_I) compromise is reflected in two equations: $A = R_2/R_1$ and $R_I = 2R_1$. Combining and solving for R_I yields $R_I = 2R_2/A$.

In other words, the higher the gain, the larger the R_2 resistors must be to maintain a given level of input resistance. For a 10kΩ input resistance and a gain of 100, the R_2 resistors become 1MΩ and can create significant output offset error in conjunction with the input offset current of the op amp. With a 741 op amp, this output offset could reach 0.2V. While a FET input op amp would make this error much smaller, bandwidth limitations would remain. Bandwidth is constrained by parasitic capacitance as the R_2 resistances increase (e.g., for R_2 = 10MΩ, a 1pF shunt restricts bandwidth to 16kHz).

Equally serious is the degradation of common-mode rejection (CMR) if parasitic capacitances unbalance the two R_1/R_2 networks. These resistor sets require an exceptional degree of matching to achieve an acceptable common-mode rejection ratio. To visualize this, consider the effect of a tolerance error, ΔR, for a resistor (which could be either R_1 or R_2). Then, $CMRR \leq (R_1 + R_2)/\Delta R$

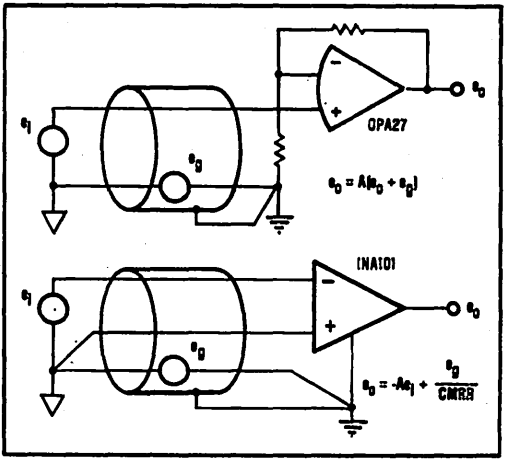


FIGURE 1. While an Op Amp (top) Amplifiers a Ground-Line Signal (e_g), an Instrumentation Amplifier (bottom) Attenuates It.

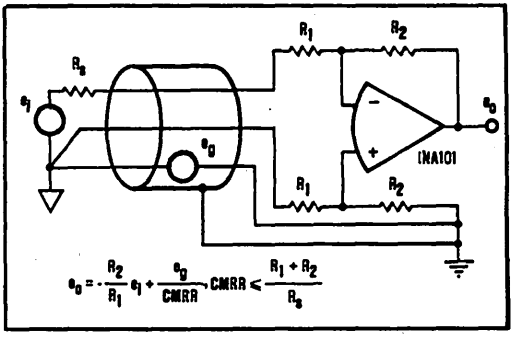


FIGURE 2. Connected as a Difference Amplifier, an Op Amp can Reduce Sensitivity to Ground-Line Signals. But Common-mode Rejection is Seriously Degraded by Signal Source Resistance.

and in the unity-gain case, where $R_I = R_2$, a 0.1% error restricts CMRR to 2000:1, or 66dB. In the same way, a 0.2pF difference in parasitic capacitance across 10MΩ R_2 resistors would restrict the CMR to 66dB at 5kHz. Further CMR difficulty is directly associated with the

difference amplifier's limited input resistance. Again, considering Figure 2, the source resistance of the element monitored is in series with only one input and therefore disturbs the critical match in resistance levels. For R_1 = 10kΩ, CMR is again limited to 66dB by only a 10Ω source resistance. This effect can be compensated for by adjusting the associated R_1 resistor if the source impedance is stable and basically resistive. Should that impedance drift or be complex, this compensation technique is less effective. However, immunity from source-impedance imbalance can be provided by an instrumentation amplifier with high input impedance.

DEALING WITH DIFFERENTIAL INPUTS

Instrumentation amplifiers exhibit a number of characteristics that are frequently not considered when designing with op amps. These characteristics primarily involve the amplifier inputs and their differential capability. (For example, consider the surprising effect of input capacitance on common-mode rejection just discussed.) Instrumentation amplifiers have very high input resistance (around $10^{10}\Omega$ and $10^{13}\Omega$ for bipolar and FET input types, respectively). However, as was noted for op amps[2], these very high resistances are quite susceptible to impedance shunting by small capacitances. Figure 3 clearly illustrates the effect of the common-mode input capacitance on typical bipolar and FET input units. Notice that input-resistance shunting begins at relatively low frequencies. And the assumption that a FET input offers higher input impedance is valid only up to 1Hz.

An instrumentation amplifier's differential inputs are frequently used to monitor floating sources. Because instrumentation amplifiers are DC coupled, the input bias depends on the signal source. The amplifier's input bias currents must have DC return paths to the amplifier's common reference. Since a floating source does not provide such a return, resistors should be connected from each input to the common point (see Figure 4).

Several amplifier characteristics change when these DC return paths are in place. Input resistances are shunted by the added resistors (common-mode by R and differential by 2R). In some cases, input current flowing in the DC returns can develop a common-mode voltage that could saturate the amplifier input. However, with the 10MΩ resistors and the Burr-Brown INA101 of Figure 4, the common-mode voltage is less than 0.3V and input impedances are lowered for frequencies below 10kHz. At higher frequencies, input capacitances dominate. And since the DC returns divert much of the amplifier input bias current, the DC error current in the signal-source resistance is reduced to one-half the difference between the two input currents of the amplifier.

INPUTS CAN BECOME OVERLOADS

Two different input voltage ranges are associated with instrumentation amplifiers: differential and common-mode. However, they are not exclusive of each other. In practice, a maximum voltage can be applied to either amplifier input without producing saturation. This-

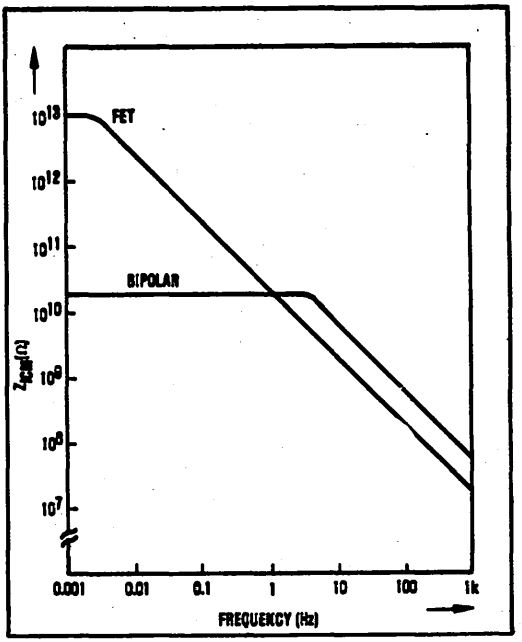


FIGURE 3. Instrumentation Amplifiers' Input Impedances are Rolled Off by Input Capacitances at High Frequencies.

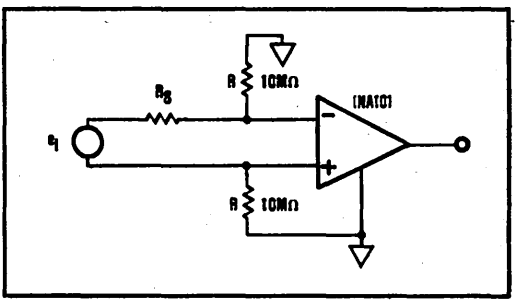


FIGURE 4. When Monitoring a Floating Source, the Inputs of an Instrumentation Amplifier must be Provided with DC Returns to Common.

applied voltage can be differential or common-mode or even a combination of the two. An instrumentation amplifier with a ±10V differential input range and a ±10V common-mode range can only accept a total applied input of ±10V.

Another precaution regarding input voltages is that of input overload protection. When instrumenation amplifiers are employed to null the effects of ground-line voltages, the extensive line lengths can occasionally develop large voltages through parasitic coupling. Similar results could crop up in highly electrostatic environments. Whenever such voltages exceed the power supply levels feeding the amplifier, damage or destruction could result.

IC amplifiers are particulary vulnerable when their isolation junctions become forward-biased. To avoid this problem, amplifier inputs can be diode-clamped to the positive and negative power supply levels (see Figure 5). The resistors limit the overload current conducted by the diodes. The diode type is selected to ensure that leakage does not create excessive input error current.

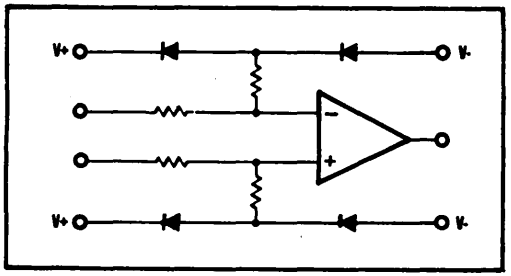


FIGURE 5. Input Overload Protection for an Instrumentation Amp is Achieved with Diode Clamping to the Two Power Supply Buses.

Another thing to be aware of in instrumentation amplifiers is that they have both input and output offset voltages. (With an op amp, all offset voltage can be referred to the input so that offset appearing at the output becomes a function of closed-loop gain.) For an instrumentation amplifier, there is a component of output offset that is independent of gain. Variable gain applications benefit from the two independent offset adjustments. Here, the input offset voltage is first adjusted at high gain where its associated output voltage masks that of the output offset component. Then, the output component is zeroed at minimum gain where the residual input offset has minimum effect (iteration may be necessary).

GROUND-REFERENCING A DIFFERENTIAL SIGNAL

Instrumentation amplifiers can be configured to perform several different data acquisition functions besides normal voltage amplification. Some applications merely require an instrumentation amp that is a modification of the basic three op-amp structure. This consists of two noninverting amplifiers having a common gain-setting resistor, followed by a difference amplifier (see Figure 6a). Input signal e_i is duplicated across gain-setting resistor R_G via feedback that forces the differential input voltages on A_1 and A_2 to zero. This is accomplished with current supplied through the R_1 feedback resistors, which become amplified replicas of e_i at the outputs of A_1 and A_2. (These outputs are of opposite phase.) Also present at the A_1 and A_2 outputs is the common-mode voltage of the inputs. The difference amplifier, A_3 nulls this common-mode voltage while the opposing-phase e_i signal components are combined; the result is a ground-referenced, amplified version of the differential input signal.

Another variation of the three op amp structure provides a current, rather than voltage, output for applications such as current-loop instrumentation (see Figure 6b). This technique returns the normally grounded R_2 resistor

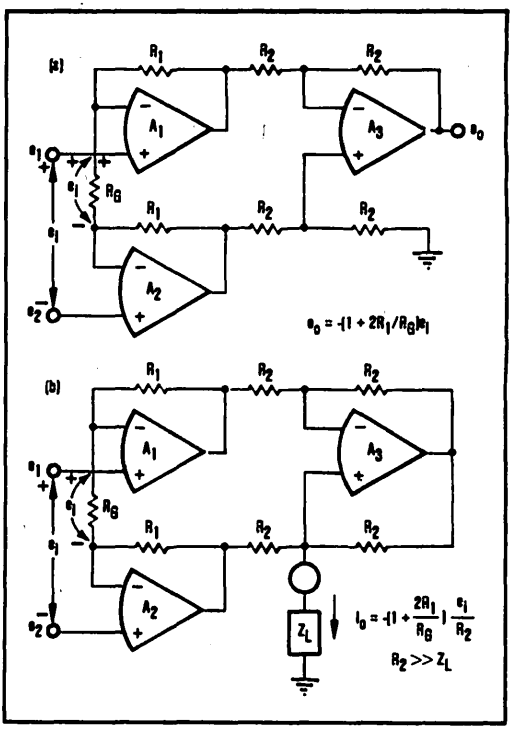


FIGURE 6. For Current-output Operation, the Basic Three Op Amp Instrumentation-Amplifier Structure (a) can be Connected with Positive Feedback on the Output Amplifier (b).

to the difference amplifier output so that the instrumentation amplifier is in a current-source configuration[3] For this current source, the output is taken from the noninverting op amp input, which is not normally accessible on factory-assembled instrumentation amplifiers. Exceptional care must be taken in matching the R_2 resistors to ensure high output resistance for the current source. As this matching is improved, the output resistance approaches R_2 times the CMRR of difference amplifier A_3.

The load-voltage swing in Figure 6b is greatly limited because the current source must be loaded by an impedance much less than R_2. With $Z_L << R_2$, the positive feedback will be significantly less than the negative feedback required to keep the amplifier in a linear mode. However, with $Z_L << R_2$, the amplifier's output swing reaching the load is just a fraction of the amplifier's output capability.

A wider load-voltage swing can be attained with an additional operational amplifier (see Figure 7). To visualize circuit operation, consider the input and output of the op amp follower to be grounded. In this condition, the circuit would be an instrumentation amplifier with load resistor R_S. A well controlled voltage would be established across the resistor so that the current in that resistor would be $-Ae_i / R_S$. This controlled current can be used by

bootstrapping the entire amplifier on the load voltage. The voltage follower isolates the load from undesired current.

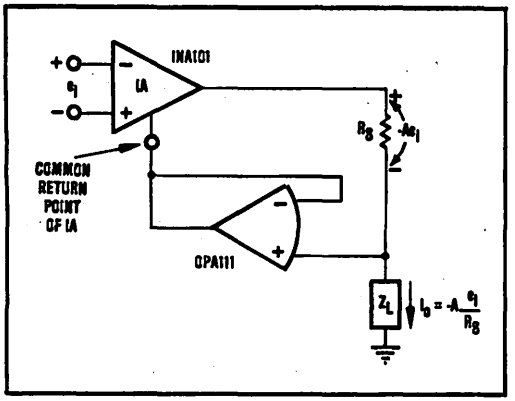


FIGURE 7. Current Output can also be Achieved by Floating the Common Return Point of an Instrumentation Amplifier on the Load Voltage.

Once signal voltage is converted to a current, another common instrumentation amplifier application - supplying input to an A/D converter - can be simplified. Often such converters accept only one input polarity, so a precision rectifier might also be needed. But this rectification is straightforward, since the voltage drops of rectifying diodes do not introduce signal current error (see Figure 8). Rectification results when the polarity change in i_o switches one diode off and the other on. This, in turn, switches the current from one input of the op amp to the other, reversing gain polarity in sync with i_o's polarity.

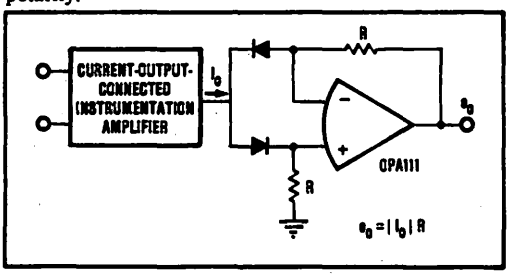


FIGURE 8. Conversion to a Unipolar Output Becomes Simple with a Current Output Configuration.

Current-to-voltage conversion is, of course, another task in current-loop instrumentation. While a sensing resistor can make this conversion, its voltage is not always ground-referenced. Common-mode voltage can be removed with an instrumentation amplifier connected across the sensing resistor.

Current can also be sensed without adding to the voltage drops in a current loop. To accomplish this, the basic three op amp circuit is again modified, this time with current feedback (see Figure 9). Here, gain-setting resistor R_G of the basic structure has been shorted so that the inverting inputs of A_1 and A_2 are common. This configuration produces no potential between the A and B inputs of the overall circuit, which means it can be inserted in a current loop without adding any series voltage drop.

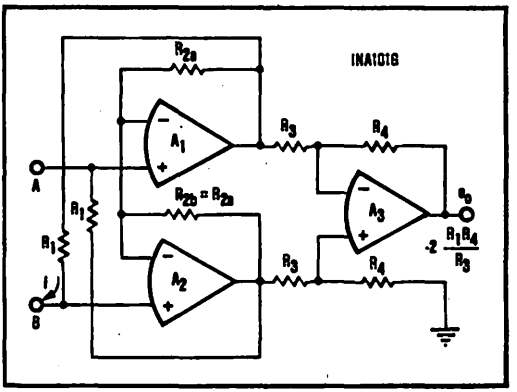


FIGURE 9. For Current Monitoring Without Introducing a Voltage Drop an Instrumentation Amplifier Structure can be Adapted with Current Feedback.

The circuit monitors current by accepting it in one of the R_1 resistors and returning it through the other. Current conducted into terminal A will cause the output of A_1 to swing positive. This produces a current in R_{2A} that is supplied to the inverting input of A_2, where it drives the output of A_2 negative. That negative voltage conducts the terminal A input current through an R_1 input resistor.

Similarly, currents conducted out of terminal A_1 produce a negative voltage at the output of A_1 and a positive voltage at the output of A_2. These opposite-polarity voltages supply equal and opposite feedback currents to the input terminals through the R_1 resistors. At equilibrium, these feedback currents (supplied to the circuit inputs) equal the signal current. (To supply these input currents, the voltage between the outputs of A_1 and A_2 outputs is common-mode voltage induced by any voltage present where A and B are connected. The difference amplifier, A_3, removes this voltage, producing a ground-referenced output voltage proportional only to the current monitored and expressed by $e_o = -2i\,(R_1R_4)/R_3$.

References:

1. J Graeme; G. Tobey; and L. Huelsman, *"Operational Amplifier: Design and Applications"*, McGraw-Hill, New York, NY, 1971.
2. J. Graeme; "Applications of Operational Amplifiers: Third Generation *Techniques"*, McGraw-Hill, 1973.
3. J. Graeme, *"Designing with Operational Amplifiers: Applications Alternatives"*, McGraw-Hill, 1977.

INSTRUMENTATION AMPLIFIER SUITS WIDE RANGE OF CIRCUIT DESIGNS

The latest monolithic instrumentation amplifiers (IAs) ease the design of a variety of high-input-impedance circuits. Data acquisition, overvoltage protection, current sensing, the driving of current loops, programmable gain amplification—all of these applications can benefit from IAs' improved performance specifications.

Monolithic instrumentation amplifiers (IAs) have made significant gains on their discrete counterparts in a number of performance categories. A high speed, fast-settling monolithic IA like the INA110, for example, proves useful in a wide variety of applications. It's easy to design the external circuitry that helps the device meet the stringent reliability requirements of industrial environments, and the speed of the device suits it to multiplexing in data acquisition systems. Other applications exemplify the versatility of the new breed of monolithic IAs.

Overvoltages on the inputs of an instrumentation amplifier can occur in many industrial applications. Two key concerns of a system designer whose products are subject to input overvoltages are therefore reliability and the maintenance of device accuracies. With the addition of the appropriate components, the INA110 will meet the requirements for reliability and negligible shifting in device parameters.

The simplified diagram of the INA110 in Figure 1 can help you to understand the basics of input overvoltage protection. As you can see, D_2 and D_4 cannot conduct for values of V_{IN} within the supply voltage range. D_1 and D_3, however, can conduct, but the currents flowing out of the device are internally limited. The external current-limiting series resistor, R_S, is therefore unnecessary whenever the input voltage remains between the supply voltages.

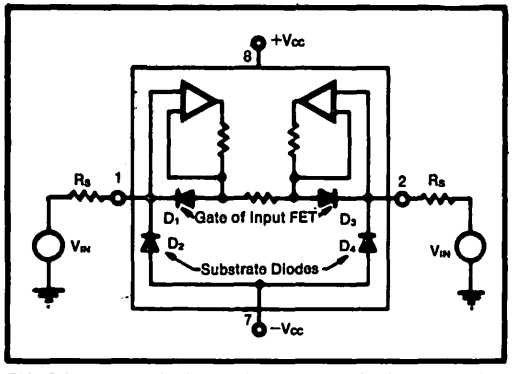


FIGURE 1. Internal circuitry provides current limiting for the INA110 as long as the input voltage remains within the supply-voltage range. To protect against overvoltage conditions, you should add external current limiting resistors (R_S).

More design care is required whenever V_{IN} exceeds either supply voltage. Notice than when V_{IN} is 0.6V below $-V_{CC}$, D_2 and D_4 conduct without an internal current-limiting resistor. When V_{IN} is 4V above $+V_{CC}$, the reverse breakdown of all diodes may occur, and there is no current limit provided for current through D_2 or D_4. To protect the device properly, you should externally limit input currents to less than 1mA; that is, R_S should be greater than

$$\frac{V_{IN\ (MAX)} - V_{CC\ (MIN)}}{1mA}$$

The offset voltage (V_{OS}) and other input-referred parameters are directly related to the input FET's gates (D_1 and D_2), and these gates typically break down before diodes D_3 and D_4 do, so the manufacturer devised the following performance test to evaluate the shift in the INA110's parameters that occurs in response to overvoltage conditions. Sample units were driven at each input with 1mA ACpk at 60Hz for 24 hours at room temperature, after which guaranteed parameters from the product data sheet were tested. The tests indicated no significant shifts in those parameters, but to guarantee that the device maintains accuracy under overvoltage conditions of extended time or at elevated temperatures, it's still good design practice to protect the input FET's gates from breakdown. To do so, you add, along with the properly selected series resistor, external low-leakage clamp diodes, placed from each input to $+V_{CC}$.

Building on these basic design techniques, you can go beyond input protection and provide some form of signal conditioning. Figure 2, for example, shows a 300Hz lowpass filter with 220VAC input protection. The 500kΩ, 1/8W resistors provide the required power dissipation at 200VAC and limit input current into the device to 700μA for a 350Vpk input voltage. You should use metal-film resistors, because many other resistor types exhibit excessive low frequency noise, which may degrade the circuit's performance.

The use of R_1 and R_2 without additional capacitors would yield extremely poor common-mode rejection (CMR), resulting from unequal capacitances on the inputs. You can alleviate the mismatch in input capaci-

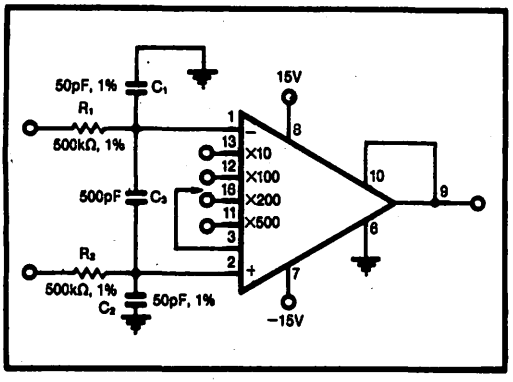


FIGURE 2. This combination input filter and overvoltage-protection circuit employs a 300Hz lowpass filter and provides input protection from 220VAC.

tance through use of shunting capacitor C_3. You obtain the desired cutoff frequency from the equation

$$f(-3dB) = \frac{1}{2\pi 2R_1 \times (C_3 + \frac{C_1}{2})}$$

where $R_2 = R_1$ and $C_2 = C_1$. Input filtering also improves the S/N ratio by reducing the thermal noise of R_1 and R_2, because the thermal noise (V_N) is a function of bandwidth:

$$V_N = \sqrt{4kTR \times \text{bandwidth}}$$

where k is Boltzmann's constant, T is the temperature in degrees Kelvin, and R is the resistance.

Figure 2's circuit assumes a cutoff frequency of 300Hz—a cutoff frequency used in many transducer applications. For practical component tolerances of 1%, C_3 should be much larger than C_1 and C_2 to minimize the differences in the time constants R_1C_1 and R_2C_2. C_1 and C_2 do improve high-frequency CMR, however, and they diminish the familiar problem of RFI rectification, so you must make a tradeoff in the ratio of C_3 to C_1 in order to obtain optimum CMR at both low and high frequencies. Figure 3 shows CMR and common-mode gain versus frequency for worst-case mismatches of values in the circuit. You can further improve the circuit's CMR by adding a small trimming resistor in series with R_1 and R_2 to match time constants R_1C_1 and R_2C_2 to one another.

The performance of the FET-input monolitic IA in this example compares favorably with the performance a premium bipolar IA could achieve. The bipolar IA would introduce a 5mV input-referred error, which is the product of the input offset current (I_{OS}, 10nA) and the 500kΩ resistor; the input-referred error of the FET-input IA would be only 12μV. You could add a V_{OS} trimming resistor to the bipolar IA, but such a resistor will typically introduce a 3.3μV/°C offset voltage per 1mV trimmed. Consequently, the bipolar device will drift in excess of 16μV/°C, compared with a maximum of 2μV/°C for the FET-input device.

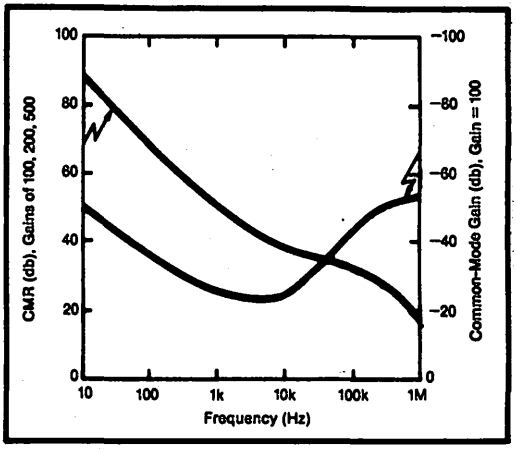


FIGURE 3. You can improve the common-mode rejection for worst-case mismatches of time constants R_1C_1 and R_2C_2 in the Figure 2 circuit by adding a small trimming resistor in series with R_1 and R_2.

The error introduced by flicker noise from the bias currents reacting with the 500kΩ resistor in a bipolar IA circuit will be the dominant noise source, whereas the FET-input IA has negligible current noise—5 to 10 times lower overall. I_{OS} drift in a bipolar IA further degrades performance, showing the necessity of a FET-input IA in applications requiring large input impedances.

The speed of the INA110 renders the device suitable to the type of high speed data acquisition channel shown in Figure 4. Using a multiplexer that settles to within 0.01% in less than 1μs (such as an MPC800 or MPC801), the SHC5320 to perform the sample/hold function, and the INA110, you can achieve 12-bit acquisition times of 5μs with gains of 10 and 100. The 5μs acquisition time translates to a sample ratee of 200kHz, allowing 12-bit sampling of four audio channels.

The low-level output signal of many transducers requires amplification by a factor of 100 for useful processing. For an industrial sensing application, a single INA110 with a gain of 100 can continuously sample more than 150 channels, maintaining a 500Hz bandwidth for each channel and providing the necessary amplification of the signals. The V_{OS} error, a result of the interaction of the input bias current and the multiplexer's on-resistance, is negligible, because the input bias current stays at the picoampere level.

A CONFIGURATION FOR PROGRAMMABLE GAIN

In yet another application, Figure 5 shows the INA110 coupled with a PGA102 programmable-gain amplifier to produce a digitally controlled, fast settling, programmable-gain IA. You can program gains of 10, 100, and 1000 with 0.01% settling times of 6μs, 6μs, and 12μs respectively. Gain ranging can increase the output voltage (V_{OUT}) to within 20dB of full scale to the next stage. When you're multiplexing many channels with different full-scale levels to the input of the IA, it's particularly

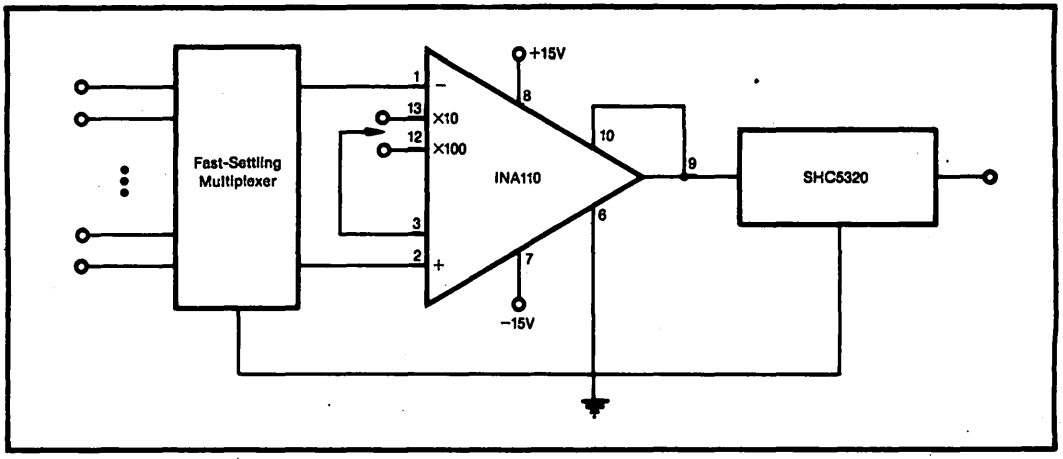


FIGURE 4. You can build a multichannel data acquisition system that has gains of 10 or 100, using the INA110, the SHC5320 to perform the sample/hold function, and an MPC800 or MPC801 multiplexer.

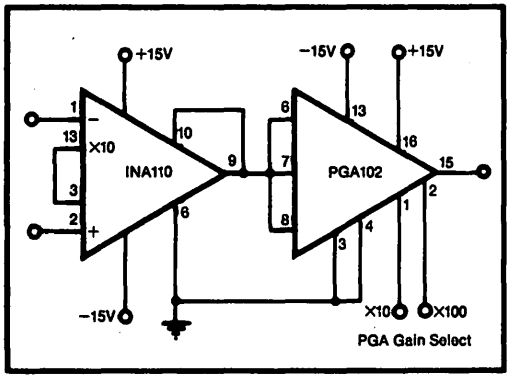


FIGURE 5. You can build a digitally controlled, fast-settling, programmable-gain IA when using the INA110 as a front end for the PGA102 programmable-gain amplifier.

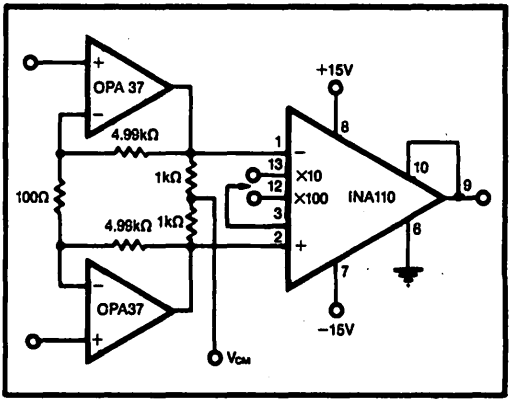


FIGURE 6. You can use the common-mode drive on this high-gain, low-noise IA to improve the circuit's AC common-mode rejection.

useful to be able to adjust the amplification of each signal in order to increase the dynamic range of the circuit. The gain-ranging technique increases the dynamic range of the circuit by as much as 40dB, thereby assuring maximum input sensitivity.

Another application makes use of the common-mode voltage to cancel input noise injected into the circuit through the input leads. Figure 6 shows an IA with gains of 1000 and 10,000 and input-referred noise of $4nV/\sqrt{Hz}$. In this circuit, V_{OS} is held below $50\mu V$, and two low-noise OPA37 op amps provide 40dB of differential gain. The INA110 performs differential-to-single-ended conversion in gains of 10 or 100, resulting in respective circuit gains of 1000 or 10,000. The minimum DC CMR is 108dB and typically exceeds 120dB. AC CMR is usually a function of the parasitics associated with the input lines. Because the bandwidth of the common-mode drive point matches the signal bandwidth of 500kHz, and because the slew rate is above $11V/\mu s$, an input shield or guard driven by the common-mode signal (V_{CM}) will greatly improve AC CMR. The discrete design of this circuit allows you access to V_{CM} for this purpose. (Settling-time considerations are important for this circuit; see "The Limit of Resolution: Settling Time or Noise.")

CURRENT SENSING IN 4 TO 20mA LOOPS

An instrumentation amp like the INA110 serves in current-sensing applications, where a small differential voltage of interest ($I \times R_{SENSE}$) is superimposed upon a large common-mode voltage. Figure 7 shows an IA with a ±100V common-mode range and an input impedance greater than 100kΩ. The circuit is well suited to receiving a signal on a 4mA to 20mA current loop. If R_{SENSE} is equal to 50Ω and the INA110 is set for a gain of 100, you obtain a full-scale output of 10V when a 20mA current flows through R_{SENSE}. The wide common-mode range of the circuit accommodates the large voltage drops, which can occur in the very long wires of a current loop.

The common-mode range of the circuit extends to ±100V when you divide down both input signals by a factor of 10. The circuit also attenuates the differential

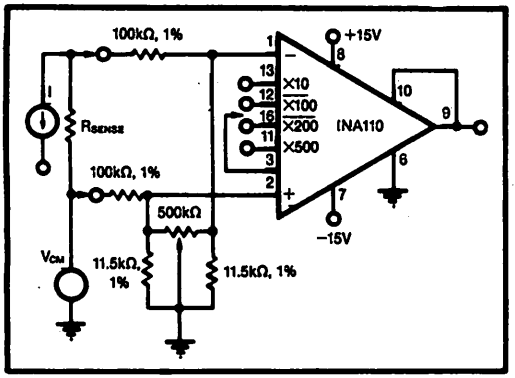


FIGURE 7. You divide down the inputs to improve the common-mode range of this IA circuit. Doing so allows you to use the IA in such applications as current sensing in a current loop, where the signal is a small differential voltage impressed upon a large common-mode voltage.

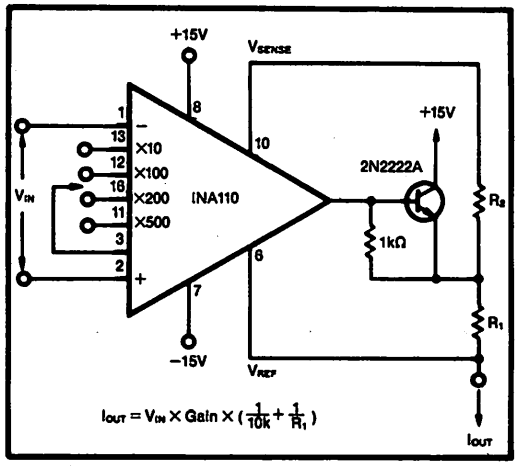


FIGURE 8. This voltage-to-current converter uses the INA110, two resistors, and a current-boosting transistor to provide the current for a 20mA current loop.

signal by 10, so

$$V_{OUT} = I \times R_{SENSE} \times \frac{IA\ gain}{10}$$

Common-mode error results from mismatches in the input attenuators, but you can trim these errors with the 500kΩ potentiometer connected between the attenuators and common. R_{SENSE} also creates a CMR error, which you can cancel by adding a resistor of equal value in series with the 100kΩ resistor in the positive input, or by trimming the 500kΩ potentiometer. To condition the inputs, you can add input filtering at the inputs of the IA using techniques similar to those described earlier.

CONVERTING VOLTAGE TO CURRENT

The current-loop mode of data transmission is very popular in many harsh environments, where differential inputs are required for common-mode rejection of noise as well as for detection of small differential signal on top of large common-mode signal. You can use an IA as the front end in the voltage-to-current converter that's required in current-loop applications. Figure 8 shows how you can build a complete differential voltage-input and current-output circuit with only two precision resistors, a current-boosting transistor, and an IA. The IA creates a voltage equal to $V_{IN} \times$ gain between V_{SENSE} and V_{REF}, causing output current (I_{OUT}) to flow as determined by the equation

$$I_{OUT} = (V_{IN} \times \text{gain}) \div \frac{10kR_1}{10k + R_1}$$

where the 10kΩ is the input impedance of the reference point. R_2 cancels errors resulting from the voltage difference between V_{REF} and the internal common-mode voltage. R_2 must therefore match R_1 to maintain a high output impedance. The current-boosting transistor inside the feedback loop keeps the high power dissipation off the chip and lowers the output current of the IA to the rated level for guaranteed DC performance. The sense point closes the feedback loop and allows you to put the power-boosting function inside the feedback loop, where errors are divided down by the loop gain of 1,000,000. The 1kΩ resistor from the base to the emitter of the current-boosting transistor forms a return path for current out of the reference and sense terminals when I_{OUT} is zero.

When R_1 and R_2 are equal to 50.25Ω, you obtain a 0 to 20mA I_{OUT} for a $V_{IN} \times$ gain product within the range 0 to 1V. The voltage at the V_{REF} point may be between +10V and −10V, which allows for voltage drops along a current loop.

A LOOK INSIDE THE INA110

The INA110 is a variation of the classic three-op-amp instrumentation amplifier (Figure 9). Its FET inputs make possible the use of a differential-input IA in many

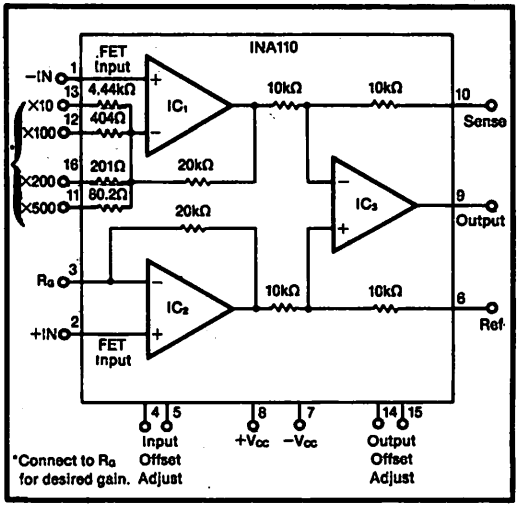


FIGURE 9. The INA110 is a variation of the familiar three-op-amp IA. The device features FET inputs and pin-strappable gains.

high-input-impedance applications, as previously described. The speed of this monolithic IA (Figure 10) suits it to fast data acquisition with multiplexed inputs, to use in gain blocks with high gain-bandwidth products, and to other applications requiring fast settling or a high gain-bandwidth product. Pin-strappable gains increase the device's utility in a variety of applications. The IA is pin compatible with the AD524/624.

Cascoding of the input FETs results in maximum input bias currents of 50pA, an input impedance of $2 \times 10^{12}\Omega$, and a high-gain CMR greater than 106dB. Cross coupling of the input amps and careful thermal layout are additional factors contributing to the INA110's CMR and DC error figures. These techniques cancel thermal feedback, keeping nonlinearity below 0.01% with a 2kΩ load. The laser-trimmed thin-film resisitors help keep gain error low with many gain figures and imparts a level of temperature tracking not achievable with standard discrete components.

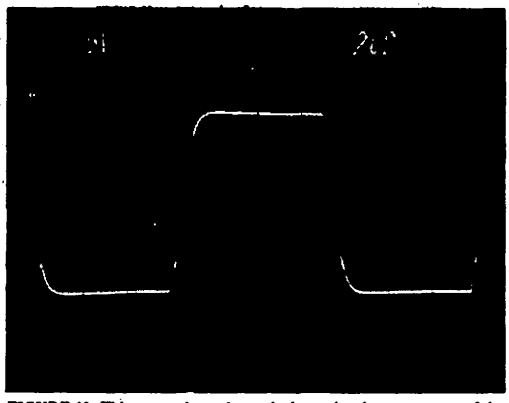


FIGURE 10. This scope photo shows the large signal-step response of the INA110 with a gain of 100. The slew rate is 17V/μs, the bandwidth is 470kHz, and the gain-bandwidth product is 47MHz.

The ability to compensate V_{OS} temperature drift at the wafer level allows a FET design to achieve bipolar level drifts of below 2 + (50/gain)μV/°C. Low noise design and processing techniques achieve an input-referred noise of only $10nV/\sqrt{Hz}$, which is the same noise level you would see in an IA that contains two low noise OPA111s in the front end.

The high-speed characteristics of the INA110 stem from the use of JFETs, rather than conventional lateral PNPs, as high-speed level shifters. A feedback scheme affecting both open-loop and closed-loop characteristics is responsible for the bandwidth's varying only from 2.5MHz to 470kHz as the gain varies from 1 to 100. For gains of 1, 10, and 100, the settling times to 0.01% of a 20V step are only 5μs, 3μs and 4μs, respectively. A slew rate of 17V/s results in a full-power response of 270kHz.

THE LIMIT OF RESOLUTION: SETTLING TIME OR NOISE?

Key concerns in many analog applications are not only how much resolution is possible, but also how long it takes the output to reach the desired accuracy in response to an input change. Manufacturers specify settling time as the time it takes the output to reach the desired accuracy, or error band, after an input-voltage step. In many applications, however, settling time is not the only specification of concern.

The reason? The industry-standard method for testing settling time may not match the user's application. The test uses a periodic waveform and averages out noise by averaging samples over many periods. This technique gives a figure for the settling time that's independent of the noise level. For applications with nonperiodic signals—for example, when an instrument is looking at a single event—you must also consider the output-noise level when computing settling times.

Compare Noise to Error Band

To determine if the output-noise level is a problem, you should make a comparison of the error band to that output-noise level. The peak output noise is equal to a factor of three multiplied by the product of the input noise, the gain, and the square root of the noise bandwidth, where the noise bandwidth is the effective bandwidth of the amplifier's input noise. For most instrumentation amplifiers, the noise bandwidth closely approximates the small signal bandwidth multiplied by 1.57. If the output-noise level is higher than the error band, then you must filter or average the output to reduce the noise bandwidth and achieve the desired resolution. In a case such as this one, the required filtering, and not the settling time of the amplifier, determines the system speed. In Table I you will find maximum noise bandwidths for various input-noise levels, gains, and desired resolutions for a 20V full-scale output.

The chart shows that for high gain or high resolution, the input-referred noise becomes the key concern for a fast-settling amplifier. Although low noise is rare in FET-input designs, the INA110 specifies an input-referred noise level of only $10nV/\sqrt{Hz}$, allowing 12-bit resolution with gains to 100 and settling times of 5μs or less. For those applications requiring even lower noise, you can use a discrete design that employs bipolar input OPA37s, like the one described earlier (see Figure 6).

TABLE I. Maximum Noise Bandwidth with Respect to Input Noise, Gain, and Resolution.

INPUT-REFERRED NOISE ($nV/\sqrt{Hz}$)	GAIN	MAXIMUM NOISE BANDWIDTH (Hz)		
		8 BITS	12 BITS	16 BITS
4	10	110G	400M	1.6M
10	10	17G	64M	260k
16	10	6.6G	25M	100k*
4	100	1.1G	4.0M	16k*
10	100	170M	640k	2.6k*
16	100	66M	250k*	1.0k*
4	1k	11M	40k*	160k*
10	1k	1.7M	6.4k*	26*
16	1k	660k	2.5k*	10*

*An amplifier with a 0.01% settling time of 5μs and a 0.001% settling time of 10μs will be limited by the time required to limit the noise bandwidth to the value shown.

INSTRUMENTATION AMPLIFIERS
Versatile Differential Input Gain Blocks

Instrumentation amplifiers (IA), often referred to as differential amplifiers or data amplifiers, are closed-loop gain blocks with differential inputs and an accurately predictable input to output relationship. They have very-high input impedance and common-mode rejection. This makes them ideal for accurately amplifying low level signals in the presence of large common-mode voltages, such as from strain gauge bridges, thermocouples, and other transducers. They can also be used to effectively eliminate ground-loop interference

NOT AN OP AMP

The instrumentation amplifier differs fundamentally from the operational amplifier. It is designed to be used as a closed-loop gain block. The necessary feedback networks are usually contained within the amplifier, requiring only one external gain-setting resistor. The gain, input and output impedances, frequency response, and other characteristics are specified for the closed-loop, committed operation. Operational amplifiers, on the other hand, are open-loop devices whose closed-loop performance depends upon the external networks.

Some IA's have digitally programmable gain, in which case, even the gain-setting resistors are contained within the amplifier. The operation of IC instrumentation amplifiers may require the user to supply one or two "feedback" resistors in addition to the gain-setting resistor. These user supplied resistors do not affect the input impedance nor the common-mode rejection, as they would in op amp circuits.

Ideally, the instrumentation amplifier responds only to the difference between two input signals and exhibits an extremely-high input impedance, both differentially and common-mode. The output voltage is generally developed single-ended with respect to ground and is equal to the product of the amplifier gain and the differential input voltage;

$$E_O = A_d (E_2 - E_1)$$

Actual amplifiers will depart from these ideal characteristics and can be modeled as in Figure 1. As illustrated in Figure 1, the output voltage has two components; one component proportional to the differential input voltage E_{id}, and another proportional to the common-mode input voltage E_{icm}. The constant A_d is the differential gain (usually fixed by the external gain-setting resistor), and A_{cm} represents the common-mode gain of the amplifier. This is more commonly specified in terms of the common-mode rejection ratio, CMRR, which is the ratio of the differential gain to the common-mode gain.

The impedance Z_{id} is the differential input impedance, and the common-mode input impedance is represented by two equal components, Z_{icm}, from each input to ground. These finite input impedances will contribute an effective gain error due to loading the source impedance, and will degrade the overall common-mode rejection of the amplifier stage if the source resistances are unbalanced.

The nonzero output impedance Z_O will also produce a gain error whose value will depend on the load resistance.

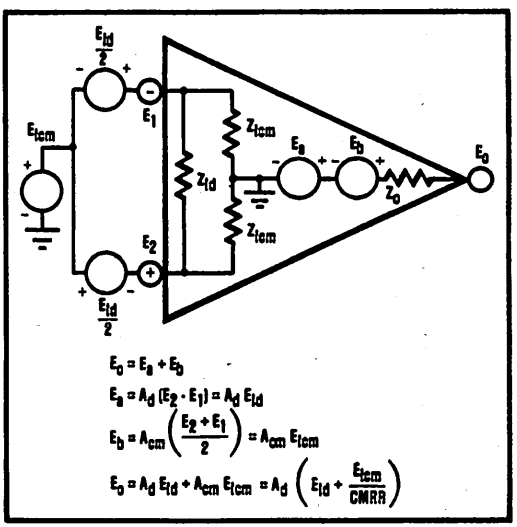


FIGURE 1. Model of Instrumentation Amplifier

SINGLE OP AMP OFTEN INSUFFICIENT

A single op amp can be used to build a differential amplifier as shown in Figure 2, and is suitable in some applications. However, if the application requires high gain, high input impedance, high CMR, or easily selectable gain over a wide range; this simple approach will probably be insufficient.

The differential input impedance of this simple differential amplifier is that of the input resistors which are generally low, particularly if high gain is required. Also, even though the op amp used may have excellent CMR, the finite matching of the resistors can degrade the overall

CMR; 0.1% resistors with zero source impedance unbalance may cause the overall CMR to be as low as 60dB, even if the op amp has infinite CMR.

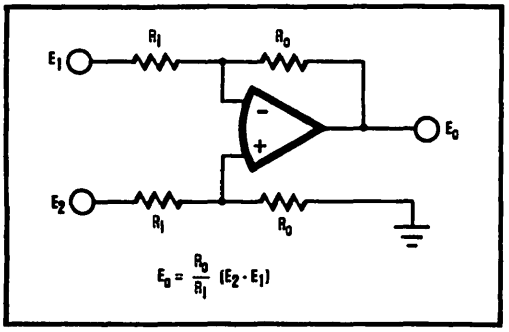


FIGURE 2. Single Op-Amp Differential Amplifier.

WIDE RANGE OF PERFORMANCE AVAILABLE

A common configuration of an instrumentation amplifier consists of three op amps as shown in Figure 3a. The two input op amps provide a differential gain of $(1 + (2R_1/R_G)$ and a common-mode gain of unity. The output op amp A_3 is a unity-gain differential amplifier. Resistors R_1 do not significantly affect the CMR nor the input impedance and their value can, therefore, be chosen for the optimum frequency and offset voltage characteristics. Since the output differential amplifier is buffered by A_1 and A_2, its feedback resistors R_0 can be made low, providing the optimum CMR with frequency and minimum offset due to bias currents.

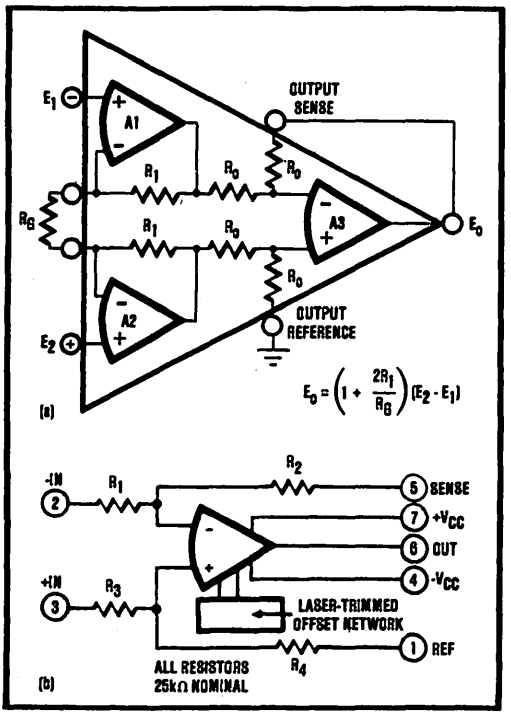


FIGURE 3 (a). Typical Instrumentation Amplifier (INA101).
(b). Low Cost, Unity-Gain Instrumentation Amplifier (INA105).

The three-op amp IA can have very-low equivalent input offsets when A_1 and A_2 have matched offset voltage and offset voltage drift (IA's with drift as low as 0.25μV/°C are available). The independent action of the gain-setting resistor allows gain ranges of 1 to 1000 with less than 0.001% gain nonlinearity while maintaining very-high CMR over the entire gain range. Typically the unity-gain CMR at 60Hz with 1kΩ source unbalance is 90dB and at a gain of 1000 it is 110dB.

A limitation of the three-op amp IA is that the output saturation level (V_{osat}) of A_1 and A_2 impose a limit on the common-mode range in addition to the input common-mode range limit of the op amps;

$$|E_{icm}| + |A_d(E_2 - E_1)/2| \leq |V_{osat}|$$

For typical IC op amps V_{osat} is ±13 volts and the effective common-mode range will only be ±8 volts for applications requiring ±10 volt outputs.

The circuit configuration of a unity-gain instrumentation amplifier is shown in Figure 3b. This type provides input impedance 50kΩ differential and common-mode, with a typical small signal -3dB frequency response of 1.2MHz.

Such performance is ideal in high speed data acquisition systems, where a fast transient signal riding on a common-mode signal must be accurately amplified.

The typcial characteristics of instrumentation amplifiers can be found in Table I. The wide range of specifications is the result of designs optimized for such parameters as low cost, low drift, FET input, ultra-high CMR, or wide bandwidth. In addition to the specifications of Table I, most IA's have input and output protection, and provisions for external adjustment of the offset voltages and CMR for optimum performance.

TABLE I. Typical Characteristics of Instrumentation Amplifiers.

PARAMETER	SPECIFICATION
Range of Gain	1 to 1000
Gain Nonlinearity	0.001%
Input Impedance	$10^{10}\Omega$
Output Impedance	0.01Ω
Common-Mode Rejection	90dB (A_d = 1) to 110dB (A_d = 1000)
Input Offset Voltage Drift	0.25μV/°C to 2μV/°C
Input Bias Current	±5mA
Full Power Bandwidth	6.4kHz

FET INPUT Z MAY BE LOWER THAN BIPOLAR

The effects of input capacitance must be considered when specifying an IA. While the FET input provides very-high input impedance at DC, the input capacitances will typcially cause the input impedance above a relatively low frequency to be no greater than, if not less than, that of the bipolar input IA. The typical input impedances of both bipolar and FET input amplifiers are shown in Figure 4.

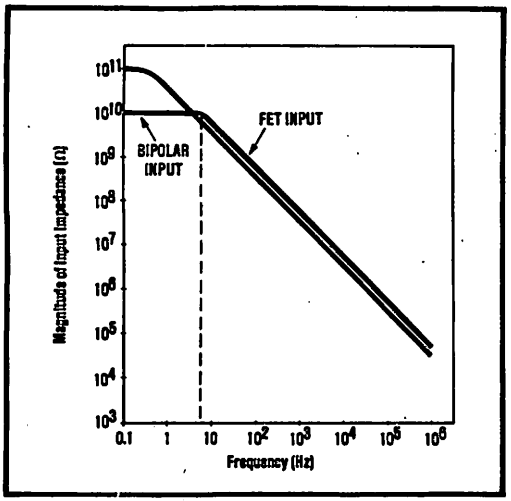


FIGURE 4. Input Impedance vs Frequency for Typical Bipolar and FET Input Instrumentation Amplifiers.

ISOLATION AMPLIFIERS PROVIDE TOTAL SIGNAL GROUND ISOLATION

The isolation amplifier, while not an instrumentation amplifier, can often be easily used as one. Burr-Brown isolation amplifiers, for example, are operational amplifiers with the unique feature of total signal ground isolation. This is accomplished by a high accuracy modulation/demodulation stage which isolates the input from the output by $10^{12}\Omega$ in parallel with only 6pF of coupling capacitance. By connecting the input stage of the isolation amplifier in a noninverting configuration as in Figure 5, the input/output characteristics are those of a high-performance instrumentation amplifier; $10^{12}\Omega$ common-mode input impedance, 160dB CMR over 3500V common-mode range, and easily selectable gains from 1 to 1000 with a linearity of 0.05%.

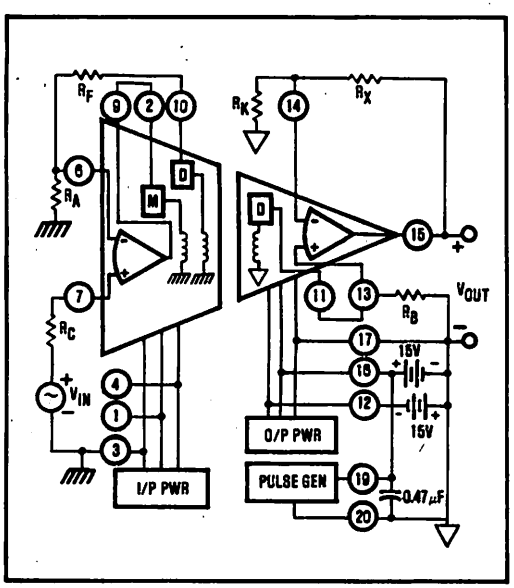


FIGURE 5. Burr-Brown 3656 as a High Performance Instrumentation Amplifier with a CMR of 160dB over a 3.5kV Common-Mode Range.

A frequent mistake made when applying instrumentation amplifiers is not providing a sufficiently low impedance common return path for the input bias currents. These input bias currents range in value from a few picoamperes with FET input amplifiers to hundreds of nanoamperes with bipolar amplifiers. Due to the total signal ground isolation of isolation amplifiers, they do not require a common return path for input bias currents. This and the excellent common-mode input characteristics make isolation amplifiers ideal for medical and control applications where 220V common-mode signals are common.

VERSATILE GAIN

As stated earlier, instrumentation amplifiers generally require only one external resistor to set the amplifier gain, which makes applications requiring a wide range of accurately selected gains a natural for instrumentation amplifiers. A significant consideration in these applications is wiring capacitance across the gain-setting resistor and from the gain-setting resistor terminals to common. These capacitances can cause gain errors in the amplifier at higher frequencies since they shunt the gain-setting impedance at high frequencies. They can also cause the amplifier to oscillate if sufficiently large.

While most instrumentation amplifiers are designed for precision differential gain with as wide a bandwidth possible for a given cost/performance trade-off, some amplifier frequency responses can be tailored for particular applications. The circuit shown in Figure 6 illus-

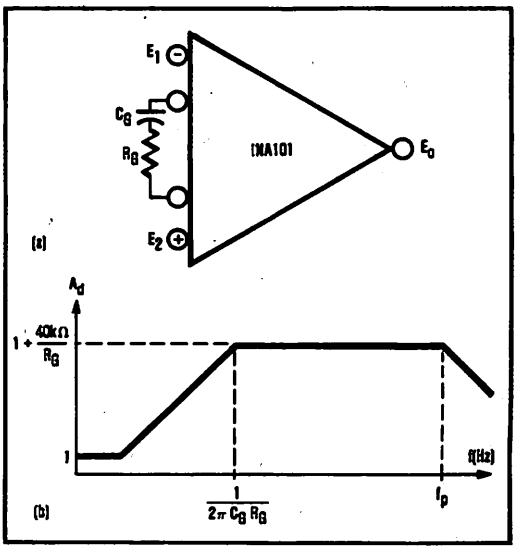


FIGURE 6. IC Instrumentation Amplifier as a Differential Input High-Pass Filter.

trates this capability by using an IC instrumentation amplifier to produce the high-pass function;

$$A_d = 1 + \left(\frac{40k\Omega}{R_G + \frac{1}{2\pi f_c}}\right)$$

The capacitor C_G in Figure 6 reduces the gain to 1 at DC, and is effectively a short for frequencies much greater than $1/2\pi C_G R_G$. The pole frequency f_p is the amplifier's original -3dB bandwidth for the mid-bank gain used.

WIDE OUTPUT OFFSET RANGE

Many modular IA's have separate output reference terminals for adjustment of the output offset over the entire output range of ±10V. With most designs it is necessary to use an active external reference to insure the high CMR specified. A suitable active reference is shown in Figure 7a.

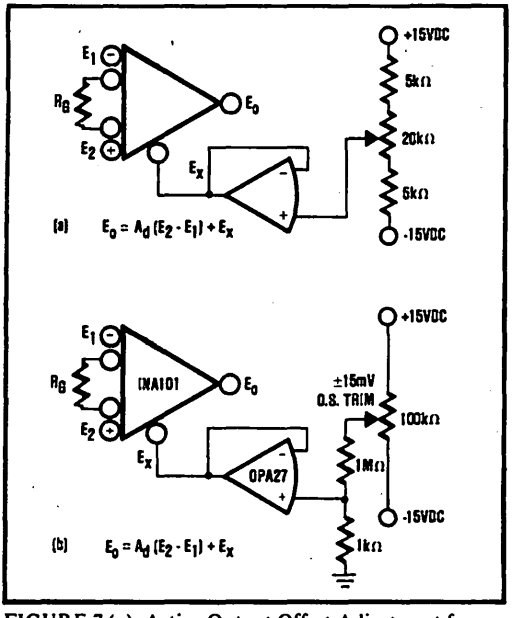


FIGURE 7 (a). Active Output Offset Adjustment for Modular Instrumentation Amplifiers.
(b). Output Offset Adjustment of IA which is Gain Independent.

Some IC instrumentation amplifiers permit output offset adjustment without loss of CMR. Such a circuit is shown in Figure 7b, and has the added advantage of an output offset adjustment independent of A_d.

BRIDGE AMPLIFIER

Probably the most common application of instrumentation amplifiers is in bridge circuits such as the one shown in Figure 8. The output in this case is;

$$E_O = \frac{A_d V}{4}\left(\frac{\delta}{1 + \delta/2}\right)$$

where A_d is the amplifier gain, V is the bridge voltage, and δ is the mismatch in the active arm. For small δ the output is approximately a linear function of δ;

$$E_O \doteq A_d V \frac{\delta}{4}, \text{ if } \delta \ll 1$$

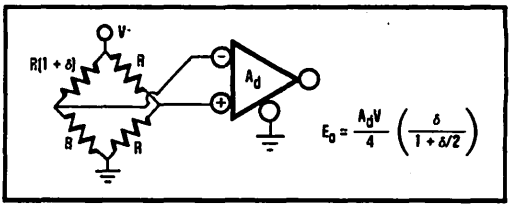


FIGURE 8. Bridge Amplifier with One Active Bridge Arm.

The primary sources of error in this application are the input offset voltage, input bias currents, and the CMR. For small variations in δ the common-mode voltage will not vary significantly, and the output error due to finite CMR may be nulled along with the offset voltage.

IA's ELIMINATE GROUND LOOP INTERFERENCE

Ground noise rejection is a problem which can be solved with an instrumentation amplifier. In installations where a large number of signal sources, amplifiers, and power supplies are being used and are physically far apart, an instrumentation amplifier with its differential inputs can provide better ground noise rejection than a single-ended amplifier.

By making the signal connections as shown in Figure 9 the ground noise at the output will be minimized. The basic problem with the single-ended approach of Figure 9a is that ground currents between the signal source and amplifier will cause a small voltage drop that is in series with the signal source. This ground drop is then amplified by the gain of the amplifier. If an IA is connected as shown in Figure 9b, this ground drop will appear as only a common-mode signal and, therefore, be rejected.

WIDE APPLICATION IN INDUSTRIAL CONTROL

Instrumentation amplifiers can be very useful in industrial control systems where long input leads are generally necessary resulting in the ground drop problems discussed above and also, where the signal source is inherently a differential one. An example of differential signal source is shown in Figure 10, where two thermocouples are used to measure a differential temperature.

In this example the thermocouples are connected series opposing, resulting in a differential signal, with both leads being the same type of metal. This connection reduces the undesired thermocouple potentials formed by the connection of the amplifier inputs to the thermocouple leads to only a common-mode signal. The common-mode signals due to the ambient temperature, parasitic thermocouples, and ground drops can easily be many times the small differential signal (typically on the order of millivolts) and the high CMR of the IA is necessary.

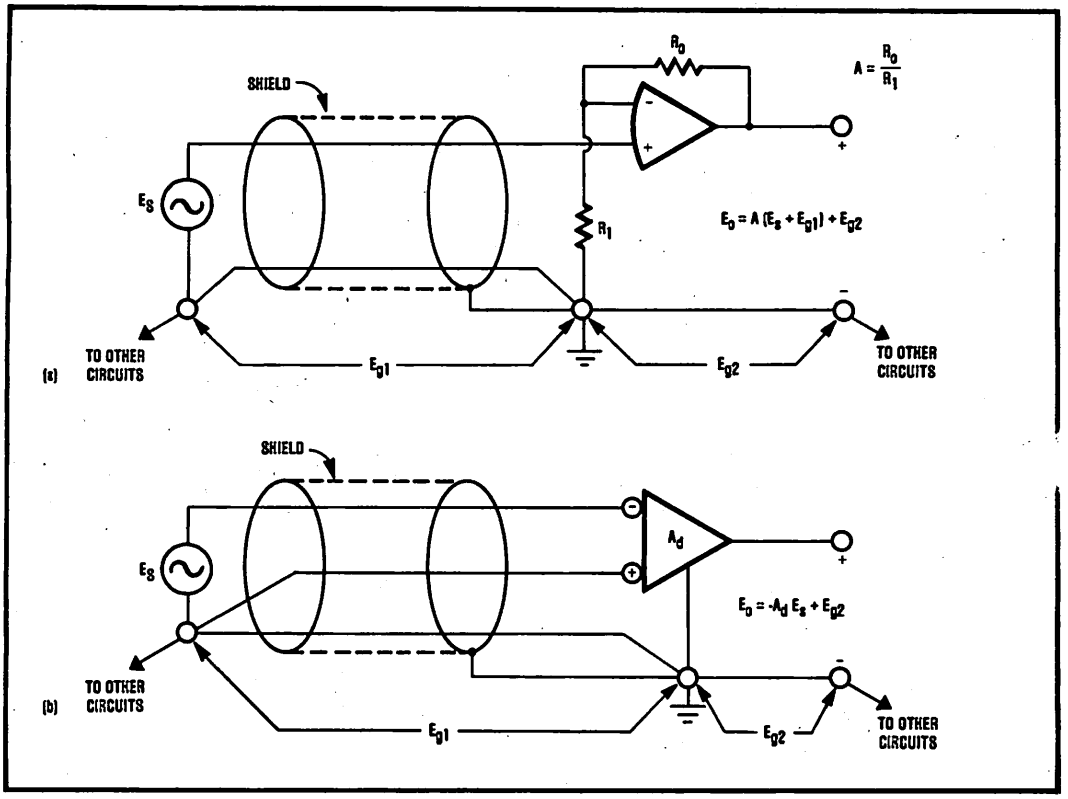


FIGURE 9 (a). Single-Ended Signal Connection.
(b). Differential Signal Connection using Instrumentation Amplifier.

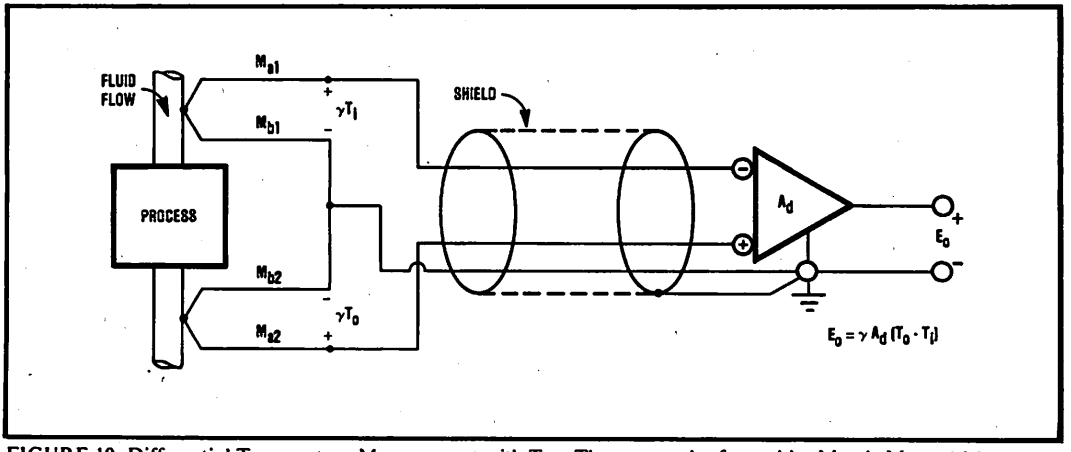


FIGURE 10. Differential Temperature Measurement with Two Thermocouples formed by Metals M_a and M_b.

GUARD DRIVE REDUCES EFFECTS OF INPUT CABLE CAPACITANCE

While the shield on long inputs, if properly used, can significantly reduce the noise picked up, the resulting high input capacitance may adversely affect the overall CMR. The common-mode input capacitance C_{icm} in conjunction with a source impedance unbalance R_u causes a limit on the CMR obtained;

$$CMR(f) \leq 20 \log \frac{1}{2\pi f R_u C_{icm}}$$

Suppose a source impedance unbalance of 1kΩ is driving a one-hundred foot cable with a capacitance of 1.5nF between each input and the shield; the effective CMR at 60Hz would then be less than 64dB, even if the amplifier itself had infinite CMR.

This problem can be overcome by driving the shield with a voltage equal to the common-mode voltage, thereby reducing the common-mode swing on the cable capacitance to zero. Some modular IA's provide a "guard drive" for this purpose, or a voltage which tracks the common-mode voltage can generally be sensed at the middle of the gain-setting resistor when a guard drive is not supplied.

Figure 11 illustrates a simple method of generating a guard drive. Note that in this example the output of the guard drive amplifier is offset from the common-mode voltage by about ±1 VDC, depending on the A_1 type used. However, this offset does not impair the effectiveness of the guard drive to remove the common-mode swing between the shield and the inputs.

The resistor divider between the gain-setting terminals does affect the gain of the instrumentation amplifier, however. For the circuit in Figure 11 the only effect is to modify the gain equation by the addition of a one; 1 + (40kΩ / R_G) versus (40kΩ/ R_G).

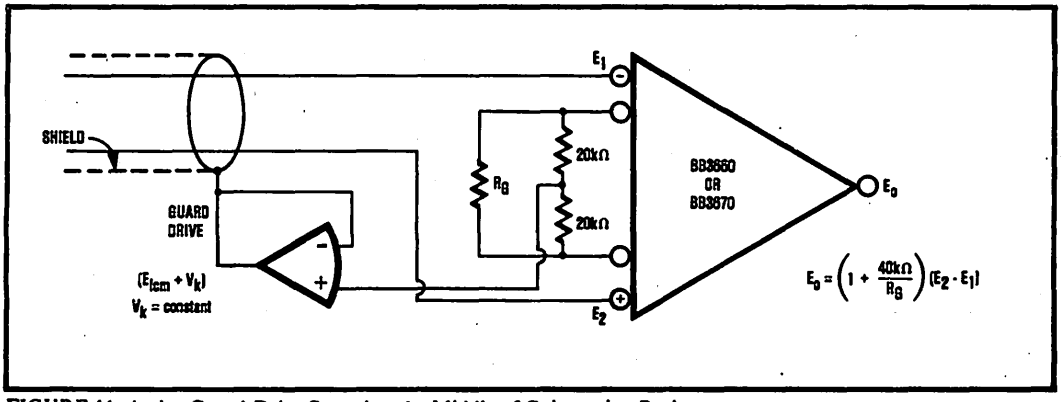


FIGURE 11. Active Guard Drive Sensed at the Middle of Gain-setting Resistance.

MONOLITHIC DIFFERENCE AMP EASES THE DESIGN OF A VARIETY OF CIRCUITS

The general-purpose INA105 monolithic difference amplifier can replace discrete op amps and resistors in a variety of circuits. Because the part's four resistors are closely matched, the chip offers better performance than that of discrete or hybrid component implementations.

You can use the INA105 precision difference amplifier to replace discrete op amps and resistors or a hybrid op amp/resistor network in a number of analog circuits, such as reference-voltage generators, instrumentation amplifiers, summing amplifiers, current sources, and absolute-value buffers. Like all monolithic circuits, the difference amplifier uses less PC board real estate and delivers better temperature performance than do discrete-component implementations. The INA105 offers an extra advantage, however: the part's four resistors are closely matched, so you don't need to perform resistor matching.

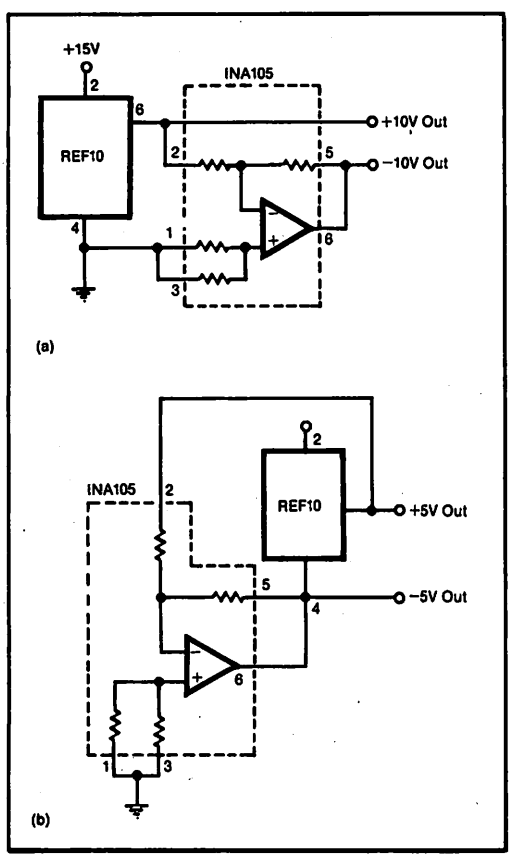


FIGURE 1. To develop precise reference-voltage generators, simply configure the INA105 as a unity-gain inverting amplifier. In the ±10V reference circuit (a), the INA105's low gain- and offset-temperature drifts add only about 2ppm/°C to the reference temperature drift. In the ±5V reference circuit (b), you can operate the REF10 from supply voltages that are lower than the zener voltage.

One application for the monolithic difference amplifier is that of a reference-voltage generator in a unity-gain inverting amplifier. To obtain a precision ±10V reference, you connect the INA105 with a REF10 (zener-based) voltage reference, as shown in Figure 1a. In this instance, the INA105's offset and low-gain temperature drift add only about 2ppm/°C to the reference's temperature drift.

To obtain a ±5V reference, connect the INA105 to REF10 as shown in Figure 1b. This configuration lets you operate a zener-based reference from dual supplies whose voltages are lower than the zener voltage. You can, for example, take advantage of the performance of a 10V zener reference when using ±9V power supplies.

By combining state-of-the-art op amps with the INA105, you can design a high-performance instrumentation amplifier (Figure 2). Resistors R_1 and R_2 set the gain of the instrumentation amplifier according to the transfer function.

$$V_O = (1 + \frac{2R_2}{R_1})(V_2 - V_1)$$

These resistors determine gain only, and you can achieve a high common-mode rejection ratio (CMRR) without precise resistor matching. The difference amplifier's operating errors are effectively divided by the gain of the

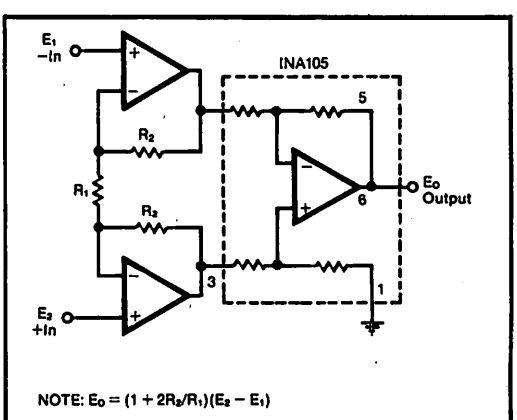


FIGURE 2. You can design a high-performance instrumentation amplifier by combining state-of-the-art op amps with the INA105. To realize low-noise performance in applications in which source impedance exceeds 10kΩ, you should employ FET-type op amps in the input stages.

input amplifiers. The instrumentation amplifier's overall performance is limited only by the input amplifiers.

In low-source-impedance applications, you can improve the instrumentation amplifier's noise, offset, and temperature-drift performance by using OPA37 bipolar op amps for the input stages. At source-impedance levels above approximately 10kΩ, the bias-current noise of an OPA37 reacts with the input impedance and begins to dominate the noise performance of the instrumentation amplifier. To realize low-noise performance in these applications, you should use OPA111 FET-type op amps in the input stages. Table I illustrates the performance of Figure 2's instrumentation amplifier when it's set for a gain of 100. To construct an electrometer-grade instrumentation amplifier, use the OPA128 for a 75fA bias current.

Further, if you drive the noninverting input resistors in parallel and ground one of the inverting input resistors, you'll have a precision gain-of-2 amplifier (Figure 3a). Here, the INA105's resistors establish the circuit's 0.01% gain accuracy. More important than gain accuracy, however, is the gain temperature drift of 2ppm/°C that results from the difference resistors' careful TCR (temperature coefficient of resistance) tracking.

TABLE I. Instrumentation Amplifier Performance.

A_1, A_2	R_1 (Ω)	R_2 (kΩ)	Gain (V/V)	CMRR (dB)	I_B	Noise(1kHz) (nV/√Hz)
OPA37A	50.5	2.5	100	126	40nA	4
OPA111B	202	10	100	110	1pA	10
OPA128LM	202	10	100	118	75fA	38

You can use this precision gain block to extend the input common-mode range of an instrumentation amplifier without degrading either its gain accuracy or its gain drift versus temperature. For example, in Figure 3b, this gain-block technique extends the INA102 instrumentation amplifier's common-mode range from 5 to 7.5V. In contrast, in a conventional instrumentation amplifier, the drive voltage necessary to develop 10V at the output of difference amplifier IC_3 limits the input's common-mode range. Adding gain improves the circuit's common-mode range because the instrumentation amplifier's output no longer has to develop 10V.

If you apply signals separately to the noninverting input resistors of an INA105, the gain-of-2 block in Figure 3a becomes a precision summing amplifier. To obtain a summing amplifier with gain, simply add a pair of external resistors (Figure 4). The inputs are summed at a gain proportional to the ratio of the external feedback resistors. The internal difference resistors set the summation accuracy (0.01%), while the ratio accuracy of external resistors R_1 and R_2 determines the gain accuracy. Offset error will be equal to one-half of the INA105 output offset, times the gain, which is determined by the external resistors.

The INA105 can also serve as a voltage-controlled

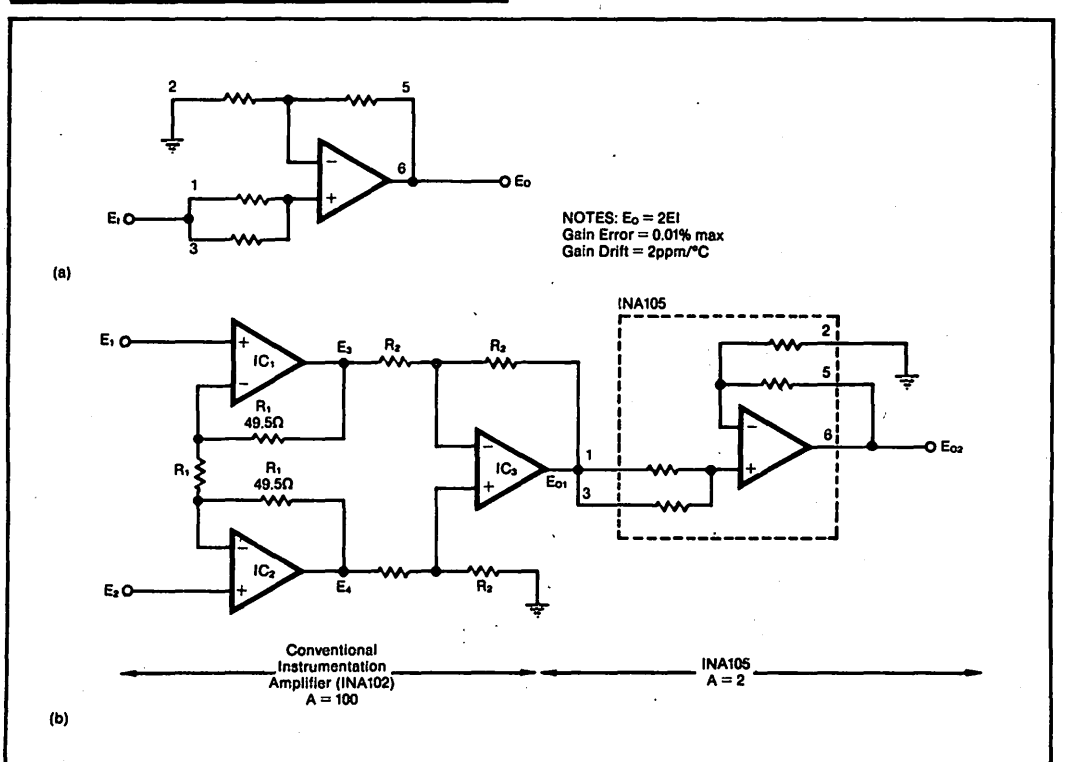


FIGURE 3. To develop a precision gain block, simply configure the INA105 as a gain-of-2 amplifier (a). By combining this gain block with an INA102 instrumentation amplifier (b), you can increase the INA102's common-mode-voltage range by 50%.

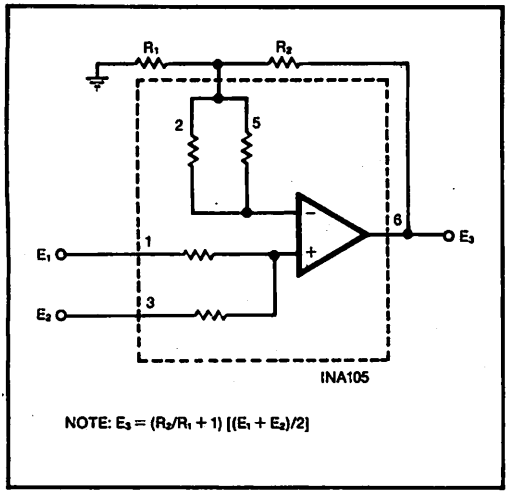


FIGURE 4. To develop a precision summing amplifier with gain, connect a pair of external resistors (R_1 and R_2) to the INA105 and drive the INA105's noninverting inputs independently.

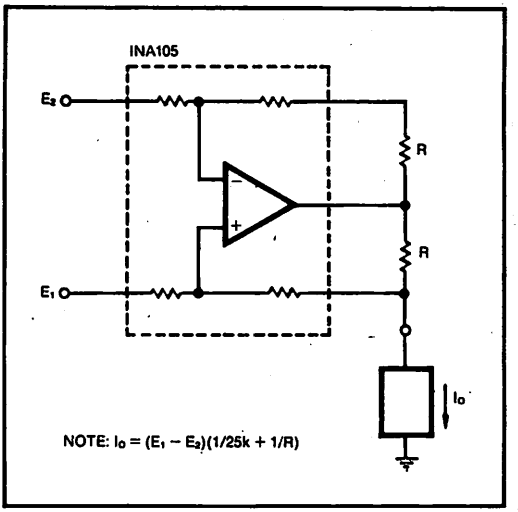


FIGURE 5. To source or sink current from either polarity of input voltage, you can employ the INA105 in this enhanced version of the Howland current pump.

current source, as shown in Figure 5, which depicts an enhanced version of the Howland current pump. The INA105's differential input capability makes the current source versatile. By grounding either input and driving the other, you can source or sink current from either polarity of input voltage. If you drive both inputs simultaneously, the circuit will develop an output current proportional to the input voltage differential.

The classical Howland current pump was difficult to implement because it required closely matched resistors and very accurate TCR tracking. The INA105, however, will let you implement the current pump easily; you simply add two external resistors. You still have to match the external resistors, of course, but you won't have to match them exactly. Because these external resistors work in conjunction with the INA105's 25kΩ resistors, the matching requirement is modified by the ratio of external to internal resistance (Figure 5).

For external resistance values of 100Ω or less, 1% accuracy is adequate. Above 100Ω, you should trim the resistor connected to pin 5 to maintain high CMRR, thereby keeping the current source's output impedance high. You can approximate this output impedance by using the following expression:

$$Z_O = R'(10^{CMRR/20})$$

where R' equals the parallel combination of R and 25kΩ, and CMRR is the common-mode rejection ratio of the INA105.

CURRENT TRANSMITTER SINKS AND SOURCES CURRENT

Because of its 20mA output-current rating, the INA105 is also suitable for use as a 4–20mA current transmitter, as Figure 6a shows. The transmitter circuit converts a 0 to 10V input to a 4–20mA output. The OPA27 is configured as an inverting attenuator. It combines the 10V reference and the 0 to 10V input to develop a −0.2 to −1V signal range at the inverting input of the INA105.

By limiting the current pump's input to 1V—and therefore, limiting the voltage across the 50.1Ω resistors to 1V—you can obtain output compliance of greater than 9V when the current transmitter is driving a grounded load. Unlike open-collector or open-drain designs, this current transmitter can both sink and source current.

To provide both buffering and gain for the current transmitter, you can add a pair of op amps at the transmitter's input (Figure 6b). As was the case with the instrumentation amplifier, the choice of bipolar or FET op amps depends on your application. When you use OPA27s on the input, this circuit will provide low-noise amplification, high common-mode rejection, and current transmission capability for direct thermocouple inputs. For applications requiring high-level current-output capability, you can add an npn transistor at the output of the INA105, as in Figure 6b.

When you implement the current pump, be sure to keep your external resistance values as low as possible. Large external resistances (greater than 250Ω) can decrease your circuit's CMRR, because even though the INA105's R_2/R_1 to R_4/R_3 ratio is trimmed to 20ppm, the absolute match of the two sides (R_2/R_4, for example) is only about 1%. If you add two perfectly matched 250Ω external resistors, the resulting mismatch could be as much as 0.01%, lowering the CMRR to 86dB.

In addition, as the value of the external resistors increases, TCR-tracking performance will suffer. If the external resistors' TCR is 100ppm/°C, values exceeding about 500Ω will degrade the circuit's CMRR (and therefore its output impedance) over temperature. You can solve this temperature problem by adding an amplifier to the output of the INA105 in your current-transmitter circuit (Figure 6c). The op amp will buffer the reference pin of the difference amplifier, eliminating any need for resistor matching.

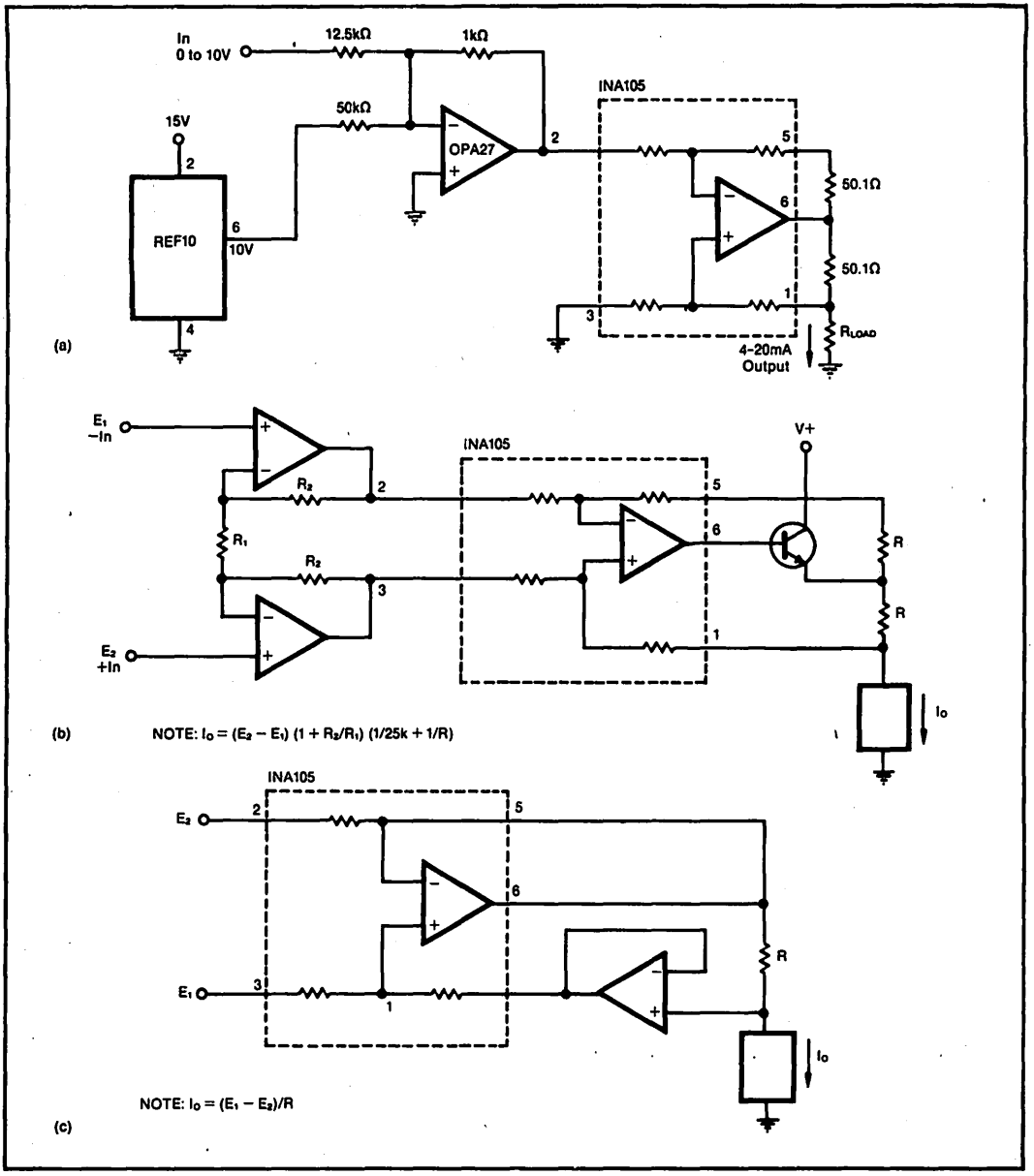


FIGURE 6. To design a 4-20mA current-transmitter circuit, use an OPA27 to sum the reference and use 0 to 10V signal inputs to develop a −0.2 to −1V signal range at the input of the INA105 (a). To provide both buffering and gain, add a pair of op amps at the input (b). To compensate for temperature problems, add an amplifier to buffer the INA105's reference pin (c).

Figure 7 illustrates a current-receiver circuit that has compliance to either power-supply rail. When you put a 100Ω sense resistor between the INA105 and the supply rail, the circuit's transfer function is $E_O = 100I_I$, for E_O in volts and I_I in amps. Adding another 100Ω resistor preserves the input resistance match of the INA105 and maintains high CMRR. Because 100Ω is small compared to the 25kΩ resistors in the difference amp, a 1% tolerance for the 100Ω resistors is sufficient to maintain an 86dB CMRR.

The 100Ω sense resistor in series with pin 2 lowers the amplifier's gain by about 0.4%, and the 50kΩ input impedance at pin 3 shunts the 100Ω sense resistor and reduces its effective resistance by 0.2%. The 1% tolerance of the 100Ω sense resistor could make the current receiver's gain error as high as 1.6%. Although 1.6% gain error is adequate for many applications, you can improve the gain accuracy to 0.05% by using 100.6Ω resistors with 0.02% tolerance.

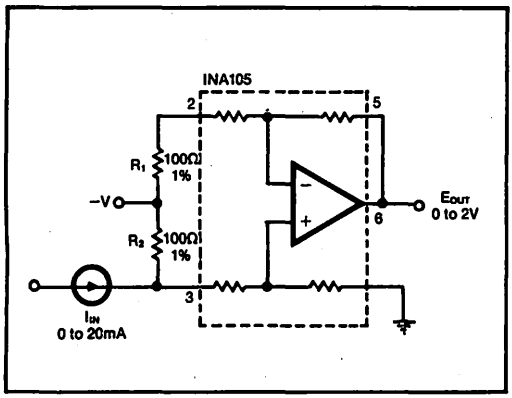


FIGURE 7. This current-receiver circuit offers compliance to either power-supply rail. The second 100Ω resistor (R_2) preserves the input-resistance match of the INA105, maintaining high CMRR.

DESIGN AN ABSOLUTE-VALUE BUFFER

The monolithic difference amplifier is also useful in absolute-value signal processing. By connecting a few components to the INA105, you can configure the difference amplifier as a precision absolute-value buffer (Figure 8a). The OPA111 provides FET-type input characteristics. Because rectification diodes D_1 and D_2 are within the input amplifier's feedback loop, the amplifier's open-loop gain corrects for the diodes' forward-voltage drop. The buffer circuit's overall accuracy equals that of the INA105—0.01%.

When it has negative input signals, the circuit functions as a unity-gain inverter (Figure 8b). D_2 is reverse biased, and IC_1 pulls current through D_1 to equalize the voltage levels at the inverting and noninverting inputs. Because R_1 equals R_2, IC_2 simply acts as a precision unity-gain inverter, and E_O equals $-E_I$.

When the circuit's input signals are positive, D_1 is reverse biased, and the circuit functions as a unity-gain buffer (Figure 8c). IC_1 forces current through D_2 to establish a voltage at IC_2's input. This voltage, in turn, makes the voltage at IC_1's inverting input equal to the voltage at IC_1's noninverting input. Because no current flows into the inputs of either IC_1 or IC_2, the voltage drop across both R_1 and R_2 is zero, and the voltage at the output of IC_2 equals that at the input of IC_1.

In an application in which you must use digital signals to control analog circuits, you can use the unity-gain buffer as an amplifier with a digitally controlled gain of +1 (Figure 9). The DG188 analog switch acts under logic control to connect the INA105's noninverting input to either the input signal or ground.

For a logical-zero control signal, the noninverting input is connected directly to ground, and the circuit functions as a conventional unity-gain inverter. For a logical-one control signal, the INA105's noninverting input is connected to the input signal. Because the voltage across the amplifier's inputs is zero, no current flows through the input resistors, and the amplifier acts as a unity-gain buffer.

Errors contributed by the analog switch (a function of the on/off resistance ratio) are less than 0.01% in this example. The DG188 toggles in less than 150ns, so the circuit's settling time (to 0.01%) is less than 5μs.

SOME DIFFERENCE-AMPLIFIER BASICS

In basic terms, a difference amplifier, such as the INA105 from Burr-Brown (Figure 10), is the combination of a unity-gain inverting amplifier and a gain-of-2 noninverting amplifier with a 1/2 resistor divider on that input. Therefore,

$$E_O = -E_{I1} + E_{I2}$$

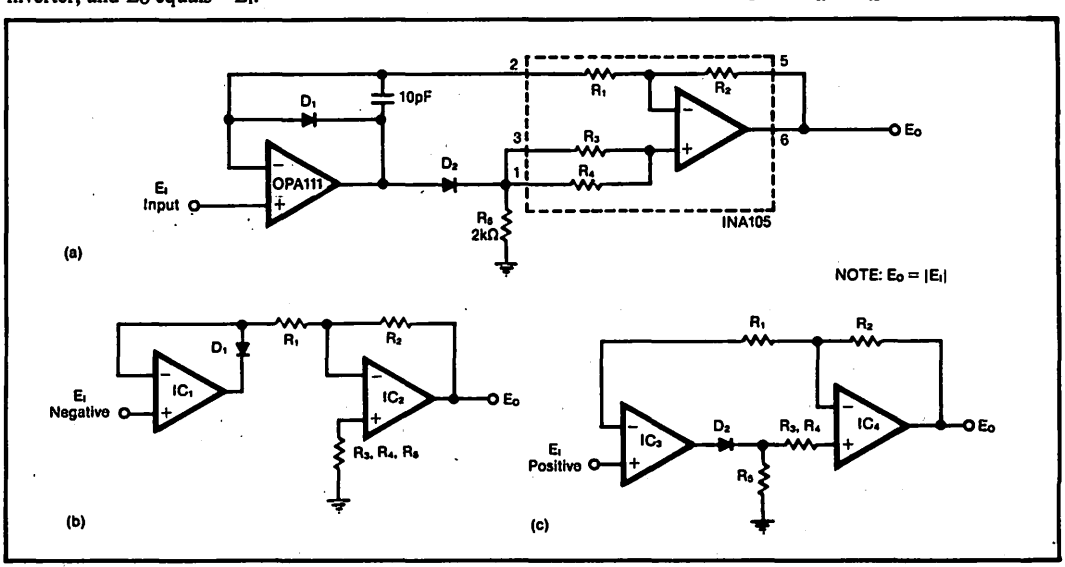


FIGURE 8. By connecting a few components to the INA105, you can configure the difference amplifier as a precision absolute-value buffer. The OPA111 in the buffer circuit (a) provides FET-type input characteristics. When the input signals are negative, the circuit functions as a unity-gain inverting buffer (b). When the input signals are positive, the circuit functions as a unity-gain buffer (c).

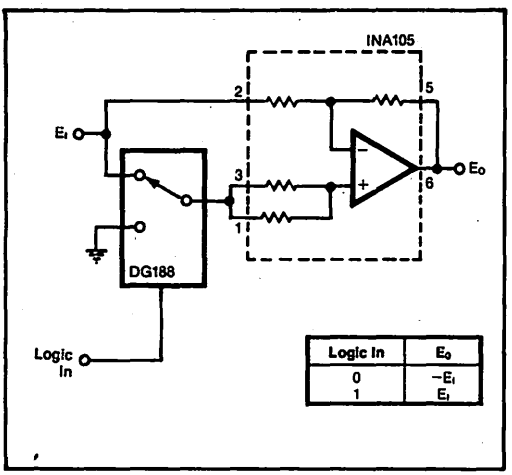


FIGURE 9. To control analog circuits with digital signals, you can configure this unity-gain buffer as an amplifier with a digitally controlled gain of ±1. In this figure, the DG188 analog switch acts under logic control to connect the INA105's noninverting input to either the input signal or ground.

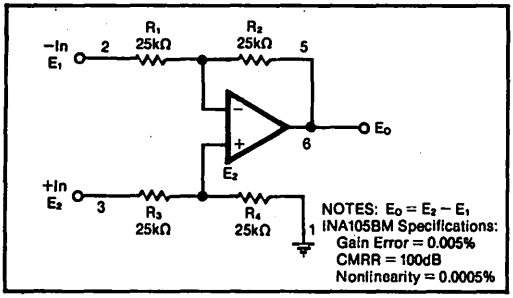


FIGURE 10. A difference amplifier such as the INA105 includes a unity-gain inverter, a gain-of-2 amplifier, and a pair of resistor dividers.

where E_{I1} is the inverting input's voltage and E_{I2} is the noninverting input's voltage. If the signals at the inputs are equal, the signal at the output is zero. The difference amplifier responds to the difference between the signals at its inputs and rejects the common-mode signal.

The common-mode signal is the signal that appears on both inputs:

$$V_O = \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) V_2 - \frac{R_2}{R_1} V_1$$

The INA105's 100dB CMRR results from the 0.002% match of the R_4/R_3 ratio to the R_1/R_2 ratio. Because the resistors' TCR tracking is better than 2ppm/°C, the part maintains an 86dB min CMRR at +85°C.

When you're applying a difference amplifier, it's important to preserve the critical resistor matching. Any source impedance adds directly to the input-resistance values (at R_1 and R_3). Likewise, any wiring resistance adds directly to the precision-difference resistance at any of the resistors. A resistance of 5.0Ω will degrade the CMRR to 80dB.

Because the resistors in the amplifier are carefully matched to preserve the $R_2/R_1 = R_4/R_3$ relationship, you should connect the INA105 as shown; don't interchange pins 1 and 3 or 2 and 5. If you were to switch R_3 and R_4, for example, the device would still be a difference amplifier, but its performance would suffer. If you were to switch pins 1 and 3, the ratio accuracies might be only 0.01% instead of 0.002%, and the circuit would experience increased temperature drift and thermal-feedback errors, in addition to CMRR problems.

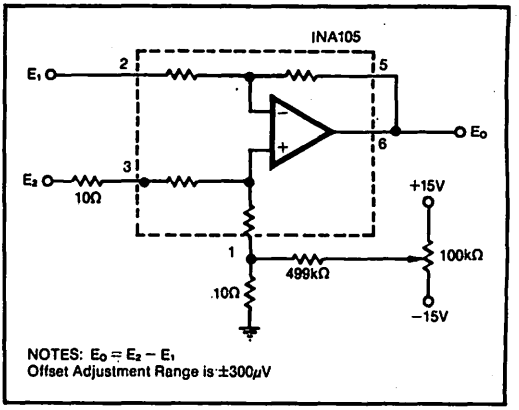


FIGURE 11. You can adjust the INA105's offset by using the circuit shown here.

Further, if you use the reference pin to trim the voltage offset, you must maintain the resistor ratios, thus preserving CMRR and gain accuracy. To maintain the resistor ratios, you can add a 10Ω resistor in series with both the reference and noninverting-input pins, as shown in Figure 11. To realize 300μV of offset adjustment, you can drive the offset point through a 499kΩ resistor from the potentiometer.

The input common-mode range of a difference amplifier extends to the power-supply rails and beyond. To sense a transmitted current signal (such as a 4–20mA signal) at one of the power-supply rails, put the currrent-sense resistor at the power-supply rail; this setup will let you take maximum advantage of the current transmitter's compliance. Unlike a conventional instrumentation amplifier—which can't function when its inputs are close to the power-supply rail, and thus requires you to restrict the common-mode range of the signal—a difference amplifier lets a sense resistor monitor the signal directly at the rail without your having to restrict common-mode range.

TAME TRANSDUCER BRIDGE ERRORS WITH OP-AMP FEEDBACK CONTROL

Designing high-performance bridge-monitoring circuitry can prove difficult. You can ease the problem significantly, though, by using op amps.

You can simplify the design of transducer bridges by using op amps to linearize bridge response and reduce drift sensitivity. Such bridges pose a demanding instrumentation challenge because of their low-level output signals and inherent nonlinearity; accurately monitoring their output calls for an amplifier with input offset voltage that exhibits very low thermal drift. This article illustrates network designs using both voltage and current bridge-biasing techniques and demonstrates how feedback control can ease the task of designing high-performance monitoring circuitry.

Instrumentation amplifiers usually serve in the classical forms of such monitoring circuits. In a typical configuration (Figure 1), the amplifier develops an output given by

$$E_O = \frac{(A)(V)(\Delta R/R)}{4(1 + \Delta R/2R)} - AV_{OS}, \qquad (1)$$

where ΔR and V_{OS} equal transducer variation and amplifier input offset voltage, respectively.

Because ΔR appears in both the numerator and denominator of the first term, this circuit develops a nonlinear output response. Keeping ΔR small—so that its effect in the denominator is negligible—minimizes nonlinearity error. Unfortunately, reducing ΔR in this manner also reduces the output signal level, making the V_{OS} term's error contribution more significant.

Although you can null out initial offset voltage, its thermally-induced drift introduces errors. V_{OS} drift is typically a primary accuracy limitation, and as Equation 1 illustrates, the instrumentation-amplifier-monitoring circuit is particularly sensitive to offset-voltage drift.

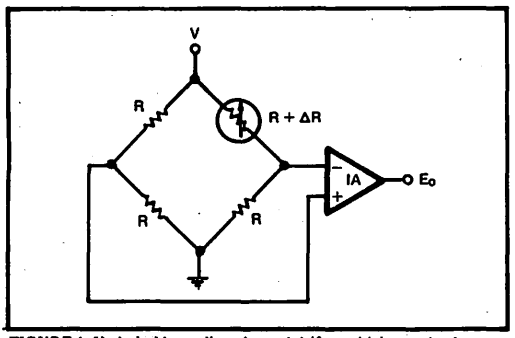


FIGURE 1. Undesirable nonlinearity and drift sensitivity result when you use an instrumentation amplifier for bridge monitoring.

Specifically, V_{OS} is multiplied by the full amplifier gain A; the $V\Delta R/R$ transducer-deviation signal is only amplified by A/4.

You can, however, reduce (or even eliminate) nonlinearity and drift errors. For example, if you bias the bridge with a current source I, network output response becomes

$$E_O = \frac{A(I)\Delta R}{4(1 + \Delta R/4R)} - AV_{OS}. \qquad (2)$$

Now the ΔR term in the denominator is divided by 4R, instead of 2R as in the voltage-bias scheme. The result: a 2:1 reduction in nonlinearity error.

A dual-transducer bridge allows you to realize the full benefit of such current biasing. With the second transducer replacing the grounded element of the opposite bridge leg, output response becomes

$$E_O = \frac{A}{2} I\Delta R - AV_{OS}. \qquad (3)$$

In addition to doubling signal gain, the dual-transducer configuration develops a linear response.

Unfortunately, reference-current sources suitable for this approach are not as readily available as their voltage counterparts. You could, of course, start with a voltage reference and build a current source, but op amp control (Figure 2) offers a more direct solution.

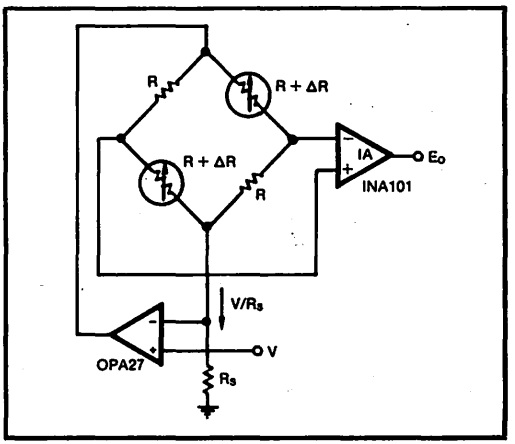


FIGURE 2. Reduce output nonlinearity by adding op amp feedback control to produce a constant-current bridge bias.

As shown, the op amp drives the bridge in a constant-

current mode. Resistor R_S senses bridge current, and the voltage developed across it gets compared with a reference voltage V. Feedback equalizes these voltages and improves response linearity by maintaining a constant current in the bridge.

In this circuit, errors introduced by the op amp are negligible. So long as you maintain V's value at a few volts, any error-current contribution from the op amp to bridge bias current I has secondary importance. Similarly, adding op amp input bias current to I rarely affects the design significantly.

However, one potential problem does exist. If the op amp isn't close to the bridge, stray wiring capacitance from its inverting input to ground can cause oscillation. Adding capacitance from the op amp's inverting input to its output overcomes this problem.

You can also achieve linearity correction by letting bridge bias vary with the signal. Examine the signal term of Figure 1's response equation:

$$\frac{V(\Delta R/R)}{1+\Delta R/2R};$$

note that if V is proportional to $1+(\Delta R/2R)$, cancelling terms appear in both the numerator and denominator. The result is a linear response.

A signal proportional to ΔR is available at the instrumentation amplifier's output. After scaling, you can feed this signal back through an op amp to modulate bridge bias (Figure 3).

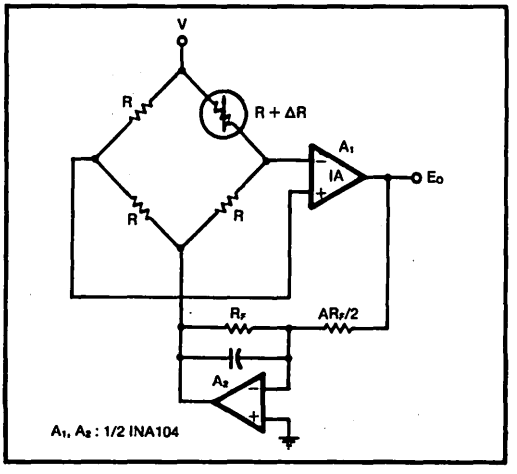


FIGURE 3. To cancel bridge nonlinearity, utilize feedback modulation of the bridge bias voltage.

In the Figure 3 design, the op amp controls the voltage at the point of the bridge that's normally grounded. This addition yields a circuit response given by

$$E_O = \frac{A}{4}\left(\frac{V\Delta R}{R}\right) - AV_{OS}. \qquad (4)$$

In this expression, if the op amp circuitry has a gain of $-2/A$ (where A equals instrumentation amplifier gain), nonlinearity cancellation is complete.

Unfortunately, you can't achieve perfect gain setting; however, adjusting op amp gain to within 0.1% of $-2/A$ produces a 1000:1 reduction in the response's inherent nonlinearity. Residual nonlinearity then equals that of the nonideal transducer.

Once again, it's easy to minimize op amp-induced error contributions. The INA104's output offset voltage generates a bridge-bias error voltage equal to $[1+(2/A)]\,V_{OS}$. So long as any drift of this error voltage is small in comparison to V, the resulting network error not removable by calibration is also small. You can control error arising from op amp input bias current by merely limiting the value of R_F.

Frequency stability is a greater concern because there are now two amplifiers in the feedback loop; unless one dominates the composite-loop frequency response, oscillation can result. You can ensure the presence of a dominant pole by shunting the op amp feedback resistor with a capacitor.

Another way to achieve error correction is via feedback modulation of a bias current (Figure 4). As in Figure 2's

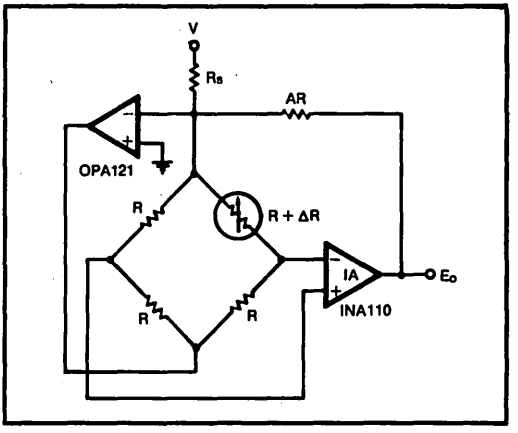


FIGURE 4. You can also use current feedback to provide nonlinearity correction. The feedback resistance determines linearization accuracy.

design, an op amp forces a constant current to flow in a bias resistor (R_S). Adding a signal derived from the instrumentation amplifier output develops a network output equal to

$$E_O = \frac{A}{4}\left(\frac{V\Delta R}{R_S}\right) - AV_{OS}. \qquad (5)$$

Feedback resistance (equal to the product of bridge resistance R and amplifier gain A) determines linearization accuracy.

This circuit must have a positive gain polarity to achieve the correct feedback-current phase. Figure 5 shows how to arrange the feedback for applications requiring a negative gain polarity. Here, the feedback drives the current-forcing op amp. An increase in transducer resistance causes E_O to swing negative and drive the op amp in the same direction. This action increases the voltage drop across R_S, increasing bridge current and

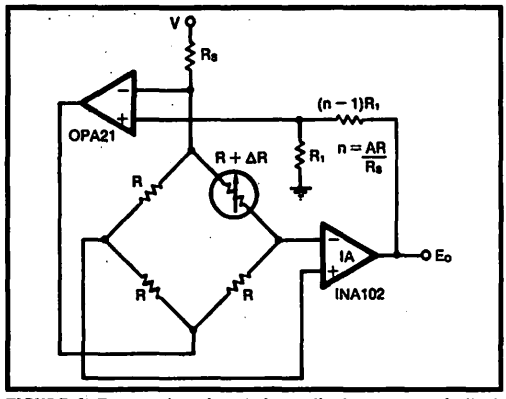


FIGURE 5. For negative-gain polarity applications, op amp feedback drives the current-setting amplifier.

producing the following circuit response:

$$E_O = -\frac{A}{4}\left(\frac{V\Delta R}{R_S}\right) - AV_{OS}. \qquad (6)$$

The circuits just discussed allow you to cope with nonlinearity. But what about the other major source of bridge-instrumentation error, thermal drift? In all the foregoing circuit designs, the amplifier's input-offset-voltage thermal drift gets amplified four times as much as the transducer-deviation signal, thanks to the bridge's voltage-divider effects.

You can reduce these effects by applying op amp feedback control to the bridge. And you can use that technique without sacrificing response linearity. For example, using two op amps places all bridge elements under either fixed bias or feedback control (Figure 6).

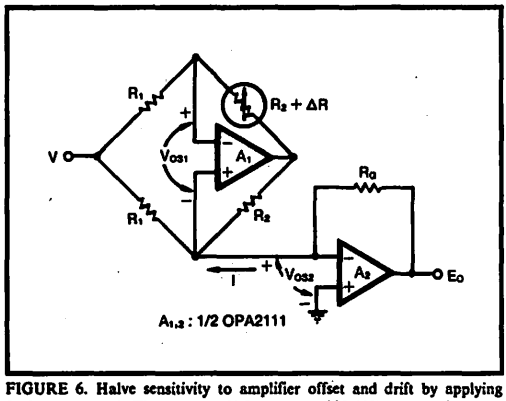


FIGURE 6. Halve sensitivity to amplifier offset and drift by applying feedback control. The scheme (U.S. patent 4,229,692) also avoids nonlinearity in bridge response.

The virtual ground at A_2's inverting input sets the voltage drop across the lower R_1 equal to V. And A_1's feedback translates this virtual ground to the upper R_1 bridge element so that both have an impressed voltage level equal to V.

Constant currents (equal to V/R_1) thus flow in both R_1 resistors, with the current in the upper R_1 also flowing through the transducer element in A_1's negative-feedback path. This current flow develops a voltage at A_1's output that drives a current through the bridge element in A_1's positive-feedback path.

If the bridge is balanced ($\Delta R = 0$), this current equals that flowing through the lower R_1 element, and $I = 0$. Any bridge imbalance alters R_2's current; I no longer equals zero, and the output becomes

$$E_O = \frac{A}{2}\left(\frac{V\Delta R}{R_2}\right) - AV_{OS1} + V_{OS2}, \qquad (7)$$

where $A = 2R_G/R_1$.

This is a very desirable response, for now the transducer-deviation signal $V\Delta R/R_2$ gets amplified by A/2—a 2:1 drop in relative sensitivity to V_{OS1} and its drift. A new offset term shows up in Equation 7, but it's not amplified. In addition, network response is linear.

The alternative configuration shown in Figure 7 offers some of the benefits afforded by the Figure 6 network. The amplified functions are quite similar, in fact. A_2, a current-to-voltage converter, establishes a virtual ground at one bridge node. At the opposite node, A_1 establishes a zero voltage and develops a constant-current supply for the transducer.

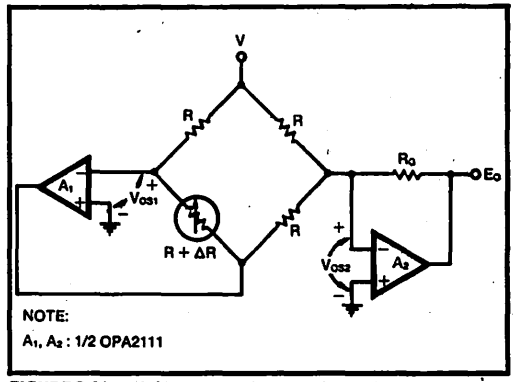


FIGURE 7. Linear bridge response is also achievable if you use inverting-only amplifiers. In some cases, you can also produce low drift using matched op amps.

Any transducer variation therefore generates a signal voltage at A_1's output, which in turn develops a signal current for A_2. At the network output,

$$E_O = \frac{A}{2}\left(\frac{V\Delta R}{R}\right) + A\,(V_{OS2} - V_{OS1}) + V_{OS2}, \qquad (8)$$

where $A = 2R_G/R$. This response illustrates the signal-gain/offset-gain improvement.

In certain applications, you can even realize high-performance bridge monitoring using only one op amp (Figure 8). Here, the network provides a linear response and retains a favorable sensitivity to amplifier offset and drift. The op amp's virtual ground removes output offset by forcing one of the bridge outputs to zero, producing the following zero-based signal:

$$E_O = -\frac{V\Delta R}{2R} + \left(1 + \frac{\Delta R}{2R}\right) V_{OS}. \qquad (9)$$

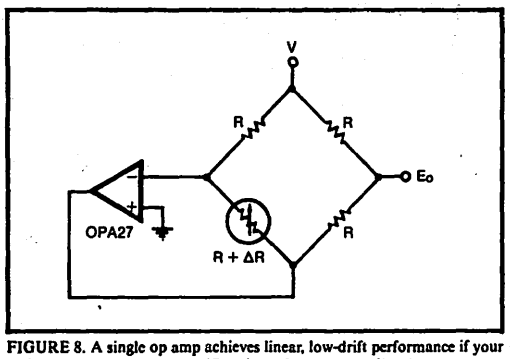


FIGURE 8. A single op amp achieves linear, low-drift performance if your design can tolerate a nonamplified signal from an unbuffered output.

Unfortunately, this circuit provides no amplification and doesn't accommodate heavy loading. Output resistance equals R/2, and heavy loading significantly attenuates the output signal. But these limitations present no problems if you're interfacing with a data-acquisition system that has its own input amplifier or where bridge output signal is sufficiently large to directly drive an A/D converter.

VOLTAGE GAIN IS JUST ONE OF THE MANY USES FOR INSTRUMENTATION AMPS

When compared with the highly versatile op amp, instrumentation amplifiers may appear rather typecast. Yet they can play more imaginative roles.

The traditional three-op-amp instrumentation amplifier is known for one trick: voltage gain. Yet it actually has quite a range of talents. By virtue of its independent feedback networks, the three-part configuration readily lends itself to a number of applications that discourage the use of individually packaged op amps.

Standard families of the device manage tasks such as summing multiple-amplifier outputs or deriving an input-guard drive signal. Other operations, like external common-mode rejection trim, current (rather than voltage) monitoring, and conversion from voltage to current all require only a small amount of external circuitry.

The functional range of a given instrumentation amplifier IC depends upon the access to its internal op amps. When pin connections to internal circuitry fall short, alternative means of achieving the desired function are often possible. Those techniques can often extend functions to other types of instrumentation amplifiers, as well.

The traditional instrumentation amplifier consists of a noninverting pair of input op amps, A_1 and A_2, followed by a difference amplifier (Figure 1). The input amplifiers depart from conventional configurations in that the normally grounded feedback resistor, R_G, is instead common to both of their feedback paths. That departure creates the differential input characteristic of the composite device.

Input signals e_1 and e_2 are transferred to the two ends of R_G through the feedback control of the two input op amps. The voltage across R_G, then, is the difference between the two input signals, creating a common feedback current. From that current, amplified differential voltages e_1(out) and e_2(out) are developed at the outputs of A_1 and A_2.

To better visualize that differential operation, use the superposition principle, separately considering the two inputs to be grounded and then combining the output results. With either input grounded, the virtual ground of the corresponding op amp places the other input amplifier in the normal noninverting configuration.

Feedback current from the noninverting amplifier also flows through the feedback loop of the grounded input amplifier, resulting in signals at the outputs of both A_1 and A_2. The differential amplifier formed by the third op amp subtracts one of those output signals, giving rise to a final output that is proportional to the difference between the two input signals.

Gain achieved by the differential signal is controlled by the resistance values of R_F and R_G, as expressed by $e_3(\text{out}) = (1 + 2R_F)(e_2 - e_1)$, where e_3(out) is the differential output voltage and e_1 and e_2 are the input voltages.

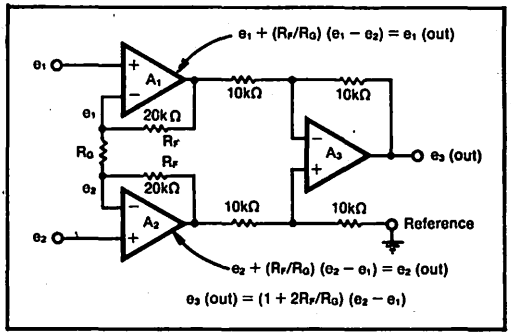


FIGURE 1. Two noninverting op amps with combined feedback, and a difference amplifier form an instrumentation amplifier with many design options.

While voltages common to the two inputs create no signal on R_G and therefore no feedback currents, they do transfer with unity gain to the outputs of A_1 and A_2. Those common voltages represent the common-mode input signal, and must be rejected by the differential amplifier for it to deliver its final output signal.

Common-mode rejection (CMR) is directly and critically dependent upon the ratio matching of the four resistors connected to the third op amp. The effect of any mismatch, however, occurs only after the differential signal has received its gain. Higher gains, then, must be accompanied by higher CMR. That is especially important to low level differential signals that are subject to large common-mode noise.

If the packaged chip allows access to all of the inputs and outputs of the three-op-amp device, several functions can be added with very little effort. They include signal summation, guard drive, common-mode rejection trim, current measurement, and current output. In the cost-conscious real world, however, the number of pins in a package are limited. Monolithic op amps, designed for the most common application, may often lack the means to easily implement the applications mentioned above. But there are other ways to perform them.

SIGNAL SUMS

No special circuitry is needed for signal summation. The traditional summing op amp is unnecessary with instrumentation amplifiers, since the latter generally use a reference pin to set the quiescent state of the output voltage. The reference normally is grounded to set the output voltage at zero in the absence of an input signal. In other cases, it is biased at some DC level to create an output offset voltage. Such an offset often is necessary to restrict the output to one polarity for circuits that cannot handle bipolar inputs, like analog-to-digital converters.

Another option is to drive the reference point with a signal. That makes an output that is referenced to the driving signal, which means the two are added. There, the output signal from A_2 is summed into the signal path of A_1 on the latter's internal register divider (Figure 2). Carrying that approach further, any number of such amplifiers could be interconnected in a chain, each one driving the reference point of the next. The output of the last link would be the sum of all of the output signals.

Still further, any other signal source in a system—say, the output of an op amp—can be connected to the reference point to be summed. The only requirement of the driving source is a very low output impedance. Otherwise, impedances so introduced can severely degrade the instrumentation amplifier's CMR by unbalancing the internal resistor networks.

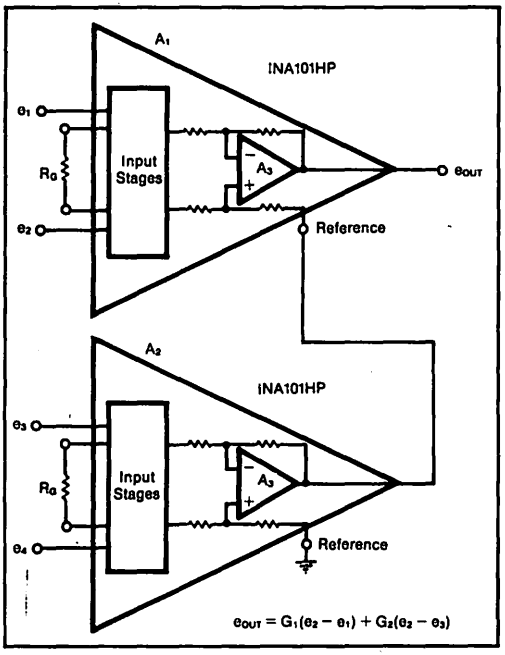


FIGURE 2. Signal summation is accomplished by driving the common reference point of an instrumentation amplifier with the output signal of another amplifier.

Common-mode rejection is so important to instrumentation amplifiers that two other techniques are frequently used to optimize that function: guard-driving input cable shields and external common-mode rejection trimming.

Driving the guard (shield) helps to preserve CMR from degradation by the capacitances of input cables.

When the coaxial shields of input cables are grounded, their capacitances, together with the source resistances, form low-pass filters as seen by the two amplifier inputs. Unless extremely well matched, those parasitic filters attenuate the common-mode signal differently on each input line. Thus attenuated, the common-mode signals create differential error signals that can dramatically degrade CMR. (Only a 0.01% attenuation difference will limit CMR to 80dB from a possible 100.)

NO PERFECT MATCHES

Because it is impractical to match the parasitic filters that closely, the common-mode signal should be removed from the cable capacitances instead. To do that, the cable shields are driven with a common-mode signal, leaving only the differential signal on their capacitances. The guard-drive signal, however, does not exist as a separate entity; it must be extracted from the two inputs.

An average of the input signals, the guard-drive is sometimes made available in more specialized, three-op-amp instrumentation amplifiers, such as the INA104. There, the signal is extracted with a two-resistor summing network (Figure 3a).

The network is connected between the outputs of the first two amplifiers and is driven by equal and opposite components of the amplified differential signal. Their effects sum to zero at the divider's center tap. The signal's common-mode component, however, is present at the outputs of both A_1 and A_2. That causes the center tap to follow that signal, and extract it.

Most of the economical instrumentation amplifier ICs, lacking the internal resistor network, must derive the common-mode signal in another way. The gain-set resistor is replaced with two resistors of equal value ($R_G/2$) to form a summing point (Figure 3b). Here, the common-mode signal is taken at the inputs of the first two amplifiers, rather than at their outputs.

Using superposition, one can see that if $e_2 = 0$, the signal at the junction of the two gain-set resistors will be $e_1/2$. That signal would be $e_2/2$ in the opposite condition ($e_1 = 0$), so the net common-mode signal at the junction of the two gain set resistors is $(e_1 + e_2)/2$. Its accuracy depends on the match between the two gain-set resistors, but that is not overly critical. Even a 1% mismatch still offers a 100-to-1 improvement over the undriven shield.

A buffer amplifier must be added to isolate the gain-set resistors from the cable's parasitic capacitances. Those capacitances can degrade the frequency stability of the input amplifiers by creating a differentiator-type feedback. The buffer removes the signal currents of the cable capacitances from the instrumentation amplifer's feedback, otherwise, those currents could create gain-peaking or oscillation.

NOT WITHOUT BIAS

While the buffer amplifier does inject its input bias current into that feedback, the result is a common-mode effect that is rejected by the difference amplifier. The added buffer should have a slew rate at least as great as the instrumentation amplifier's to avoid increasing the transient common-mode signals that remain on the cable-shield capacitances.

Though CMR may be very precisely trimmed at the wafer level, subsequent assembly operations can cause slight resistor shifts. Later, the completed device is most

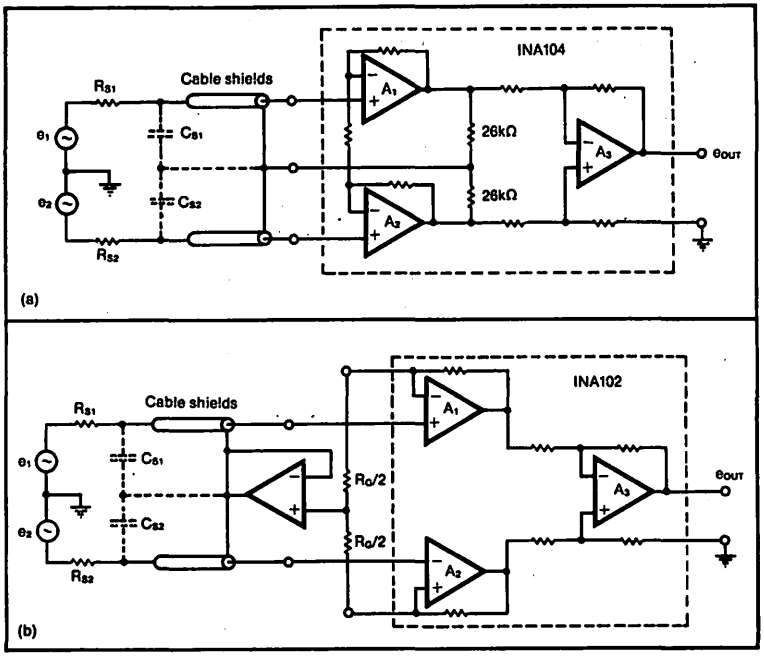


FIGURE 3. A guard-drive signal is included in some instrumentation amplifiers (a). It can be derived from others by splitting the gain-set resistor (b).

commonly fine-tuned through pin connections at the two inputs of the third op amp. Those pins permit parallel adjustment resistors to be added at the output or the common reference points. Such adjustment also alters gain accuracy, but to a relatively insignificant degree.

With no access to the conventional CMR trim points, ICs like the INA101 have only one possibility. A compensation resistor can be added in series with the reference point, for adjustment in one direction. That, of course, works only half the time—when increasing the resistance. A negative adjustment requires a different approach. The balance of positive and negative feedback around an external op amp can be controlled with a potentiometer, increasing CMR by 20dB or more at all gain levels (Figure 4). At a gain of 100, that parameter for the INA101 can be adjusted to 130dB. Of course, the resistors must be very closely matched (to within 0.6ppm, after a thorough warm-up) before the trim. Afterwards, the common-mode error signal becomes lost in the circuit noise.

Current conducted into that circuit from the instrumentation amplifier will develop a positive voltage on the first resistor it encounters. However, that current continues through the negative feedback resistance connected to the op amp A_4, and results in a negative voltage at that amplifier's output.

That voltage, in turn, is fed back to the op amp's noninverting input and pulls it negative. Since amplifier A_4's inverting input must follow, it too swings negative If

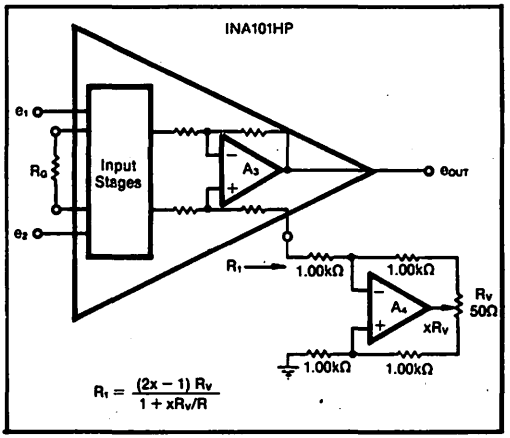


FIGURE 4. When lack of access to internal nodes rules out conventional CMR trim, a potentiometer circuit can serve that purpose.

it swings far enough, a net negative voltage change is presented to the instrumentation amplifier. In that case, a current in the compensation circuit produces a negative voltage by means of a negative resistance.

The polarity and magnitude of this resistance are determined by the two feedback paths controlled by potentiometer R_V. Its value is described by the circuit input resistance, expressed as $R_I = (2x - 1)\,R_V/1 + xR_V/R$.

Error introduced by the CMR trim amplifier can be kept small. That amplifier's input offset voltage and input voltage noise are transmitted directly to the instrumen-

tation amplifer output without gain. The op amp's input offset current, combined with the noise of the input bias currents, create similarly transmitted error voltages through a resistance (R).

Bandwidth limitations of the trim amplifier are not likely to be encountered, since its net negative feedback factor is one-half. Long before the op-amp trim effects begin to degrade, the AC roll-off of the instrumentation amplifier CMR will have dominated.

A side benefit of this CMR trim technique is simplified output offsetting. As noted, the ground reference point of an instrumentation amplifer is frequently connected to an offset voltage to convert its output to a unipolar signal. Since resistance to ground strongly affects CMR, the voltage source used must be of very low impedance, typically requiring a buffer amplifier.

The CMR trim circuit described above, however, eliminates the buffer amplifier by connecting the trim circuit's ground reference to the offsetting voltage source instead. Small resistances at that source that would have degraded CMR can instead be counteracted by the trim circuit adjustment.

CURRENT APPLICATIONS

Though instrumentation amplifiers are usually applied to voltages, they also work with current signals. In current-loop instrumentation, the ideal is to monitor the current at a floating junction without introducing a voltage drop in the loop.

Since the floating voltage is a common-mode signal, that is just where amplifiers with good CMR excel. Generally, a loop-signal current is detected by inserting a sense resistor into the loop and measuring the differential voltage drop across it. (Instrumentation amplifiers typically serve that purpose in their voltage mode.) Each such voltage drop, however, subtracts from the total voltage range available for load is then restricted.

Configuring the instrumentation amplifier for current input results in an essentially ideal ammeter (Figure 5). The loop voltage drop is eliminated while the CMR continues to remove the floating voltage. Such an ammeter accepts an input current, measures it, and returns it to the loop without introducing a voltage drop. The zero voltage-drop condition is assured by shorting together the gain-set terminals ($R_G = 0$).

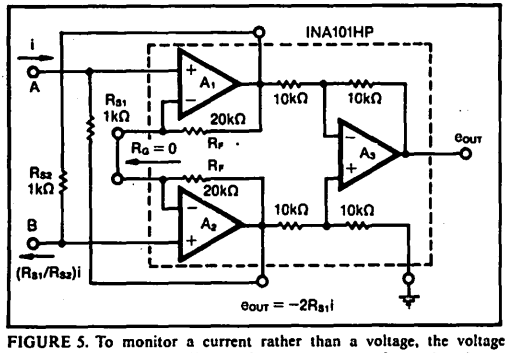


FIGURE 5. To monitor a current rather than a voltage, the voltage feedback of the input amplifiers is disabled and current feedback paths are provided instead.

Virtually no differential input voltage is required to cause the input amplifiers to respond. At first, it may seem that shorting R_G demands infinite gain of the two input amplifiers, but alternate feedback has been added. Specifically, voltage feedback has been supplanted by current feedback through the resistors labelled R_{S1} and R_{S2}. Those resistors carry the sense voltage that would otherwise have been introduced to the current loop.

Current input to terminal A will be returned to the loop through terminal B by the added current feedback. Current supplied to terminal A will cause the output of A_1 to rise, delivering a current to terminal B. The amount of that current is controlled by the fact that the output voltage rise of A_1 also causes current flow in its own feedback to be delivered to A_2 through the shorted gain-set terminals. That delivered current drives the output of A_2 negative, so that A_2 draws current through its sense resistor R_S, fed back from terminal A.

At equilibrium, the current drawn by A_2 will equal that delivered by A_1. That equality is ensured by matching the two sense resistors, unless gain or attenuation are desired. In that case, the two resistors can be scaled.

Because the voltage at terminals A and B may very likely float with respect to ground, the effects of the floating voltage must be removed. The floating voltage is common to the two input terminals, since no voltage drop appears between the two. It is transferred directly to the outputs of A_1 and A_2 and presented to the inputs of the differential amplifier.

SEE THE DIFFERENCE

Just as in voltage mode, the differential amplifier responds only to the output difference between the input amplifiers, and rejects the common-mode (floating) signal. The net result is a ground-referenced output voltage that is proportional to the input current.

Current-loop-based instrumentation also depends upon current output devices in its signal processing. While the connection above accommodates current inputs, other provide current outputs; alternatives exist for pin-restricted cases.

Current output is normally accomplished by connecting the common reference point of the instrumentation amplifier to its output (Figure 6a). That configures the difference amplifier as a common current source, but with differential inputs. The instrumentation amplifier becomes a differential-input, voltage-controlled current source and finds uses in test systems, as well as current-loop instrumentation.

The output for that voltage-controlled current source is the noninverting input of the third op amp. Any load resistance (Z_L) connected to that point should not exceed the value of the difference amplifier's internal resistors. Larger load resistances introduce the chance of frequency instability stemming from the positive feedback created

by connecting the reference point to the output.

To make the normal negative feedback dominant, the positive feedback factor is made lower thorugh the control of the load resistance. The load should significantly shunt the internal resistors, which are typically 10kΩ. That load restriction limits the load voltage swing, as it will be only a part of the instrumentation amplifier's output swing.

Again, many of the more economical one-chip instrumentation amplifiers will not include a pin connection for normal current output. The addition of an op amp, however, fixes that problem (Figure 6b). Here, the op amp floats the instrumentation device on the load voltage. With the instrumentation amplifier's own load bootstrapped, the load's current is delivered to the final current output.

In such operation, the input and output of the op-amp follower appear to be grounded. An input signal then creates an amplified replica of the signal voltage and a corresponding current on resistor R_S.

Actually, that current is delivered to the current-output load by bootstrapping the instrumentation amplifier common point, and buffereing the current drain of the amplifier common return. Driving the common return removes the signal of the current-output load from R_E, so that current in the latter is controlled only by the input signals. The added op-amp buffer removes the effects of the instrumentation amplifier's ground-return current from the final current output.

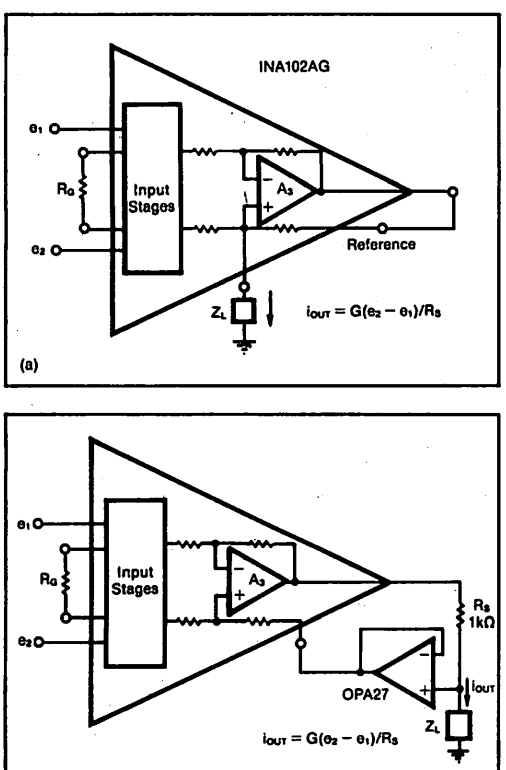


FIGURE 6. Current output is attained by reconfiguring the difference amplifier when the needed circuit points are supplied (a), or by bootstrapping the amplifier from the load when they are not (b).

AN ERROR ANALYSIS OF THE ISO102 IN A SMALL SIGNAL MEASURING APPLICATION

High accuracy measurements of low-level signals in the presence of high isolation mode voltages can be difficult due to the errors of the isolation amplifiers themselves.

This error analysis shows that when a low drift operational amplifier is used to preamplify the low-level source signal, a low cost, simple and accurate solution is possible.

In the circuit shown in Figure 1, a 50mV shunt is used to measure the current in a 500VDC motor. The OPA27 amplifies the 50mV by 200 × to 10V full scale. The output of the OPA27 is fed to the input of the ISO102, which is a unity-gain isolation amplifier. The 5kΩ and 1kΩ potentiometers connected to the ISO102 are used to adjust the gain and offset errors to zero as described in the ISO102 data sheet.

SOME OBSERVATIONS

The total errors of the op amp and the iso amp combined are approximately 0.6% of full-scale range. If the op amp had not been used to preamplify the signal, the errors would have been 74.4% of FSR. Clearly, the small cost of adding the op amp buys a large performance improvement.

After gain and offset nulling, the dominant errors of the iso amp are gain nonlinearity and power supply rejection. Thus, well regulated supplies will reduce the errors even further.

The RMS noise of the ISO102 with a 120Hz bandwidth is only 0.18mVrms, which is only 0.0018% of the 10V full-scale output. Therefore, even though the $16\mu V/\sqrt{Hz}$ noise spectral density specification may appear large compared to other isolation amplifiers, it does not turn out to be a significant error term. It is worth noting that even if the bandwidth is increased to 10kHz, the noise of the iso amp would only contribute 0.016%FSR error.

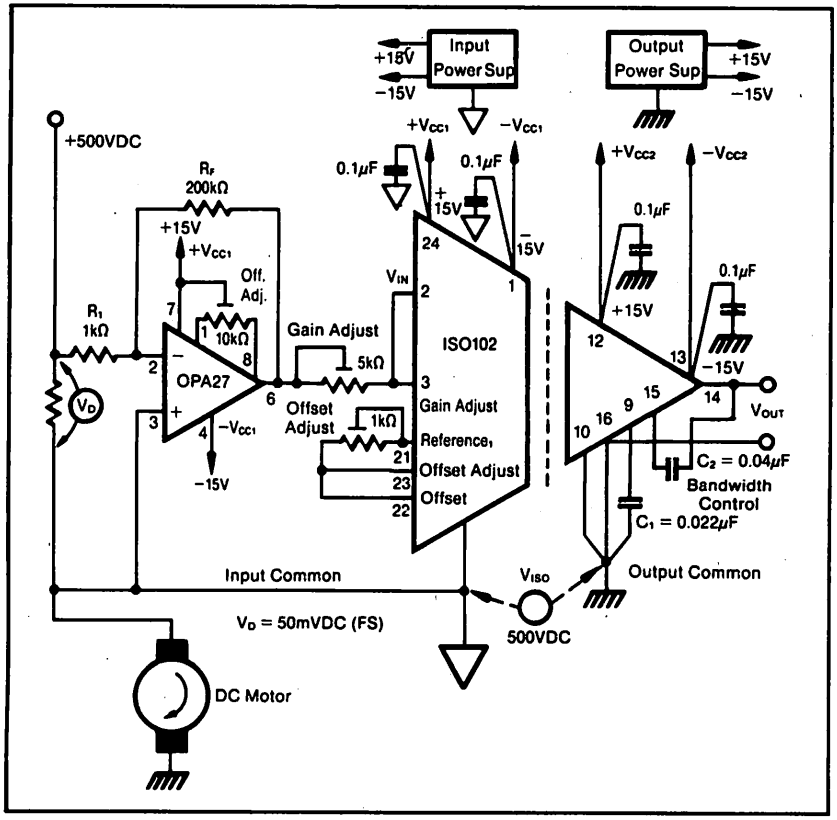


FIGURE 1. 50mV Shunt Measures Current in A 500VDC Motor.

The Errors Of The Op Amp At 25°C (Referred To Input, RTI)

$$V_{E\,(OPA)} = V_D \left[1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right] + V_{OS}\left[1 + \frac{R_1}{R_F}\right] + I_B R_1 + P.S.R. + Noise$$

$V_{E\,(OPA)}$ = Total Op Amp Error (RTI)

V_D = Differential Voltage (Full Scale) Across Shunt

$\left[1 - \frac{1}{1 + \frac{1}{\beta A_{VOL}}}\right]$ = Gain Error Due to Finite Open Loop Gain

β = Feedback Factor

A_{VOL} = Open Loop Gain at Signal Frequency

V_{OS} = Input Offset Voltage

I_B = Input Bias Current

P.S.R. = Power Supply Rejection (μV/V) [Assuming a 20% change with ±15V supplies. Total error is twice that due to one supply]

Noise = $5nV\sqrt{Hz}$ (for 1kΩ source resistance and 1kHz bandwidth)

$ERROR_{(OPA)}$ (RTI)		GAIN ERROR		OFFSET		P.S.R.		NOISE
$V_{E\,(OPA)}$	=	$50mV\left[1 - \frac{1}{1 + \frac{1}{10^6/200}}\right]$		$\left[0{,}025mV\left(1 + \frac{1}{200}\right) + 40 \times 10^{-9} \times 10^3\right]$		[20μV/V × 3V × 2]		[$5nV\sqrt{120}$ (nVrms)]
	=	0.01mV		[0,0251mV + 0,04mV]	+	0.12mV	+	$0{,}055 \times 10^{-3}$mVrms
Error as % of FSR	=	0.02%	+	[0.05% + 0.08%]	+	0.24%	+	0.00011%
After Nulling								
	=	0.01mV	+	[0mV + 0mV]	+	0.12mV	+	0.055×10^{-3}mVrms
	=	0.13mV						
Error as % of FSR*	=	0.02%	+	[0% + 0%]	+	0.24%	+	0.00011%
	=	0.26% of 50mV						

*FSR = Full-Scale Range. 50mV at input to op amp, or 10V at input (and output) of ISO amp.

The Errors Of The ISO Amp At 25°C (RTI)

$$V_{E\,(ISO)} = \frac{1}{200}\left[\frac{V_{ISO}}{IMR} + V_{OS} + G.E. + Nonlinearity + P.S.R. + Noise\right]$$

$V_{E\,(ISO)}$ = Total ISO Amp Error

IMR = Isolation Mode Rejection

V_{OS} = Input Offset Voltage

$V_{ISO} = V_{AMV}$ = Isolation Voltage = Isolation Mode Voltage

G.E. = Gain Error (% of FSR)

Nonlinearity = Peak-to-peak deviation of output voltage from best-fit straight line. It is expressed as ratio based on full-scale range.

P.S.R. = Change in V_{OS}/10V × Supply Change

Noise = Spectral noise density × $\sqrt{\text{bandwidth}}$. It is recommended that bandwidth be limited to twice maximum signal bandwidth for optimum dynamic range.

$ERROR_{(ISO)}$ (RTI)		IMR		V_{OS}		G.E.		NONLINEARITY		P.S.R.		NOISE
$V_{E\,(ISO)}$	=	$\frac{1}{200}\left[\frac{500VDC}{140dB}\right.$	+	70mV	+	$20V \times \frac{0.25}{100}$	+	$\frac{0.75}{100} \times 20V$	+	3.7mV × 3V × 2	+	$\left.18\mu V\sqrt{120}\text{ (rms)}\right]$
	=	$\frac{1}{200}$ [0.05mV	+	70mV	+	50mV	+	15mV	+	22.2mV	+	0.175mVrms]
Error as % of FSR	=	0.0005%	+	0.7%	+	0.5%	+	0.15%	+	0.22%	+	0.00175%
After Nulling												
$V_{E\,(ISO)}$	=	$\frac{1}{200}$ [0.05mV	+	0mV	+	0mV	+	15mV	+	22.2mV	+	0.175mVrms]
	=	$\frac{1}{200}$ [37.2mV]										
	=	0.19mV										
Error as % of FSR	=	0.0005%	+	0%	+	0%	+	0.15%	+	0.22%	+	0.00175%
	=	0.37% of 50mV										
Total Error	=	$V_{E\,(OPA)}$	+	$V_{E\,(ISO)}$								
	=	0.13mV	+	0.19mV								
	=	0.32mV										
	=	0.64% of 50mV										

HYBRID ISOLATION AMPS ZAP PRICE AND VOLTAGE BARRIERS

Two hybrid amplifiers cut a novel path to high-voltage isolation. They spare designers from having to engineer difficult solutions themselves.

If any device tests an analog designer's ingenuity, it is an isolation amplifier. Its job is to pass precise analog signals—safely and without degradation—between two points that may differ by hundreds, even thousands, of volts. Even though the high voltage may be damaging and noisy, it is often there by design, and sometimes because of a fault in the system.

Ideally, an amplifier should be small, hermetically sealed, reliable—and inexpensive. Standard devices have included modular and hybrid isolation amplifiers, now available for more than 10 years. Yet because of the stringent requirements of most applications, some 80% of all amplifiers in use are in-house designs.

A family of isolation amplifiers aims at relieving engineers of the chore of designing their own. The family's first two members, the ISO102 and ISO106, are rated respectively at 1500V and 3500V. Both are unity-gain buffers. Operating from −25° to +85°C, they dissipate 900mW. Each device is easy to make, electrically and mechanically rugged, inexpensive, and isolates better than any now available by an order of magnitude.

As three-chip hybrids, the amplifiers have from the start been designed to solve economically the problems that up to now have limited the use of off-the-shelf units. Key to keeping costs down is a capacitive-coupling approach to isolation. Any amplifiers so far available with the same capabilities are costly, enlisting magnetic or optical techniques to bridge the high-voltage barrier. Whether hybrids or modules, they are all multidevice circuits requiring complex assembly procedures.

The least expensive competitive device, for example, is rated at half the ISO102's rms voltage, yet costs twice as much.

The two new units, on the other hand, combine innovative packaging to their novel approach to high-voltage isolation. Each of the amplifiers is housed in a low-profile, side-brazed 0.6-in.-wide ceramic DIP (see "Building a Hermetically Sealed Isolation Amp").

DIFFERENT VOLTAGE, DIFFERENT LENGTH

The only physical difference between the two amplifiers lies in the different lengths needed for withstanding their respective isolation voltages—the voltage across the barrier. The ISO102 is in a 24-pin package, the ISO106 in one for 40 pins. However, to maximize isolation, all but 16 pins—8 at each end of the packages—have been eliminated. External spacing between conductive materials on opposite sides of the barrier is 390 mils for the 1500V ISO102, 1180 mils for the 3500V ISO106.

Because of that construction, their isolation-mode rejection ratio (IMRR), a key specification similar to common-mode rejection ratio (CMRR), is guaranteed to be at least −125dB at 60Hz. (The IMRR is found by taking the change in the amplifier's output-signal voltage caused by a change in the voltage across the barrier, and dividing it by the barrier-voltage change.) While not a function of ambient temperature, IMRR, like CMRR, rolls off with frequency at 20dB per decade. However, unlike that of most other amplifiers, the IMRRs of the ISO102 and ISO106 hold their value at the rated isolation voltage.

Another unusual feature, even among hybrids built on ceramic substrates, is that they are hermetically sealed. Furthermore, many other devices incorporate organic packaging materials and therefore are subject to something called partial discharge, which can degrade a barrier continuously exposed to high AC voltages.

It is important to understand partial discharge when using isolation amplifiers. The phenomenon takes place as a localized breakdown of material, but the breakdown does not bridge the space across the barrier. The discharge-inception voltage depends on the insulation material and can be significantly less than the rated breakdown voltage.

Experiments show that a typical barrier's breakdown voltage will actually decrease with time if continuously exposed to partial discharge. Thus, for maximum reliability the isolation barrier must not be operated at an AC voltage beyond the point at which partial discharge starts.

Voids in the insulating material set the stage for the problem. Alternating electric fields can generate a localized plasma within the voids. A short burst of current flows for about 50ns as the pockets of plasma form, and measurement of this current indicates that

partial discharge is taking place. The plasma is usually destructive because ionic bombardment of the walls of the void creates excessive temperature on the wall surface.

Because the barriers of the ISO102 and ISO106 are made of ceramic they are not only virtually free of voids, but also able to stand high temperatures over long periods without damage. Moreover, partial discharge is much more prevalent in barriers insulated with organic materials, which are impossible to fabricate without voids and therefore more damageable by plasma.

In another innovative technique, the ISO102 and ISO106 feature coupling capacitors that jump the isolation barrier by using frequency modulation, a technique previously untried in isolation amps. The capacitors are simply 3pF thick-film devices deposited on the ceramic substrate at the time its tungsten metallization is laid down. The capacitors take the place of transformers or of a combination of LEDs and photo diodes.

The signal through the capacitors is a 1MHz frequency-modulated square wave; in effect it is a pseudo-digital waveform. It takes three proprietary chips to modulate and demodulate the ±10V input signal—one of them a phase-locked loop, the other two are voltage-to-frequency converters. One of the three, the encoder (which is the FM modulator) to which the floating signal is applied, is a voltage-controlled oscillator (VCO) with a center frequency of 1MHz (Figure 1). The ±10V input modulates the 1MHz signal ±500kHz. The VCO's output is through a pair of complimentary pulse trains, fo and $\overline{fo}$, that drive the two tungsten capacitors. The decoder on the other side of the barrier is formed by the phase-locked loop (PLL) and the second VCO.

The PLL chip contains a sense amplifier, the loop circuitry, and an output filter. The sense amplifier reshapes the pulse trains after they have been high-pass filtered by an RC network formed by the barrier capacitors and the chip's 3kΩ input resistors. The sense amplifier drives a digital phase and frequency detector that guarantees rapid phase-locking. The detector's output, in turn, feeds a 70kHz loop filter that drives the feedback VCO.

The pair of VCOs gives virtually identical transfer functions to modulation and demodulation. The accuracy of the isolation buffer thus depends only on the matching of the VCOs, not on their actual transfer function. The PLL forces the feedback VCO to run at the same frequency as the encoder VCO, something that occurs when the two have the same input voltage. The input voltage to the feedback VCO becomes the output (V_{OUT}) of the isolation amplifier after a second-order Butterworth low-pass filter removes residual carrier noise.

Each VCO chip also contains a 5V, 10ppm-per-degree-Celsius reference that controls the buffer's input and output offset voltages. The references are in effect independent 5V sources, each of which can supply up to 5mA to external circuits.

The easy-to-use buffers have gain and offset trimmed respectively to within 0.1% and 20mV while the chips are still on-wafer. Gain and offset errors may be trimmed through zero with a pair of input potentiometers.

Nominally, the chips on both sides of the barrier operate from split ±15V supplies; in practice they will operate anywhere between ±10 and ±20V. The device can put out 5mA and swing to within 3V of the rails. Indeed, because only the output supplies limit the swing, input voltage can actually exceed input supply voltage.

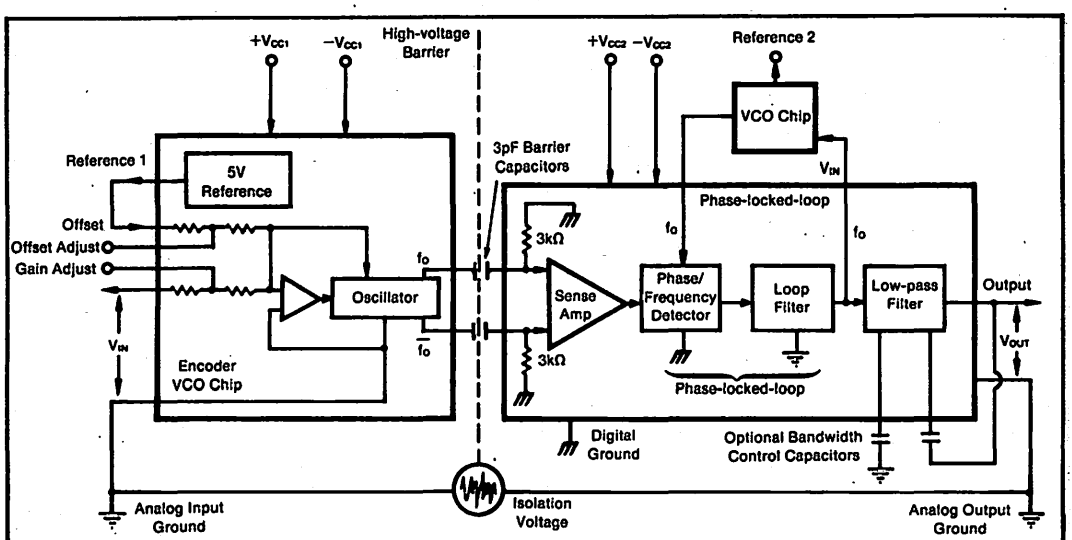


FIGURE 1. The ISO102 and ISO106, respectively rated 1500V and 3500V, transport their analog input signals across the high-voltage barrier on a pair of 3pF tungsten capacitors; to feed the input signal through the capacitors, the signal frequency modulates a 1MHz carrier in an encoder VCO; the signal is demodulated on the other side of the barrier by a matching feedback VCO and a phase-locked loop.

By adding a pair of small capacitors on the output side of the buffer, in parallel with the low-pass-filter capacitors, the designer can trade off between system bandwith and system dynamic range—maximum signal swing divided by the noise floor. Doubling the dynamic range quarters the bandwidth (Figure 1 again); adding 0.01 and 0.02μF capacitors boosts the dynamic range to 16 bits while cutting the bandwidth to 280Hz. Without the two capacitors, dynamic range is typically 12 bits, small-signal bandwidth 70kHz, and the 1MHz carrier appears as a 1mVp-p ripple on the output.

One common configuration for an isolation amplifier is a system with multiple channels isolated from each other as well as from their output side. At the output, the signals feed an A/D converter and a computer. An eight-channel system of this type can be built with eight ISO102 amplifiers for as little as $25 per channel (Figure 2).

One of the eight amplifiers drives an eight-channel analog multiplexer. A 5kΩ potentiometer trims the channel's gain to unity, while one of two 1kΩ potentiometers trims offset voltage to as close to zero as possible. The potentiometers can also trim other gain and offset errors in the channel. In addition, with 300pF and 600pF capacitors connected respectively to the C_1 and C_2 pins, small-signal bandwidth is reduced to 10kHz.

Isolated power for the eight separate amplifiers comes from the PWS740 series of DC/DC converter building blocks. One 400kHz PWS740-1 switch-mode control circuit drives eight PWS740-2 transformers in parallel, one for each channel.

Each transformer's output is rectified by a PWS740-3 diode bridge, while 0.1μF bypass capacitors on the isolation amplifier's power pins provide all the filtering needed. An LC π filter in the +15V line to the controller eliminates conducted EMI from the rest of the circuit.

To maintain a system's accuracy, a designer must take several limiting aspects of the amplifiers into consideration. For example, the modulation and demodulation technique imposes a limit on the isolation voltage's permissible slew rate.

Transients across the barrier that exceed 100V/μs can generate enough common-mode current in the capacitors to overdrive the decoding circuit. The effect is to interrupt accurate signal transmission for a moment, but no damage occurs because the devices are protected for transients to 100,000V/μs.

On the other hand, the rated IMRR prevails in the presence of a 7.5kHz, 1500Vrms sine wave because slew rate across the barrier does not exceed 100V/μs. For a rated IMRR, the rms value of the isolation voltage must be less than 11.3MV divided by the frequency in Hertz, as well as less than the rated isolation voltage.

The slew-rate limit is of concern only when the signal floats continuously on rapidly changing potentials. It need not be considered where isolation is only a factor under fault conditions, as in medical devices.

Typical among isolated systems is the kind with completely floating inputs powered by a high-frequency DC/DC converter, driven in turn by a logic supply on the barrier's output side. The likelihood then is that the supply's ground is the same as the buffer's digital ground.

In such a case, because the primary of the transformer is driven with a fast rising and falling rectangular waveform, the converter capacitively couples a charge to the

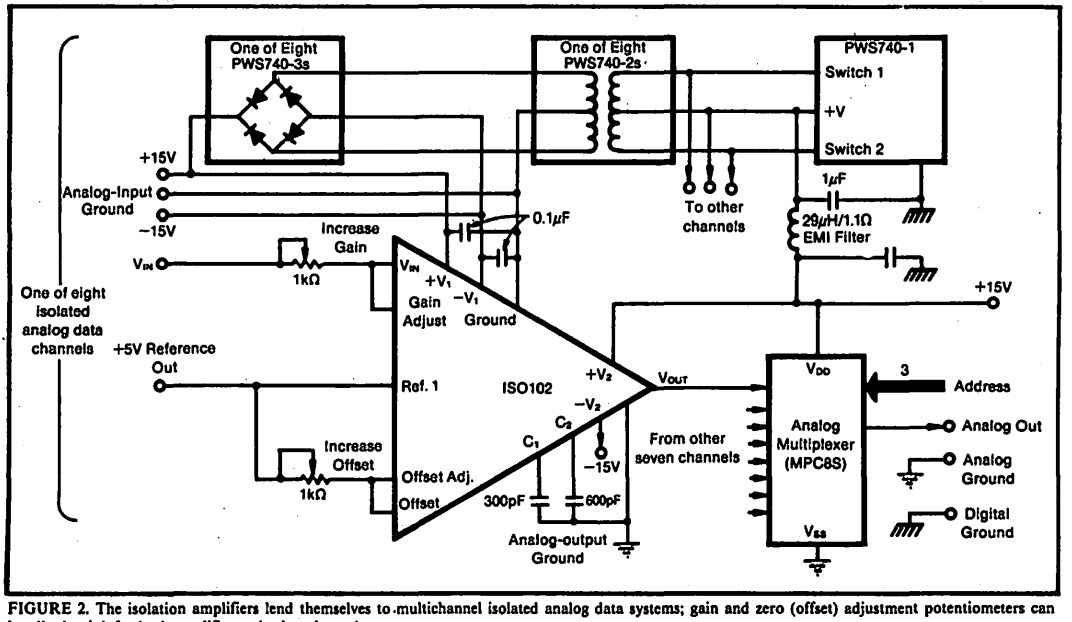


FIGURE 2. The isolation amplifiers lend themselves to multichannel isolated analog data systems; gain and zero (offset) adjustment potentiometers can handle that job for both amplifier and other channel errors.

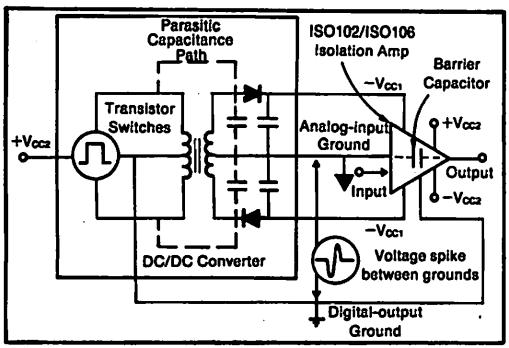


FIGURE 3. In some cases, like when a DC/DC converter drives the isolation amplifier, voltage rate of change is as important as voltage level. The reason is that the transformer's core and the barrier capacitors form a voltage divider, with a portion of the switching waveform appearing across it.

ground system of its output side (Figure 3). Moreover, the transformer's core and wiring capacitance form a path between the primary and secondary windings.

That path continues through the amplifier and its barrier capacitors to the digital ground. The transformer capacitance in turn forms a voltage divider with the barrier capacitors so that a portion of the switching waveform appears across them.

Any noise spikes between input and output grounds faster than 100V/μs and higher than 1Vp-p, will interfere with the buffer. Spikes can be reduced, however, by using bifilar wire for the transformer's primary and secondary windings; that is, winding each side of the center tap with a pair of twisted wires, rather than one wire. The result is a greater symmetry in the primary to secondary capacitance, reducing the coupled charge. Another method is to use an electrostatic shield between the primary and secondary windings.

BUILDING A HERMETICALLY SEALED ISOLATION AMP

The hardest part of making an isolation amplifier is building the high-voltage barrier. The barrier in the 1500V ISO102 and the 3500V ISO106 is an elegant and simple solution: a pair of 3pF capacitors form an integral part of the DIP that houses the amplifier.

Construction of the package starts with a 0.6-inch wide ceramic substrate. A layer of tungsten forms the amplifier's pin-to-die and die-to-die connections, as well as the spiral patterns of the barrier capacitors. Capacitance results from the fringing electric fields of adjacent lines of tungsten, which are 0.63mm apart.

Next, a layer of ceramic is fired on top of the substrate, embedding the capacitor in solid ceramic. The material's 15,000V-per-mm dielectric strength imparts a breakdown voltage in excess of 9000Vrms. The barrier's resistance is typically $10^{14}\Omega$. Windows in this second layer of ceramic form cavities for the amplifier's three integrated circuits—two voltage controlled oscillators and a phase-locked loop.

Metal patterns, including lid-seal rings and lead pads, are screened onto the layer and nickel-plated. The pins are brazed to the sides of the package and all exposed metal is plated with one micron of gold. The chips are then mounted in the finished package. After testing, the lids are soft-soldered over the two cavities, hermetically sealing the amplifier.

THE KEY TO UNDERSTANDING SOURCES OF ERROR IN THE ISO100 ISOLATION AMPLIFIER

A Practical Guide to Optimizing Accuracy

While most applications of the ISO100 do not require error correction, being aware of the adjustment options can be beneficial. Provisions for several types of error correction are included to allow the circuit designer to obtain maximum accuracy in a specific application. Adjustments can be made to null errors that are internal to the isolation amplifier, or in other parts of the system.

This application note describes how to quantify the effects of these potential errors, and to help identify the most appropriate means of correction. Each figure has a caption that gives a summary of the important ideas. Subjects to be covered include:

- Theory of operation
- Definition of terms
- Offset current (I_{OS})
- Gain error (A_e)
- Offset voltage (V_{OS})

THE ISO100

The ISO100 has several modes of operation: unipolar or bipolar, voltage or current input and inverting or non-inverting. The product data sheet for the ISO100 includes sections detailing both the error model and the theory of operation. Study of the data sheet is suggested. A simplified block diagram of the ISO100 is shown in Figure 1.

Signal transmission (across the isolation barrier) is accomplished through an optical coupler, which acts as a 1:1 current translator. Current at the input of the device is replicated on the output side of the coupler. The isolated output current (I_{out}) is forced to flow through R_f, by the summing node action of the output op amp.

At first glance it might seem unusual that the non-inverting input of the ISO100 is connected to the inverting input of the input op amp. However, this is due

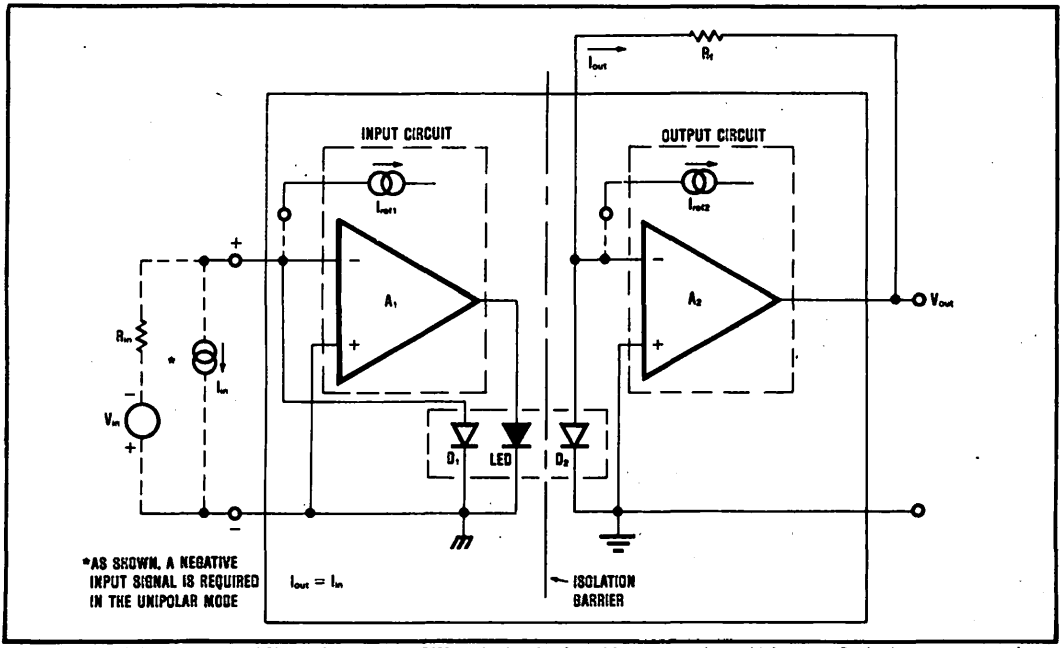


FIGURE 1. SIMPLIFIED ISO100 BLOCK DIAGRAM. The ISO100 can be thought of as a 1:1 current translator with its output flowing into a current to voltage converter. This isolation amplifier is inherently a current input device. However, since the input is a virtual ground, an input voltage can be converted to a current by simply including R_{in}. The optional I_{ref} connections are used to produce bipolar operation.

to two inversions in the signal path from isolation input to output. Care should be taken not to be confused on this point.

The resulting simplified transfer function for the ISO100 is given by:

$$V_{out}/I_{in} = (R_f)(1 + A_e).$$

Gain error (A_e) is defined as the deviation of the ratio, I_{in}/I_{out} from unity. It can be thought of as the "coupling error."

The optical coupler uses a matched pair of photo-diodes and a light emitting diode (LED) to produce signal transmission. Since an LED only works when current flows in one direction, the basic mode of operation is unipolar. In the unipolar mode, only negative input currents are allowed (ie: only currents out of the input produce a positive voltage to turn the LED on). Bipolar operation can be easily produced by internally offsetting the input from zero. Two matched current sources (I_{ref1} and I_{ref2}) are included in the ISO100 for this purpose. By connecting current source I_{ref1}, on the input side of the coupler, the amplifier is made to operate at half-scale (when the input current is zero). Connecting an equal source (I_{ref2}) on the output side, shifts the output voltage back to zero. This arrangement maintains a desirable "zero-in/zero-out" relationship, while allowing input currents of either polarity to be accepted.

THE ERROR MODEL

The model used to represent ISO100 errors is shown in Figure 2. Offset current (I_{OS}) is defined as the input current required to make the output voltage zero. In the unipolar mode, it is mainly composed of mismatches in the optical paths. I_{ref1} and I_{ref2} are the current sources that are optionally connected to produce bipolar operation. The major source of bipolar I_{OS} is the mismatch in I_{ref1} and I_{ref2}. The various contributions to the offset current are grouped together and are modeled as a single current source at the input. Keep in mind that I_{OS} has a sensitivity to temperature, supply voltage, common mode voltage and iso-mode voltage. However, it would be very rare that all of these factors would be significant. Analysis examples for these terms are found in the data sheet. It will be shown that gain error also introduces an offset current term. Voltage offsets (V_{OS}) are modeled as voltage sources at the inputs of each op amp. I_{D1} and I_{D2} represent the currents being generated by the photo-diodes. The currents are related by the equation:

$$I_{D2} = I_{D1}(1 + A_e).$$

These are internal currents which mathematically cancel in presenting the total transfer equation. The gain error (A_e) and the unipolar offset current (I_{OS}) cannot be directly altered. However, these terms can be considered constant for each amplifier, allowing their effects to be compensated by simple external means. For instance, the gain error is compensated by adjusting either R_f or R_{in}. Voltage offset can be trimmed as in most other op amps, using the trim pins provided. Offset current is trimmed by adjusting the magnitude of one of the reference currents (I_{ref1}, I_{ref2}). Because of the on-chip design, sampling or adjusting of the internal references does not have a detrimental effect on the isolation amplifier's performance. I_{OS} trim with an external input current is possible, but careful consideration should be given to the effects of temperature and supply voltage variations. Noise can also be an important error source. While not treated in this applicaiton note, information can be found in the product data sheet.

WHAT IS THE OUTPUT?

It is important to be able to calculate total worst case errors for a particular circuit configuration. Clearly, this is important for establishing incoming inspection criteria as well as circuit and system design.

Equation 2 in the ISO100 data sheet allows the user to solve for the output voltage under any conditions. This transfer equation (for the voltage mode) is repeated here:

$$V_o = R_f[(V_{IN}/R_{in} + V_{OSI}/R_{in} - I_{ref1} + I_{OS})(1 + A_e) + I_{ref2}] + V_{OSo}.$$

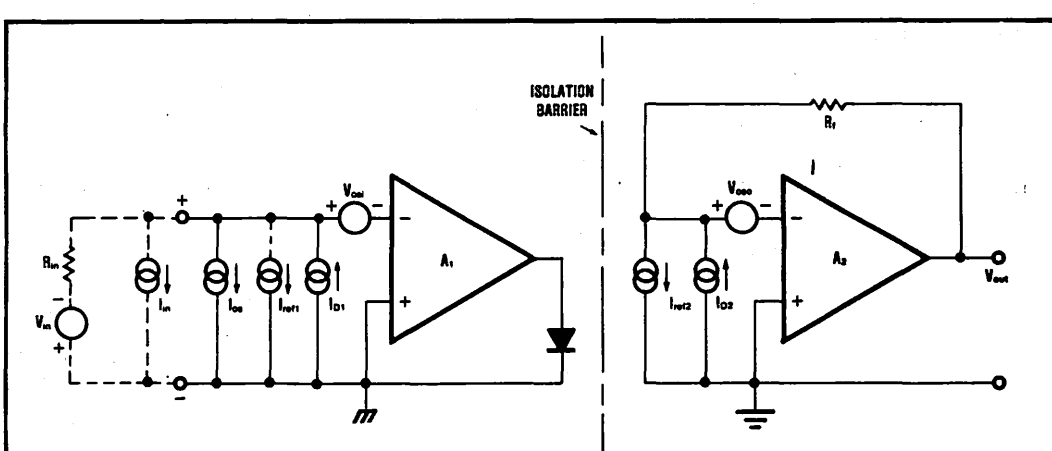


FIGURE 2. DC ERROR MODEL. V_{OSI} and V_{OSo} model the respective input offset voltages. There are several possible contributors to offset current. The composite effect is modeled with one current source, I_{OS}, at the input. The gain error (A_e) defines the relationship between I_{D1} and I_{D2} ($I_{D2} = I_{D1}[1 + A_e]$). While shown as separate sources, any mismatch in I_{ref1} and I_{ref2} are included in the I_{OS} term.

The transfer equation for an input current is:

$V_o = R_f[(I_{in} - I_{ref1} + I_{OS})(1 + A_e) + I_{ref2}] + V_{OSo}$

By substituting worst case numbers for all the error terms, the maximum error in the value of V_o can be determined as shown in example 1.

Example 1: An ISO100CP is to be tested at incoming inspection. The part is to be tested in a bipolar unity gain configuration. For the conditions of $R_f = R_{in} = 1Meg$ and $V_{in} = 0$, what output voltage would be within the specification limits?

The maximum values for the error terms are found in the data sheet. Inserting them into the output equation presented above:

$$V_{err} = 1Meg[\pm 200\mu V/1Meg - 12.5\mu A \pm 35nA)(1 \pm .02) + 12.5\mu A] \pm 200\mu V$$

$$V_{err} = \pm 286mV \text{ (maximum)}$$

±286mV would then be the range of permissible output voltage in this configuration.

A significant portion of the output error in the bipolar mode is due to the gain error. With no input,

$V_o \simeq R_f[I_{OS} - I_{ref}(A_e)]$.

The term that dominates is the reference current times the gain error. This error appears as an offset, and must be accounted for if the output is being measured to obtain the actual I_{OS}. Otherwise the user may wonder why an additional error is present in the output voltage measurement. The next example shows that this is not true for the unipolar mode of operation.

Example 2: Consider a unipolar, non-inverting, gain of one amplifier, as shown in Figure 3A. The output equation can be rewritten for the unipolar case as shown:

$V_o = R_f[(V_{in}/R_{in} + V_{OSi}/R_{in} - I_{OS})(1 + A_e)] + V_{OSo}$.

Error analysis proceeds as follows: unipolar operation is not defined at zero input current because the LED could be turned off, disabling the amplifier's internal feedback loop. V_{in} will be set to the minimum allowed value. The remaining errors are as specified in the data sheet. Note that the $V_{in\ (min)}$ specification of 20mV follows from the 20nA minimum input current specification for linear operation.

$$V_o = 1Meg[(-20mV/1Meg \pm 200\mu V/1Meg \pm 10nA)(1 \pm .02)] \pm 200\mu V$$

$V_o = -31mV$ (worst case, all errors negative)

Therefore, $V_{error} = V_o - V_{in} = \pm 11mV$.

CORRECTING THE ERRORS

The next logical step after calculating the errors is to reduce them. In the following discussion, each error is considered by itself. The suggested methods of trimming or adjusting errors are considered, and some general hints are presented.

OFFSET CURRENT ERRORS

Because the ISO100 is a current input device, the dominant error in most configurations will be the input offset current (I_{OS}). As stated above, I_{OS} is defined as the current, injected at the input, necessary to force the output to zero. In the unipolar mode, this definition has a limitation which must be understood. Zero output requires that I_{D2} be zero, implying that the optical feedback path is open. This condition is unsatisfactory for predictable performance. Therefore, a minimum input current must be maintained to assure that the amplifier is operating in its linear region. The transfer function is only defined when the net current at the input node flows out of that node. The unipolar I_{OS} term is extrapolated from this minimum practical current.

In the bipolar mode, no such limitation exists. In this mode the internal references keep the LED and photodiodes running at half-scale when the input is zero. I_{OS} can therefore be measured directly.

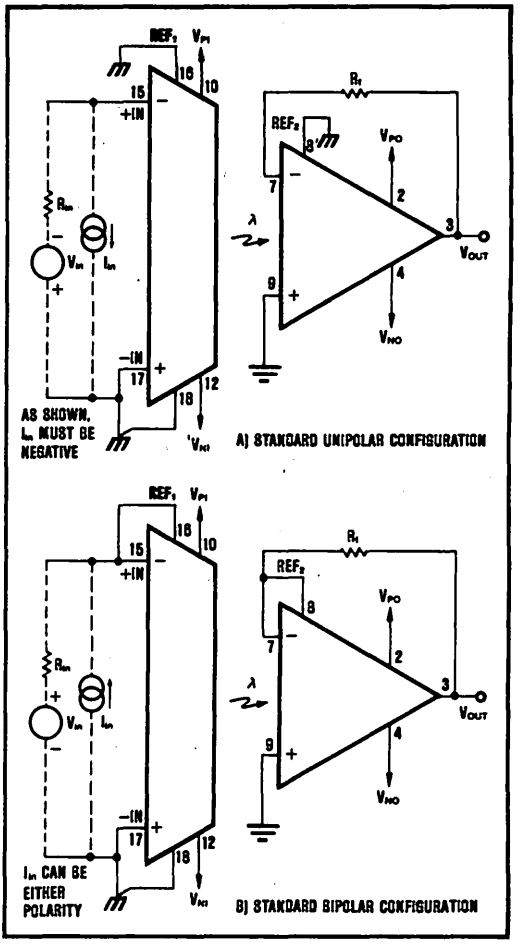


FIGURE 3. STANDARD CONFIGURATIONS. Most applications of the ISO100 will make use of these configurations, with slight variations. (A) shows the configuration for unipolar operation, which functions for negative inputs only. (B) shows how to use the internal references to provide bipolar operation. The circuits show all necessary connections and indicate the package pin numbers. Note that power supply connections (V_P and V_N) to the input and output stages must be "isolated."

I_{OS} ADJUSTMENTS

As suggested above, the internal references can be used to generate a compensation current to cancel I_{OS}. In Figure 4 a current divider is used to divert a small portion of the input stage reference current to the input node. Note that the direction of the current is negative. This additional current flowing out of the summing node behaves like any input signal, and thus causes more current to flow in R_f. The change in V_o is $-I_c(R_f)$, where I_c is the new (offset correcting) current. The graph of the transfer function shows how the curve is shifted by this adjustment.

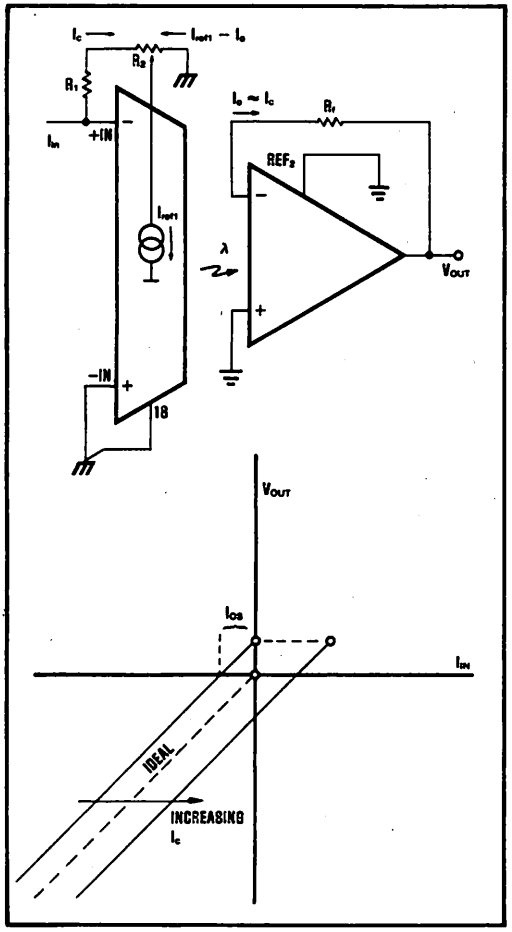


FIGURE 4. I_{OS} ADJUSTMENT FROM THE INPUT SIDE. If I_{OS} were negative, the ideal transfer curve would be shifted to the left, as shown above. This would cause a positive output voltage when there was no input current. Connecting a negative correction current, I_c, to the summing node of the first op amp causes the transfer curve to shift to the right. Thus, the effect of I_{OS} can be trimmed out.

Since the reference current is of fixed polarity, the curve can only be shifted in one direction with the above connection. However, the curve can be shifted the other way by making use of the output reference ($_{ref2}$). Figure 5 shows the effect of tapping a small current from this source and applying it to the input of the second stage. The nominal value of I_{ref} is 12.5 to 13μA.

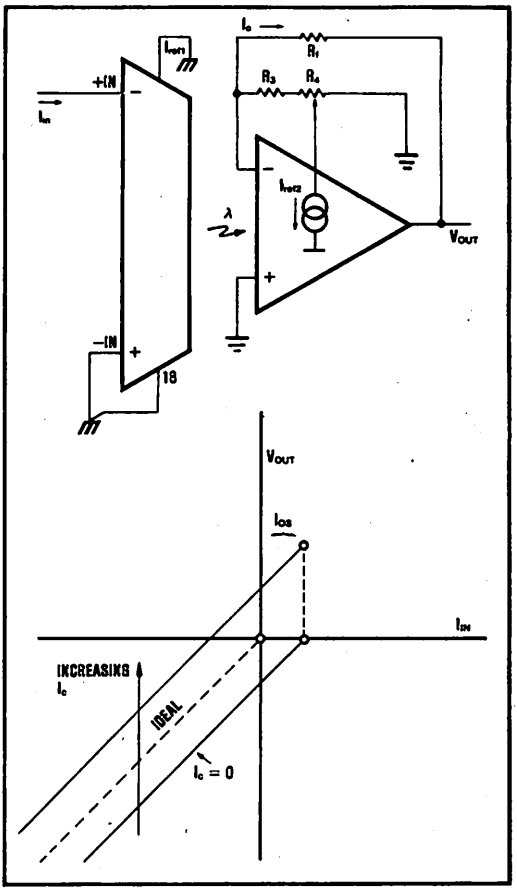


FIGURE 5. I_{OS} ADJUSTMENT FROM THE OUTPUT SIDE. Connecting a negative correction current (I_c) to the summing node of the output amplifier causes the transfer curve to shift upwards by the amount of I_c. This causes the output to shift back toward zero. Again, a current divider is used to derive the correction current from the internal references. By combining the methods of Figures 4 and 5, a correction current can be generated that will cancel either polarity of I_{OS}.

By using a combination of these two methods it is possible to always move the transfer curve to the ideal position. In Figure 6, the network in the input stage offsets the system in a known direction. The variable divider network in the output stage has enough range to move the output voltage through zero. It is worth repeating that the correction currents could be generated with resistive dividers connected to the power supplies, but using the internal references takes advantage of their inherent stability, accuracy, and power supply rejection.

Example 3: A common use of the circuit in Figure 6 might be to provide a "keep alive" current for the ISO100. This might be required in a unipolar application where it is possible for the input to go to zero. While it would be a little simpler to use the bipolar configuration, this would result in higher noise and increased quiescent current.

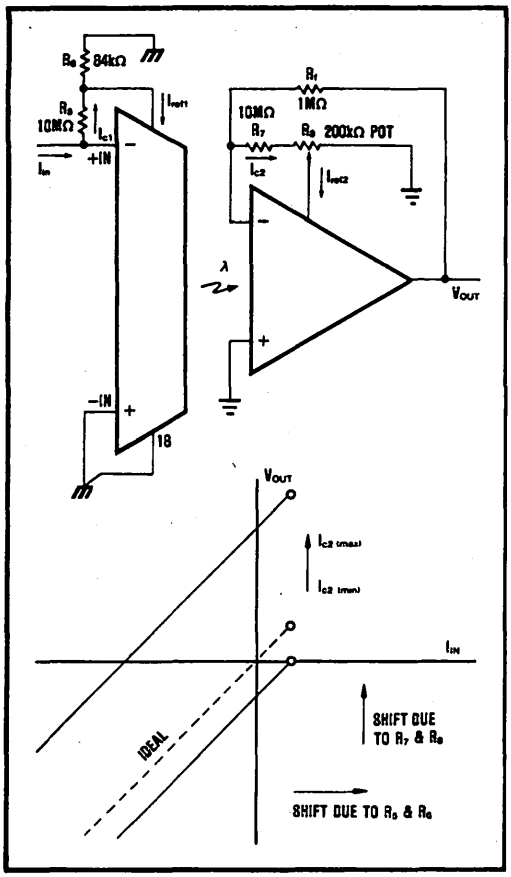


FIGURE 6. USING THE UNIPOLAR AMPLIFIER AT ZERO INPUT. The unipolar amplifier can be used down to zero input if it is made to be "slightly bipolar." By sampling the reference current with R5 and R6 the minimum current required to keep the input stage in the linear region of operation can be established. R7 and R8 are adjusted to cancel the offset created in the input stage. This brings the output to zero, when the input is zero. While the amplifier can now operate down to zero input voltage, it only has a small portion of the current drain and noise that the true bipolar configuration would have.

The circuit uses a fixed current divider in the input stage to ensure the direction of I_{OS}. A variable divider in the output stage allows the user to adjust the amplifier to be just "slightly bipolar." Enough current (20 to 30nA minimum) must be drawn from the input to fulfill the minimum unipolar requirement. Since only a small portion of the reference current is being used, a minimal increase in the noise will result.

A suggested value of I_{c1} is about 100nA (1% I_{REF}). Solving the resistive current divider network yields:

$$R5/R6 \simeq I_{ref}/I_{c1} = 120.$$

Practical resistor values would be: R5 = 10Meg, R6 = 84K. The adjustment range of I_{c2} should include I_{c1} and the built-in error sources (100nA + 20nA = 120nA). This yields: R7 = 10Meg, R8 = 200K.

GAIN ERROR ADJUSTMENTS

Gain error in the ISO100 is due mainly to mismatches in the optical cavity. These mismatches show up as an error in the ratio of the two photo-diode currents (ID1 and ID2).

As shown in Figure 7, a gain error will cause the transfer function curve to rotate about the quiescent operating point of the photo-diodes. The output stage functions as a current to voltage converter with a transconductance (gm) = $1/R_f$. Thus, changing R_f will also cause the line to rotate about the Q point. Therefore, in the unipolar mode, A_e is simply corrected by adjusting R_f.

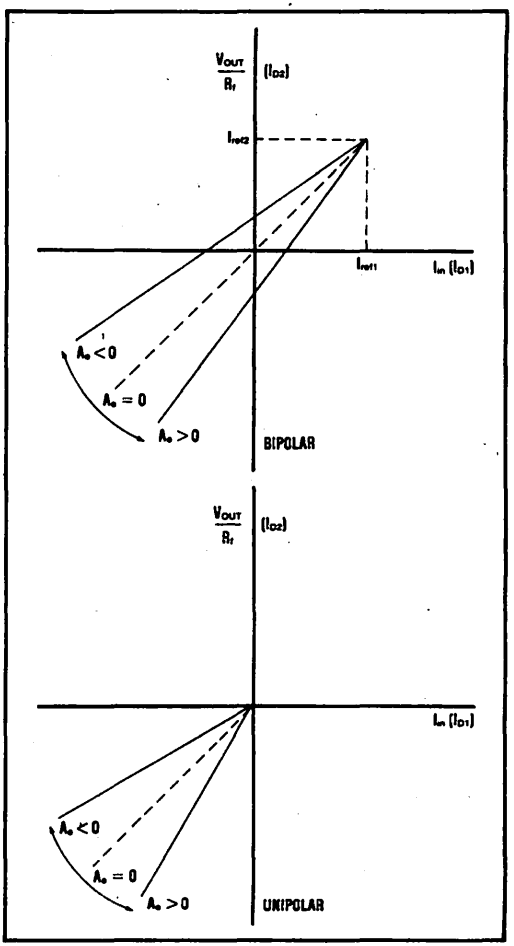


FIGURE 7. EFFECT OF GAIN ERROR (A_e). A_e will cause an error in the slope of the transfer function, rotating the line about a point determined by the quiescent current in D1 and D2. Unipolar, this point is near the origin. In the bipolar mode, the internal references cause this point to shift to the right and up as shown above. In either case, the change in slope is the same.

In the bipolar mode, gain adjustment is not quite so simple. Gain error will still cause the line to rotate about the photo-diode Q point, but that point is no longer near the origin. Figure 8 shows that changing either R_f or R_{in} will cause the transfer curve to rotate about the point where the input current is zero (as it does in the unipolar case). However, if the ratio R_f/R_{in} is changed to make up for A_e, an Ios term is introduced. This "Apparent Ios"

term is due to the fact that I_{ref2} will get divided by the gain error, but I_{ref1} will not. The difference in reference currents, as seen at the input, will be the apparent offset error (see Figure 9). This effect makes the trimming of gain error a two step process for bipolar applications. First, either resistor is adjusted to corect the slope of the line, then the I_{OS} is trimmed using the methods discussed earlier.

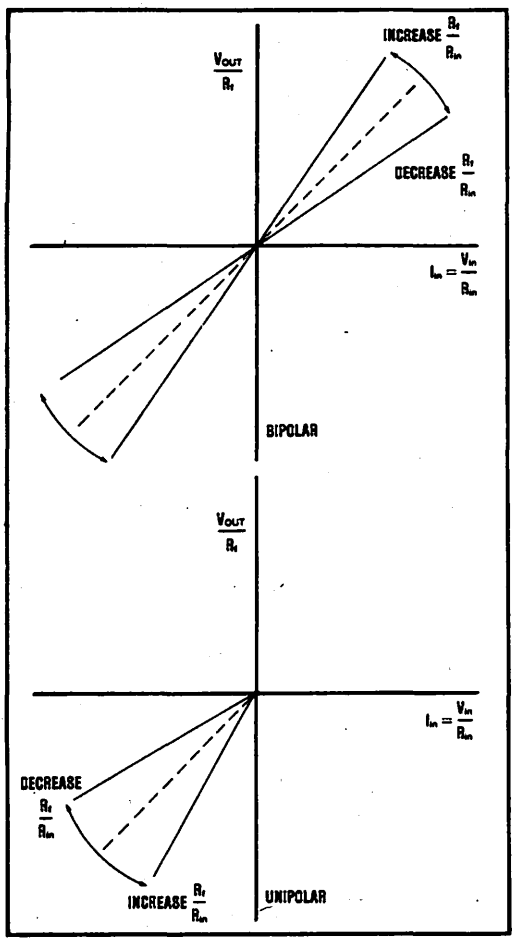


FIGURE 8. ADJUSTING THE GAIN. Changing the ratio R_f/R_{in} will change the gain by rotating the transfer function about the pont where $I_{in} = 0$. This will be true for both the unipolar and bipolar cases. I_{OS} is zero in these examples.

V_{OS} ADJUSTMENTS

While both the input and output amplifiers of the ISO100 have provisions for adjusting offset voltage, it is generally not necessary to do so because the contribution to total error is small. Only V_{OSI} has practical significance (in most applications), and then only when R_{in} is small. In most cases the output amplifier is configured so that it has a voltage gain of one, and as such its V_{OS} contribution will be insignificant. The output adjustment range via the V_{OSO} control will be only a few millivolts.

The input offset voltage (V_{OSI}) will affect the output only

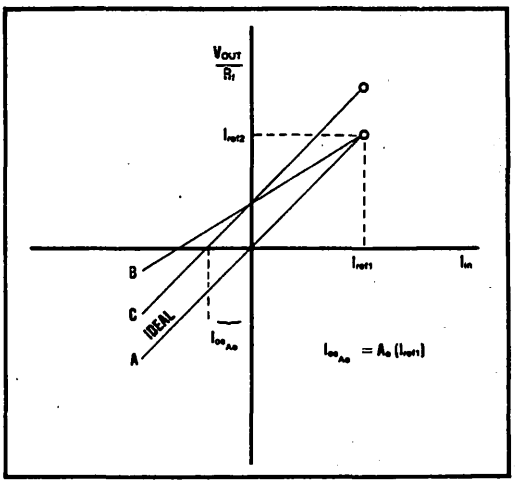


FIGURE 9. OFFSET INTRODUCED BY GAIN ERROR (BIPOLAR ONLY). The gain error (A_e) will cause an apparent I_{OS} term to appear when in the bipolar mode. A_e causes the ideal transfer line A to rotate to position B. Adjusting R_f or R_{in} can correct the slope, as suggested by line C. The line will rotate about the point where $I_{in} = 0$. The result is a line with the correct slope, but having an offset equal to $I_{ref1}(A_e)$. This offset term can be adjusted out in the same way as regular I_{OS}.

through its interaction with R_{in}. V_{OSI} causes a current error equal to V_{OSI}/R_{in} which is then scaled by R_f. The output voltage is $V_o = V_{OSI}(R_f/R_{in})$. To adjust V_{OSI} see Figure 10. If R_{in} is a high value (because the amplifier is in a low gain or has a current source input) the output contribution of V_{OSI} will be minimal. Even in a high gain, where V_{OSI} has a larger effect on the output, the signal/offset ratio is constant.

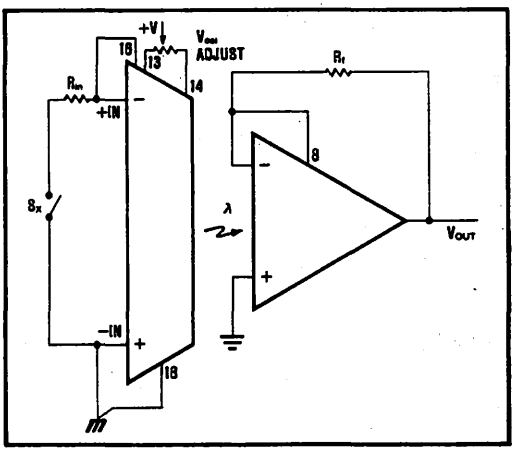


FIGURE 10. PREFERRED METHOD FOR VOLTAGE OFFSET TRIM. In those rare applications where offset voltage is significant, it is best to adjust the input offset voltage, V_{OSI}, as shown above. V_{OS} and its drift appear at the output multiplied by the factor R_f/R_{in}. V_{OSO} will usually not be gained up, and thus will not need adjustment. Adjust V_{OSI} until opening up and closing S_x causes no shift in the output voltage.

If the system offset must be adjusted from the output side of the ISO100, the output amplifier can be placed in a gain configuration. As shown in Figure 11, the output voltage offset (V_{OSO}) is now multiplied by a gain of 1 +

(R_f/R_9). If R_f = 1Meg, and R9 = 1k, the output will be 1001 times V_{OSo}. This connection does not alter the input signal gain, but it does amplify all output stage errors including V_{OSo} and noise. It is also important to realize that adjusting offset voltage in the ISO100 (and most op amps) causes a change in the offset voltage drift of about 3μV/°C for each millivolt introduced. Offset drift will be amplified by the same gain factors (as the V_{OS}) above.

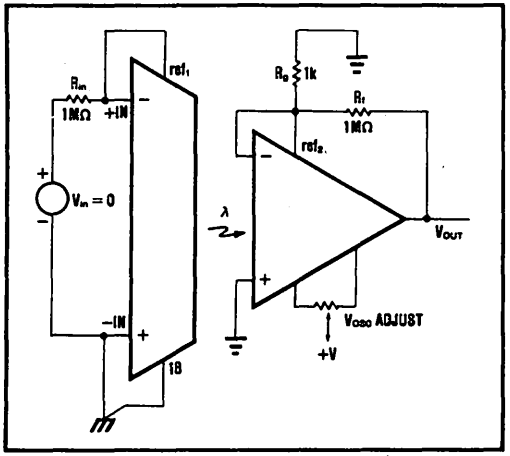


FIGURE 11. ALTERNATE METHOD FOR OFFSET VOLTAGE TRIM. If the offset voltage has to be adjusted on the output side of the isolation barrier, the output amplifier can be put in an offset multiplying gain. V_{OSo}, drift of V_{OSo}, and output stage noise appear at the output, multiplied by ($R_f/R9$) + 1. However, the signal is unaffected. Signal to noise ratio could be adversely affected.

Example 4 [Figure 12]: Using the methods described previously, the output errors of an ISO100 can be adjusted to zero. In this example, an ISO100BP is in the standard bipolar configuration with a gain of 100. Let R_f = 1Meg. From the data sheet, the maximum errors are: A_e = 2%, I_{OS} = 70nA, V_{OS} = 300μV.

I_{OS} correction uses a variation of previous techniques. The adjustment not only trims the 70nA of I_{OS}, but also the apparent I_{OS} caused by the gain error. This additional current could be as large as 250nA [$A_e(I_{ref}1)$ = .02(12μA)]. The total trim range should then be 70nA +250nA = 320nA. Because the input of the second amplifier is a virtual ground, R12 has the same voltage across it as R13. R12 is then:

$$R12 = [(R13)(I_e) \div (I_{ref} - I_e)]$$
$$= 10M\Omega(320nA) \div (10.5\mu A - 320nA)$$
$$= 316k\Omega$$

The 10.5μA is the minimum I_{ref} specification on the data sheet. Conservative design allows the R10 divider to produce twice the compensation current of the R12 divider. Therefore, R10 must be twice R12. The calculated value of R10 is 632kΩ, so a standard 1Meg pot is selected.

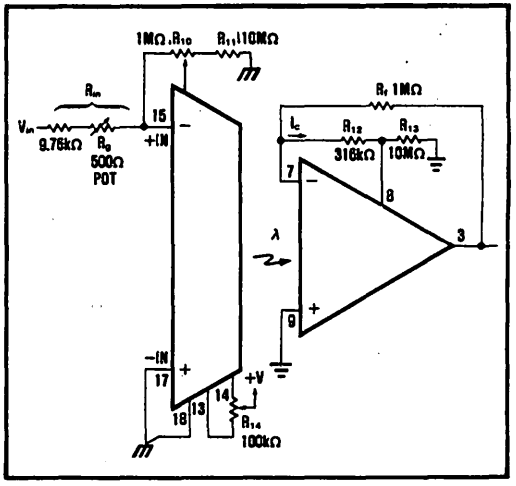


FIGURE 12. ADJUSTING THE BIPOLAR ERRORS (EXAMPLE 4). Each of the errors are adjusted in turn. With V_{in} = "open," I_{OS} is trimmed by adjusting R10 to make the output zero. R_g is then adjusted to trim the gain error. The effects of offset voltage are removed by adjusting R14.

SUMMARY OF CORRECTION TECHNIQUES [FIGURE 12]

To trim I_{OS}, disconnect the input source and let it float. This minimizes voltage offset effects. R10 is then adjusted to bring the output to zero.

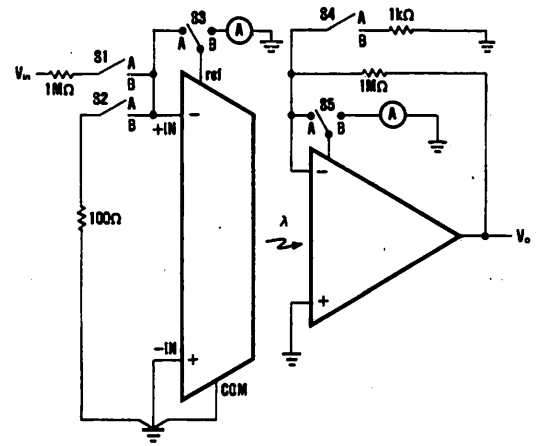
The gain error can be compensated by adjusting either R_f or R_{in}. In most circuits it will not matter which is trimemd. In this case R_{in} will be adjusted via R_g. Allowing for a 2% gain error, R_{in} should be 2% low with R_g providing a 4% trim range. This makes R_{in} = 9.8kΩ with 400Ω of trim. Using standard values, R_g would be a 500Ω pot and the fixed resistor will be 9.76kΩ. The gain is corrected by making a known change in the input voltage, and by adjusting R_g for the correct change at the output. Remember that in the bipolar mode there is an interaction between the adjustment of A_e and I_{OS}. Repeat these adjustments until the desired accuracy is obtained.

The last step is to adjust V_{OS}. Because the output stage is in a gain of one, V_{OSO} can be ignored. V_{OSI}, on the other hand, is multiplied by 101 and should be trimmed. R14 is adjusted so that there is no shift in the output when the input side of R_{in} is switched between floating and ground. Any shift is due to the offset voltage causing a current to flow in R_{in}, which is then gained up to the output.

All errors should now be minimized.

TEST CIRCUIT

A circuit is shown in Figure 13 that will allow all the major errors of the ISO100 to be measured.



TEST	SWITCHES					V_{IN}		
	S1	S2	S3	S4	S5			
A_o	B	A	A	A	A	+10V	V01 = V0	$A_o = (1 - \frac{V02 - V01}{Vin2 - Vin1})$
	B	A	A	A	A	−10V	V02 = V0	
$I_{ref1,2}$	B	A	B	A	B	−10V	$I_{ref1,2}$ = Ammeter Reading	
I_{OS} Bipolar	A	A	A	A	A	—	$I_{OS} = (V_o + R_f) - (I_{ref1} \times A_o)$	
V_{OSO}	B	A	B	B	B	+1V	$V_{OSO} = V_o/1001$	
V_{OSI}	A	A	A	A	A	—	V01 = V0	$V_{OSI} = \frac{V02 - V01}{10k}$
	A	B	A	A	A	—	V02 = V0	

FIGURE 13. STANDARD TEST CONFIGURATION. Each of the major errors in the ISO100 can be measured with the circuit shown. The test circuitry is similar in concept to the methods used in the actual production test equipment. To make measurements, the switches are placed in the positions indicated in the table, and the input voltage is set accordingly. The voltage or current reading is then used to compute the error.

DESIGN AND APPLICATION OF TRANSFORMER-COUPLED HYBRID ISOLATION AMPLIFIER MODEL 3656

Hybrid-compatible toroid assembly, in a flyback-modulated circuit, achieves long-term stability, high frequency response, and superior breakdown ratings

Whenever engineers who need or use isolation amplifiers get together and talk about the improvements they would like to see most, the big three - cost, size, and performance are likely to be mentioned. The industrial or medical equipment manufacturer often has to make a choice of either buying an isolation amplifier or building his own. Cost is the key criterion for such a decision, but there are others as well. For example, the multichannel analog system designer usually runs into printed circuit board space limitations, since he almost always requires a lot of data channels on each PC board. On the other hand, the medical equipment manufacturer is not as concerned with size but encounters very-high breakdown voltages and requires low leakage at a reasonable price.

To meet the widely varying needs of these and other potential users, Burr-Brown has made a radical departure from established design and manufacturing techniques in developing its new isolation amplifier, model 3656. Among the key design features and the resultant benefits for the user are:

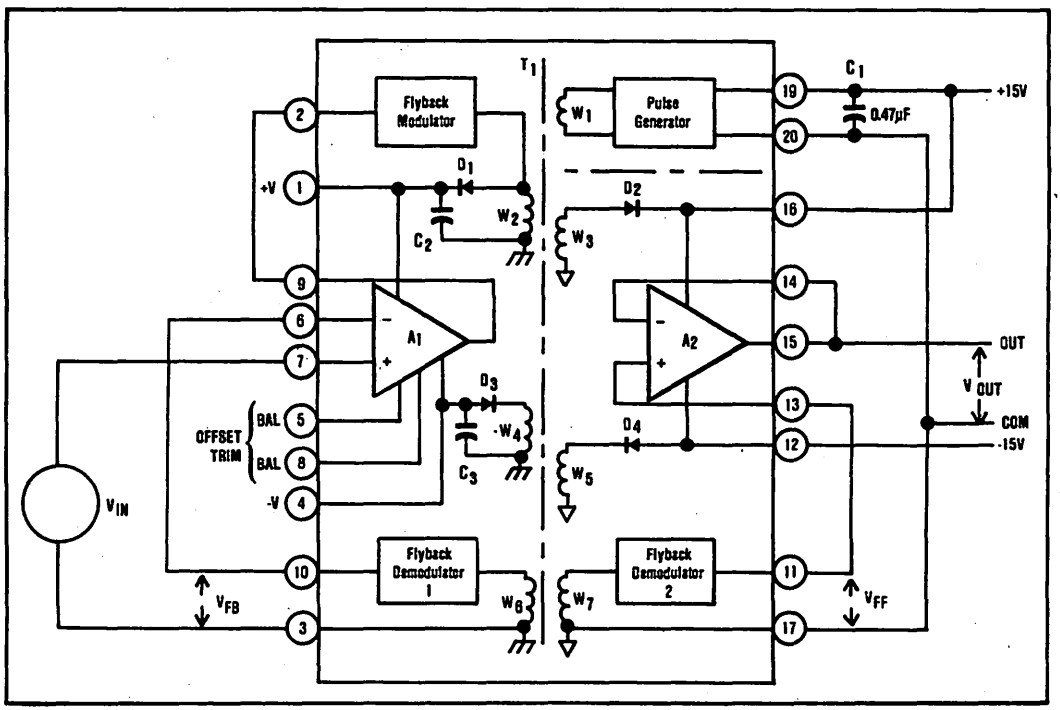


FIGURE 1. Self-contained by design. Functional diagram of hybrid isolation amplifier shows transformer T_1 at its heart and a minimum of external components. Switching rate of 750kHz results in high frequency response and eliminates external filter components.

- A single hybrid-compatible transformer (patents 4,006,974; 4,103,267; 4,082,908) in conjunction with a patented circuit, that couples both signal and power across the isolation barrier, resulting in the industry's smallest and lowest cost isolation amplifier having its own internal isolated power.
- A ceramic thick-film integrated circuit that uses the transformer to provide long-term stability and reliability at low cost.
- True three-port isolator design that achieves unprecedented voltage breakdown ratings and versatility.
- A 750kHz switching rate that results in the highest small-signal frequency response for any isolation amplifier and reduces external filtering requirements.
- A differential design concept that uses two demodulators, one for feedback and one for feedforward, producing accuracies comparable to those of higher priced transformer-coupled devices.

Figure 1 shows the functional diagram of the device in its unity-gain, noninverting configuration with a minimum of external components. A highly inductive transformer, T_1, is excited by the pulse generator containing a solid-state switch that alternately applies an open circuit and the voltage present across filter capacitor C_1 to transformer winding W_1, as illustrated in Figure 2a. When the voltage (V) is applied to the winding, the current (i) in the inductance (L) of the winding increases as shown in Figure 2b according to :

$$di/dt = V/L$$

(circuit resistances and capacitances have only secondary effects and can be ignored here). At the instant the switch opens, the voltage across the transformer reverses and reaches the magnitude necessary to maintain the current at its previous value. This effect is called flyback.

The flyback voltage (V_F) appears on all windings in the form shown in Figure 2c. Its amplitude is proportional to the instantaneous current and the equivalent resistance (R_p) shunting the transformer inductance:

$$V_F = iR_p$$

The magnitude of V_F can be varied by changing the parallel resistance across any winding of the transformer, resulting in a form of amplitude modulation. This is accomplished by the flyback modulator, which is controlled by input operational amplifier A_1. Power for A_1 is generated by rectifying the positive energizing pulse appearing across W_2. Rectification is accomplished by diode D_1, and the resultant direct current is smoothed out by C_2 to derive the positive supply voltage. Similarly, the negative supply voltage is derived by diode D_3 and capacitor C_3 from winding W_4. If the isolation amplifier is to be used as a three-port isolator, isolated power voltages for output op amp A_2 can be derived by adding filter capacitors between pins 16 and 17 and between pins 12 and 17.

At the heart of the isolation amplifier are two identical flyback demodulators. Both compare the positive-going flyback signal at the respective winding at which they are connected with the amplitude of the negative energizing pulse. At minimum modulation (load), they produce a positive output signal; as modulation increases, the demodulator output signal decreases until it is negative at maximum modulation.

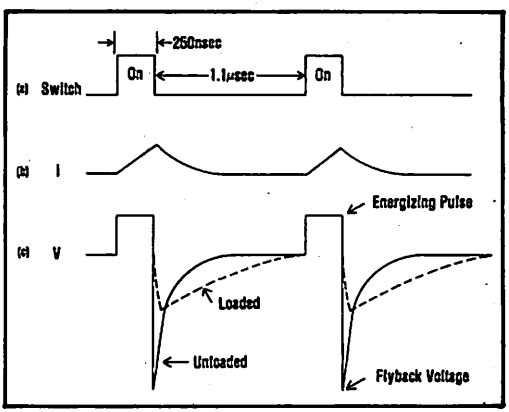


FIGURE 2. Flyback modulation. The pulsed supply voltage is applied to transformer winding (a). As a result of voltage V across winding, current I increases as in (b) until switch opens, producing flyback shown in (c). Rectified positive-going pulses provide power to energize input op amp A_1 which controls flyback modulator.

Flyback demodulator 1 is used in a closed-loop system by connecting its output to the inverting (feedback) terminal of A_1. This configuration causes A_1 to control the level of the modulator until the output of flyback demodulator 1 equals the signal at the noninverting input of A_1, so that $V_{FB} = V_{IN}$. Flyback demodulator 2, identical to flyback demodulator 1, has the same output, and thus $V_{FF} = V_{IN}$. To prevent loading of demodulator 2, it is buffered by A_2, which is configured as a unity-gain amplifier. As a result, $V_{OUT} = V_{FF} = V_{IN}$.

The accuracy of the transfer equation depends basically on the stability and tracking of the two op amps and the close matching of the demodulator components. With high grade op amps and components matched to within 0.5% or better initially, and a temperature coefficient of 25ppm/°C, a very-high gain accuracy can be achieved. Nonlinearity caused by differences in demodulator outputs is very low because of the repeatable matching of the resistors and stray capacitances made possible by thick-film hybrid-circuit technology.

HYBRIDS AND TRANSFORMERS

Until now, transformers and large chokes were to be avoided in hybrid integrated circuits. The few hybrids manufactured with such components are hard to produce and very costly because of the difficulties with size, uneven mounting surfaces, and substrate-to-magnet-wire interconnections. When Burr-Brown moved to enter the rapidly expanding market for isolation amplifiers and isolated DC/DC converters with low cost transformer-coupled hybrid circuits, it decided that these shortcomings had to be eliminated. As a result, it developed a new

approach to implementing a toroidal transformer on a hybrid substrate that eliminates the manufacturing problems.

Table I is a step-by-step comparison of the new technique with the conventional (but rarely used) approach. At present, the hybrid-compatible transformer is well suited for low-cost, low-power transformers, with the overall cost of the transformer assembly about 60% to 80% of the mounted transformer. However, it does not yet provide the same performance as the conventional transformer in all respects. Although coupling capacitance is lower and accuracy is better, the resistive losses are higher and the achievable inductance is lower.

COMPARING PAST AND PRESENT

Table II is a comparison of features and specifications of the new isolation amplifier with previously available component type units. (Note that previously available transformer-coupled isolation amps were built as printed circuits most often housed in plastic modules.) Amplitude-modulated isolation amplifiers were the first to appear, high accuracy pulse-width-modulated types were introduced in 1973, and optical ones have been available since 1976.

It can be seen that the single-transformer, flyback modulated amplifier performs well in most areas. Its nonlinearity is in line with that of all the other types and exceeds that of the low-cost amplitude-modulated types. Its isolation-voltage pulse rating is higher than that of any other amplifier and conforms with the requirements specified in medical applications for protection against defibrillator pulses.

Also, its isolation barrier capacitance is the lowest of any transformer-coupled device available today - a highly desirable feature in medical applications where the leakage from the standard 115VAC equipment power outlets to the patient must be kept at a minimum. Actually, the single transformer design keeps the leakage current below 0.5 microamperes, 20 times lower than the limit specified by Underwriters Laboratories.

Another big advantage of low barrier capacitance is that the isolation-mode rejection degradation is kept at a minimum in applications where the source impedance is high and the isolation amplifier does not have a balanced front end. The isolation-mode rejection of the new unit also compares well with that of previous designs. Another strong point of this device is its small-signal frequency response - an order of magnitude better than any other transformer-coupled isolation amp and even better than optically coupled devices.

Moreover, the 20-pin ceramic package, which measures 1.1" x 1.1" x 0.26", is the smallest of any isolation amp available today. Finally, its price is the lowest for any transformer-coupled device with an internal isolated power supply. Thus, it is more economical to use than even optically coupled devices in applications where isolated input power is not readily available.

The innovation that makes it economically feasible to put this isolation amplifier into a ceramic hybrid package is the hybrid-compatible transformer design. Figure 3, a photograph of an uncapped isolation amplifier, shows the location of the transformer, the rest of the components (the op amps, resistors, capacitors, and diodes) and

TABLE I. Comparision of Conventional and Hybrid-Compatible Transformers.

CONVENTIONAL TRANSFORMERS	HYBRID-COMPATIBLE TRANSFORMERS
To be mounted into a hybrid package,a small toroid transformer not only must be wound by hand, but all wire must be accurately placed and dressed.	Turns are completed using a manual or automatic wire bonder, cutting labor by 50% to 90%.
The mounting surface of a toroid transformer is formed by the magnet wire, causing problems of tolerance and flatness.	The flat surface of the toroid itself is used for mounting, giving a high degree of uniformity.
The magnet wire bonded to the substrate must hold the core in place and take g stress.	The core is bonded directly to the substrate, resulting in better adhesion and device integrity.
Magnet wire is hard to position accurately on small pads for soldering. The difficulty in making connections and required substrate area increases with the number of connections.	Connections are made with wire bonds. The number of connections does not affect complexity or cost.
Magnet wire must be held in place and soldered.	No soldering is required.

TABLE II. Comparison of Isolation Amplifiers.

Isolation Method	Single Transformer	Dual Transformer	Dual Transformer	Differential Optical
Package	Ceramic - IC	Plastic - Module	Plastic - Module	Ceramic - IC
Modulation	Flyback	Amplitude	Pulse-width	Light-intensity
Nonlinearity max. specified (%)	0.05 - 0.1	0.03 - 0.3	0.005 - 0.025	0.05 - 0.2
Isolation voltage pulse rating (kV)	8	up to 7.5	up to 5	5
Isolation barrier capacitance (pF)	6.0	20 - 100	16	1.8
Isolation-mode rejection (dB) at 60Hz and Gain = 10V/V	125	115 - 130	140 - 150	120
Frequency response, small signal (kHz)	35	1 - 2.5	1.5 - 2.5	15
Size (in^3)	0.33	1.4 - 10	5.6	0.44

the gold-plated pins. The toroid transformer assembly is the dominant feature in the center. It turns are made of gold rather than magnet wire, a sharp departure in construction from the state-of-the-art until now. To further illustrate the construction details of the transformer, Figure 4a gives an X-ray type view through the transformer structure from the top, and Figure 4b shows a sectional cut of the assembly.

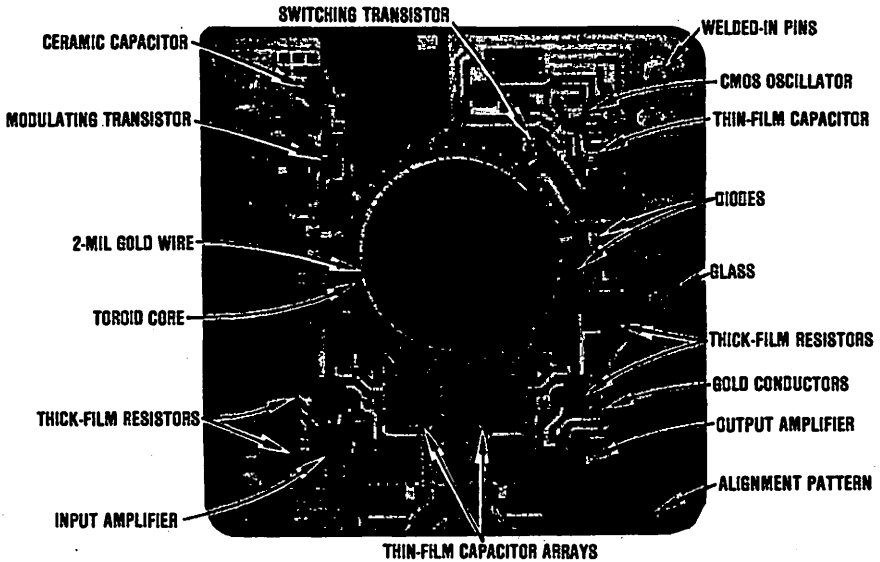


FIGURE 3. Dominant feature of this hybrid intregrated-circuit isolation amplifier is compatible transformer, which, in conjunction with the flyback-modulation technique, is used to achieve isolation of signal and power with a single transformer.

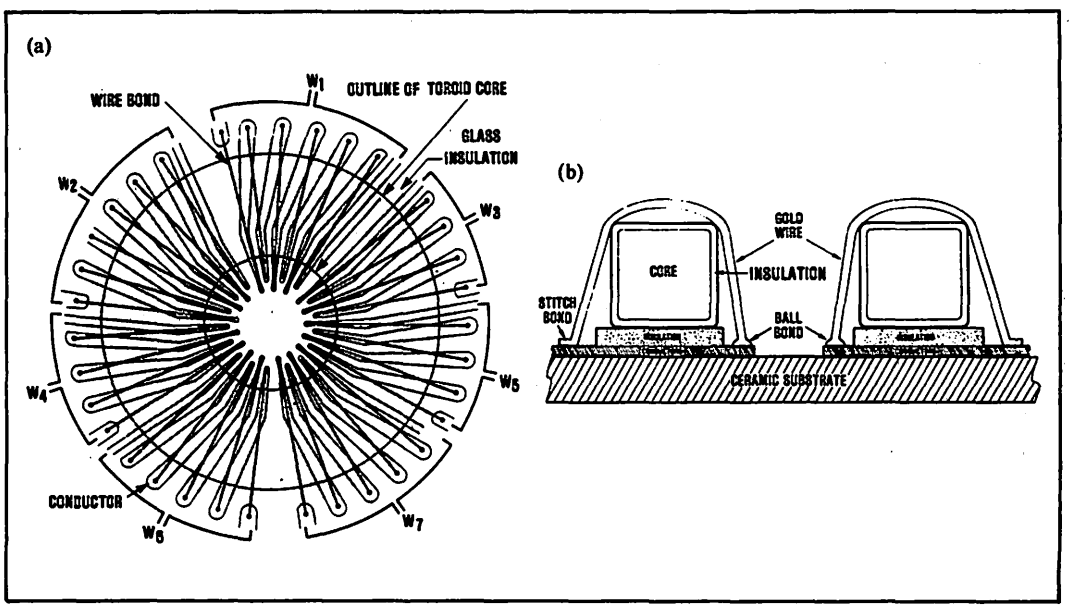


FIGURE 4. Transformer views. Top X-ray view (a) and cross section (b) show construction of toroid assembly, which provides coupling of signal and power across amplifier's isolation barrier. Turns are of gold wire instead of usual magnet wire and are bonded to screened gold interconnection pattern on ceramic substrate.

MANUFACTURE

Manufacture of the isolation amplifier begins by screening gold conductors onto the ceramic substrate to provide circuit interconnection patterns and the transformer conductor patterns shown in Figure 4a. The gold conductor is then fired in accordance with Burr-Brown's standard thick-film process. The layer of glass insulation is also screened on and fired using thick-film technology. Further processing completes the substrate, which contains 20 laser-trimmed cermet resistors and 19 gold-plated pins, swaged and welded in place.

The first step on the assembly line is the bonding of the insulation-coated toroid to the glass insulation layer. All the other circuit components are then bonded to the substrates. Chip-to-conductor interconnectors are made with 1-mil gold wire and transformer turns are completed with 2-mil gold wire in accordance with the pattern shown in Figure 4a.

Next, the unit is actively laser-trimmed, tested, and insulation-coated with a high dielectric constant insulating material.

The integrity of the transformer under high voltage stress is ensured by the use of several insulation steps. The glass layer on top of the conductors and the insulator coating on the toroid core each have a minimum dielectric strength of 8kV.

Finally, the package is sealed by applying a ceramic cap over the top of the unit under pressure and heat in a nitrogen atmosphere. The heat cures an epoxy ring prescreened onto the ceramic cap to form an airtight seal.

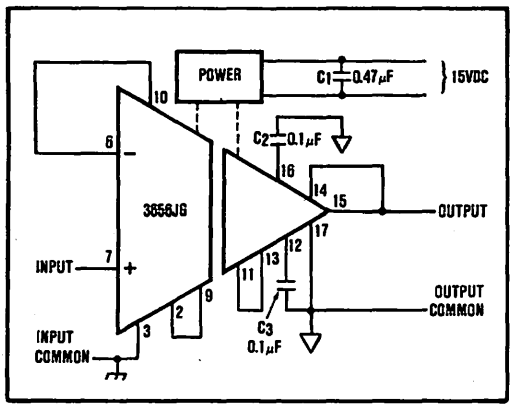


FIGURE 5. Three-port. The 3656, shown here in unity-gain configuration, has a dynamic input and output range of 5V with internally generated power. With external dual-polarity supply, capacitors C_2 and C_3 can be eliminated.

APPLICATIONS

In the two-port unity-gain isolator of Figure 1, only one external filter capacitor (C_1) and a ±8V to ±15V supply are required. With a standard ±15V supply and at unity gain, this circuit provides a dynamic input and output voltage range of ±5V. With two additional resistors, A_2 can be programmed for a noninverting gain of 2, providing a minimum dynamic output voltage range of ±10V.

Figure 5 shows the 3656 connected as a unity-gain, three-port isolator. All isolated supplies are internally generated. C_2 and C_3 filter the internal supplies for output-buffer op amp A_2. If a dual-polarity supply is available at the output port, these capacitors can be eliminated. With the internal supplies as configured, the dynamic input and output voltate range is ±5V.

As a result of increased public awareness and increasing government involvement in patient safety, isolation amplifiers have become a must for most electrical patient-monitoring devices marketed today. The 3656 is well suited to such applications because of its low noise, low isolation capacitance, and a high isolation breakdown.

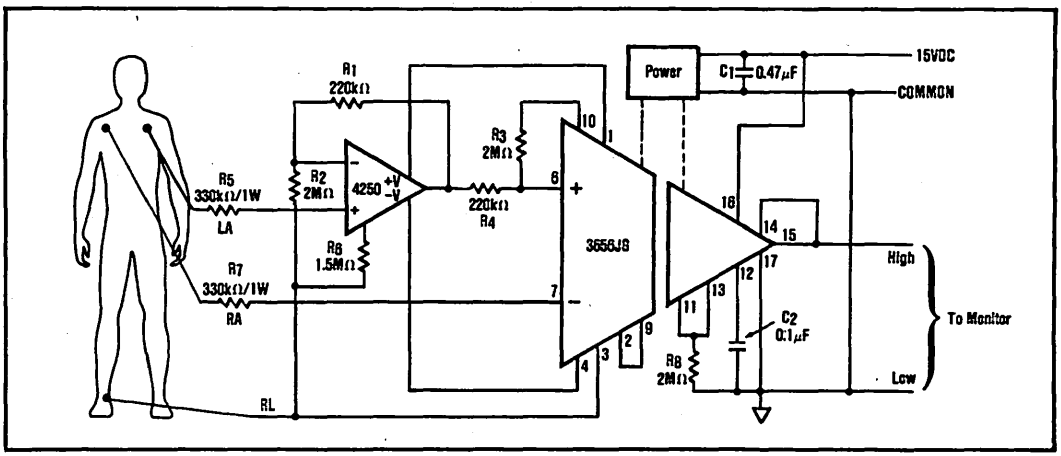


FIGURE 6. Medical beat. Because of its high isolation, the 3656 is ideal as an electrocardiograph amplifier. It can withstand inadvertent applications of defibrillation pulses while the patient is being monitored. Heart pulses are accurately amplified with a frequency response of DC to 3kHz.

The electrocardiograph amplifier in Figure 6 is implemented with an instrumentation input stage by using a second low power, low noise op amp (such as industry type 4250) in addition to the internal device. Resistors R_3 and R_4 set the noninverting gain of the internal op amp to 10 and resistors R_1 and R_2 provide matching of the external op amp inputs in accordance with standard practice for designing instrumentation amplifiers.

Resistors R_5 and R_7 protect against the peaks of defibrillation pulses, which might be inadvertently applied to the input if a defibrillator is used to restore the patient's heart function while he is being monitored. These resistors must be carbon composition types, because film types of the same rating cannot survive defibrillator impulse energy, which can range up to 2 watts/second (8kv).

Resistor R_6 sets the quiescent current of A_1, and R_8 equalizes the load of the output demodulator with that of the input demodulator for maximum gain accuracy. Capacitor C_2 filters the internal negative supply for the output buffer op amp, but if a ±15V supply is connected to the output buffer op amp, C_2 can be eliminated.

This circuit accurately amplifies heart pulses with a frequency response of DC to 3kHz. A bandpass filter between amplifier and monitor can select out the desired frequency range.

For electroencephalography, or brain wave monitoring, where defibrillator protection is not required, R_5 and R_7 can be eliminated, resulting in lower noise. But in order for the frequency band to be monitored, the gain must be increased, since brain waves are an order of magnitude smaller in amplitude than heart pulses. Increasing the gain is accomplished by bypassing both R_1 and R_4 with an appropriate RC series network. For example, to monitor alpha and theta waves (4Hz to 13Hz) with a gain of 200, two 10kΩ resistors and two 10μF capacitors should be used.

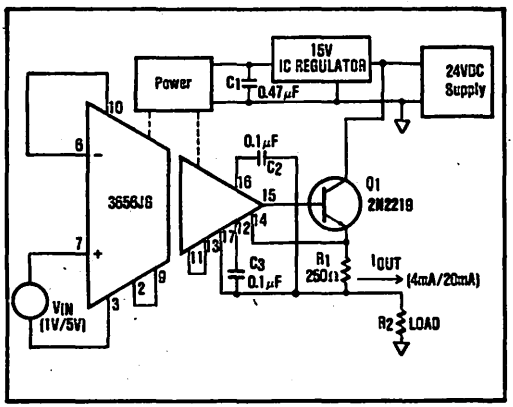


FIGURE 7. Industrial control. Current-mode signal transmission, often used in industrial control loops, is conveniently implemented with the 3656, here used as a three-port isolator to control current-source transistor Q_1. Circuit converts 1V or 5V input into a 4mA or 20mA signal.

INDUSTRIAL CONTROL LOOPS

Analog signal transmission for industrial control circuits is typically done with 4mA to 20mA loops, where 4mA represents zero or quiescent level and 20mA represents maximum signal. Current-mode signal transmission eliminates inaccuracies that are caused by attenuation in cables, intrinsic safety barriers, and multiple sensors. The shifted zero inherent in the 4mA to 20mA range also makes it easy to recognize abnormal operating conditions such as power-

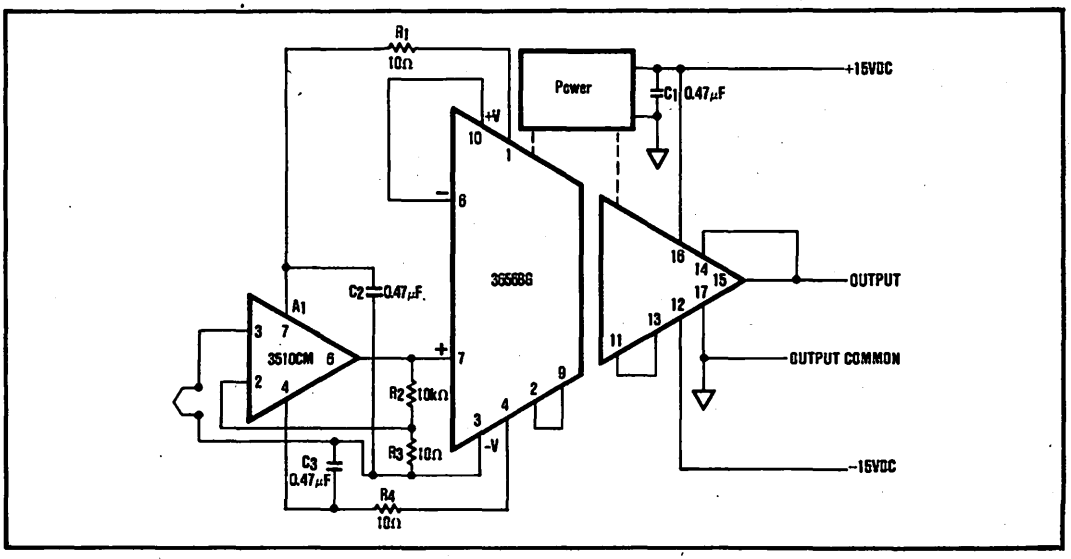


FIGURE 8. Stability. For applications like this thermocouple, where DC stability is important, the isolation amplifier can be supplemented with a high-performance op amp, using the internal isolated power supply, for which capacitors C_2 and C_3 provide additional filtering.

down or open circuits. If the transmitted current is not between 4mA and 20mA, an error condition is generally assumed.

Figure 7 shows an isolated 1V..5V to 4mA..20mA converter. All power is derived from a single 24VDC supply. The voltage for the isolation amplifier is regulated to 15V using a standard three-terminal regulator. The isolation amplifier is used with a floating output (three ports) to control current-source transistor Q_1 and feed its emitter current into grounded load resistor R_2. The feedback voltage for the internal output buffer is derived across sense resistor R_1 and is proportional to the output current.

For increased DC stability when required in applications like a thermocouple amplifier, the front end of the 3656 can be supplemented with a high performance op amp by using the available isolated supply. Figure 8 shows such a configuration. Resistors R_2 and R_3 set the gain of the front end amplifier to 1000. Capacitors C_2 and C_3 provide additional filtering for the isolated supply - recommended if A_1 draws more than 0.1mA of supply current.

GETTING FULL ISOLATION-MODE REJECTION

A recent analysis of an isolation amplifier to determine the effect of internal- and external-component and stray capacitances on isolation-mode rejection shows that only the capacitances of the input wires to the output circuits are critical. Thus, the major factors for the user are specified isolation-barrier capacitance (C_{ISO}) and the external capacitance between any of the input and output pins.

Designing for high isolation-mode rejection becomes very simple if the isolation amp includes an instrumentation or balanced front end or one is added externally. The balanced front end makes it easy to maintain the full isolation-mode rejection specified because the barrier capacitances from each input-to-output common can be easily balanced. To maintain an isolation-mode rejection close to 120 decibels with a capacitance unbalance of 0.5pF, a source impedance unbalance of up to 50kΩ can be tolerated.

Maintaining full isolation-mode rejection with a single-ended or unbalanced front end is more difficult. The source resistances in this case must be no more than a few hundred ohms. With large source impedances, degradation can occur in degrees that depend on the circuit, the isolation capacitance, and external stray capacitances.

A simple model of an isolation amplifier with an operational amplifier input stage is shown in Figure 9. Amplifier A_1 represents the input op amp, and A_2 the unity-gain isolation stage. Specified isolation-mode rejection is achieved if common-mode signal V_{CM} produces no differential input signal between the inputs of A_1, A_2, or both. This is the case if both R_2, R_4, and R_5 and C_1, C_2, and C_{ISO} are zero. However, when these resistors and capacitors have finite values, they form three low-pass filters, each with the general attenuation function:

$$A = [R + (1/j\omega C)]j\omega C$$

For example, if R_5= 1kΩ and C_{ISO}= 6pF, the calculated attenuation A at 60Hz is 2.2×10^{-6}, or 2.2ppm. Though a few ppm of attenuation seems trivial, note that 1ppm is equivalent to 120dB (20 log 1ppm).

Any differential signal appearing at the input of A_1 because of unequal attenuation of V_{CM} by network C_1-R_2 loaded with R_5 on the one hand and C_2- R_4 loaded with the noninverting input of A_1 on the other will be amplified the same as an input signal (V_{IN}). Thus, unequal attenuation can be directly translated into a limit on isolation-mode rejection referred to the input. Any attenuation of V_{CM} caused by low-pass filter R_5-C_{ISO} with respect to the common portion of V_{CM} across the input of A_1 appears across the input of A_2. The gain for this signal is only unity regardless of gain of A_1, causing an isolation-mode rejection degradation with reference to the output.

The three-wire input system in the figure maximizes the isolation-mode rejection of the 3656 or other isolation amplifiers with an unbalanced input, because C_{ISO} becomes less critical with high gain and C_1 and C_2 can be kept small. But the value of R_2 affects the circuit gain.

If a two-wire system is chosen and the input common is connected to the junction of R_2 and R_3 (S_1 switched), the gain is no longer affected by R_2, but the degradation of balance caused by network C_1- R_2 loaded by R_3 in conjunction with the largest capacitance C_{ISO} is amplified by A_1 and causes much poorer isolation-mode rejection at gains higher than unity.

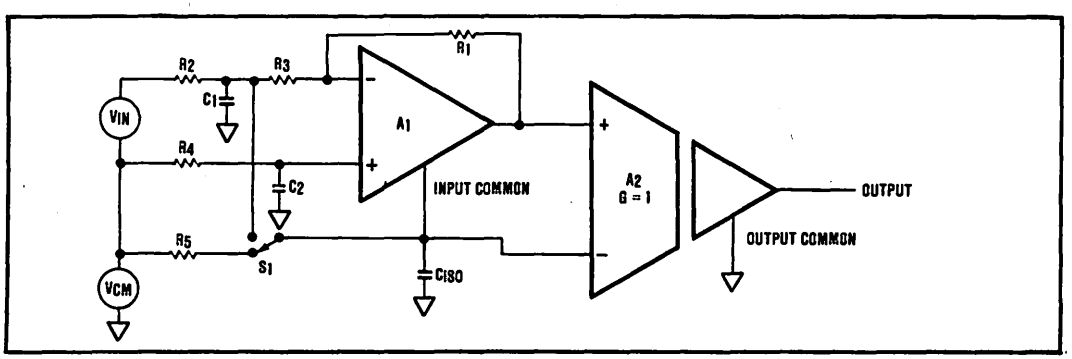


FIGURE 9. Isolation Amplifier Model For Analyzing Isolation-Mode Rejection.

WHAT IS AN ISOLATION AMPLIFIER?

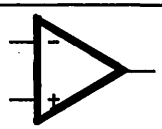
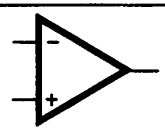
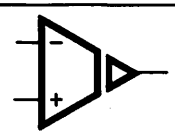
Isolation amplifiers resemble operational amplifiers but are designed to have a galvanic discontinuity between their input and output pins. This discontinuity, called an isolation barrier, must have high breakdown voltage, low DC leakage (high barrier resistance), and low AC leakage (low barrier capacitance).

The isolation barrier sets the isolation amplifier apart from operational and instrumentation amplifiers in cost and complexity, as well as in application. So called three-port isolation amplifiers have an additional isolation barrier between the power supply connection and the signal connections. This feature increases versatility because it allows the user to connect power in common with either the amplifier's input or its output. In some cases, it may be advantageous to isolate the power supply from the input or the output and thereby eliminate additional error sources that may be present in a system.

Isolation amplifiers generally serve the following functions not achievable with operational or instrumentation amplifiers:

- Sensing small signals in the presence of very-high (> 10 volts) or unknown common-mode voltages.
- Protecting patients undergoing medical monitoring or diagnostic measurements.
- Completely breaking ground loops.

Below is a comparison of the three basic amplifier types. The isolation amplifier, as well as offering isolation, increases accuracy because of its floating input. In contrast to the instrumentation amplifier, it not only eliminates ground loop errors but further reduces the total system error because its isolation-mode rejection ratio is generally one or two orders of magnitude higher than the common-mode rejection of an instrumentation amplifier.

	OP AMP	INSTRUMENTATION AMP	ISOLATION AMP
SYMBOL			
FEEDBACK CONFIGURATION	User defined feedback such as voltage, current dV/dt: $\int$ Vdt. log V, etc.	Committed feedback. Gain adjustable within fixed limits.	
BASIC APPLICATION	1. General purpose gain element. 2. Buffer. 3. Analog computer.	High accuracy analog sense amplifier when common-mode potentials are smaller than the supply voltage.	1. High accuracy analog sense amplifier for common-mode potentials in excess of supply voltage. 2. Analog safety isolator. 3. Break ground loops.
MAJOR ERRORS	Offset, noise and common-mode errors independent of gain.	Input and output offset and noise. Total error depends on gain. One set of common-mode specifications.	Input and output offset and noise. Separate common-mode and isolation mode errors except for single-ended input devices.

COMBINE TWO OP AMPS TO AVOID THE SPEED ACCURACY COMPROMISE

By interconnecting a low drift op amp and a wideband op amp, the best characteristics of both amplifiers are attained in the composite amplifier. Typically, wideband op amps have high voltage offset drift with time and temperature, which can produce significant error. Shown in Figures 1 and 2 are two composite op amps. Each uses a low drift op amp, A_1, and a wideband op amp, A_2, in configurations which yield the best performance characteristics of each amplifier: the wide bandwidth of A_2 and the low offset voltage drift of A_1. Added benefits include increased open-loop gain and reduced low frequency noise. The low drift op amp provides continuous correction for the input offset voltage of the fast amplifier. For the inverting-only composite amplifier shown in Figure 1, the low drift op amp A_1 senses the offset voltage from ground present at the summing junction of the wideband amplifier. Any such offset will be integrated by A_1 to develop an offset compensating voltage at the non-inverting input of the fast op amp. Integration continues until the summing junction voltage is equal to the input offset voltage of the low drift amplifier (including the effects of the low drift amplifier's input bias currents on resistors R_1 and R_2). Then the offset voltage of the composite amplifier is essentially that of the low drift op amp.

For the differential input composite amplifier shown in Figure 2, the low drift op amp amplifies the offset voltage at the inputs of the wideband op amp and supplies an offset correction to the offset nulling pin of the fast amplifier (pin 8 for the wideband amplifier shown). The output of the low drift amplifier stabilizes at the voltage necessary to reduce the offset voltage of the fast amplifier to that of the low drift op amp plus the offset from the bias current in resistors R_1 and R_2. Again, the offset voltage of the composite amplifier is reduced to that of the low drift op amp.

The open-loop gain of both composite amplifiers is $A_2 \times (1 + \alpha A_1)$, where α is defined as E_X/A_1E_i. For the inverting-only composite op amp shown in Figure 1, αA_1 is the response of the integrator formed by A_1, R_1 and C_1. For the differential input composite op amp shown in Figure 2, α is essentially a constant, independent of frequency, and is the change in the offset voltage of A_2 due to a change in E_X divided by the change in E_X. It can be shown that for the composite op amps to have a single pole in their open-loop gain response, R_1C_1 must equal $A_{O2}/2\pi f_{c2}$ in the inverting-only composite op amp and α must equal $-f_{c2}/A_{O2}f_{c1}$ in the differential input composite op amp, where f_{c1}, f_{c2}, and A_{O2} are the unit

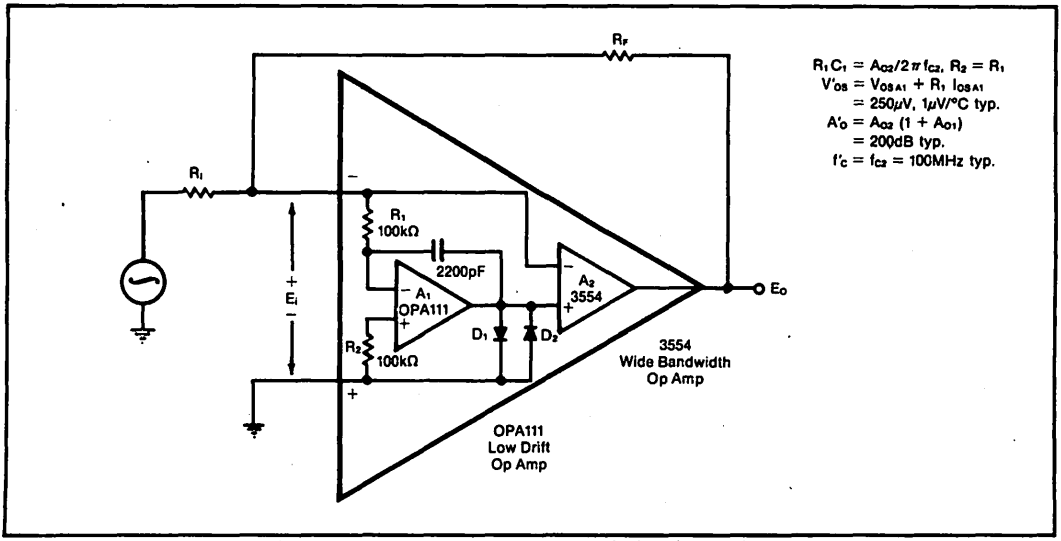


FIGURE 1. Composite op amp for inverting amplifier configurations where the non-inverting input is at signal ground.

gain bandwidths of amplifiers A_1 and A_2, and the DC open-loop gain of A_2, respectively.

In addition to a decreased offset voltage drift and an increased open-loop gain, the differential input composite op amp has the further advantage of improved common-mode rejection at low frequencies. At low frequencies the CMR of the wideband amplifier is essentially replaced by that of the low drift amplifier, which is typically much better than the wideband amplifier.

Diodes D_1 and D_2 at the output of the low drift amplifier in Figure 1 prevent a latch-up condition which can exist in the composite amplifier, since the output saturation voltage of the low drift amplifier specified exceeds the common mode range of the wideband amplifier shown. Low-pass filters R_1/C_1 and R_2/C_2 at the inputs of the low drift op amp in Figure 2 prevent high frequency common mode swing from unbalancing the input stage of the low drift amplifier, which would cause a change in its input offset voltage.

The composite amplifier has some idiosyncrasies which may be important in certain applications. It will not completely stabilize in response to a step input until the low-drift op amp and its integrator loop have settled to a final value. This can produce a settling "tail". Since the DC correction loop has a small effect on the output, the magnitude of this aberration may be small or negligible. Actual applications should be evaluated to determine the significance of this effect.

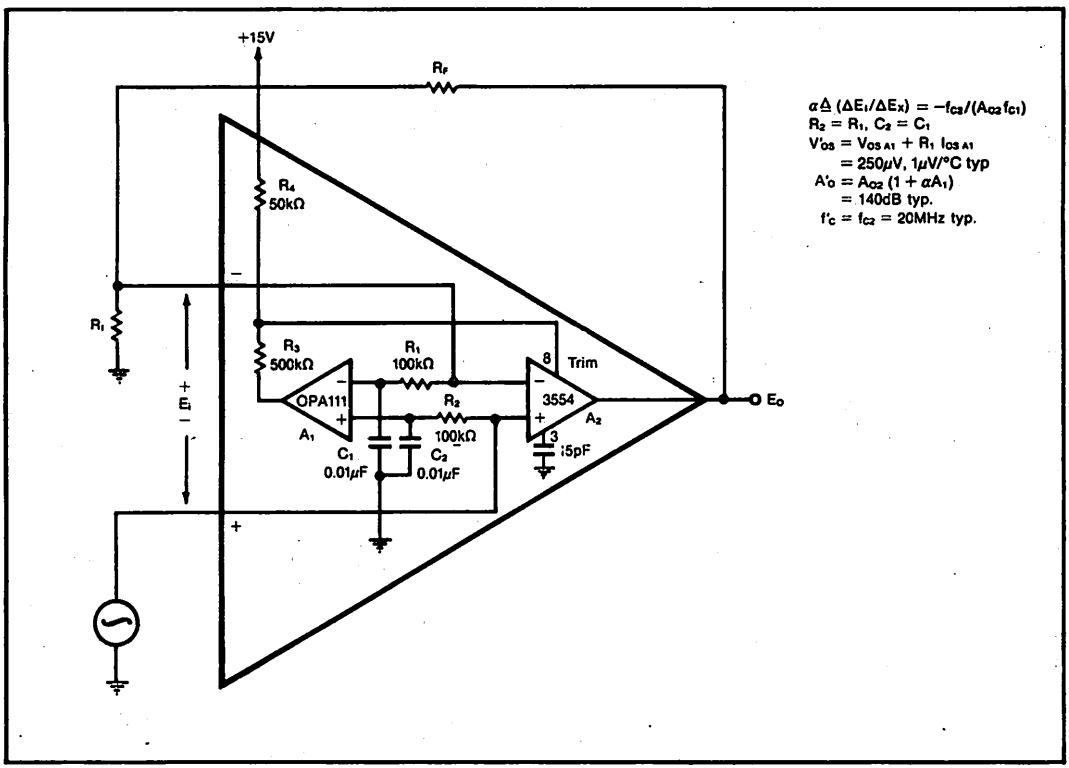


FIGURE 2. Differential Composite Op Amp. This version may be used in applications where neither the inverting or non-inverting input are at signal ground.

DESIGNING PHOTODIODE AMPLIFIER CIRCUITS WITH OPA128

The new OPA128 ultra-low bias current operational amplifier achieves its 75fA maximum bias current without compromise. Until now, serious performance trade-offs were required which sacrificed overall amplifier performance in order to reach femtoamp (fA = 10^{-15}A) bias currents. It is the world's first **monolithic** sub-picoamp op amp.

UNIQUE DESIGN MINIMIZES PERFORMANCE TRADE-OFFS

Small-geometry FETs have low bias current, of course, but FET size reduction reduces transconductance and increases noise dramatically, placing a serious restriction on performance when low bias current is achieved simply by making input FETs extremely small. Unfortunately, larger geometries suffer from high gate-to-substrate isolation diode leakage (which is the major contribution to BIFET® amplifier input bias current).

Replacing the reverse-biased gate-to-substrate isolation diode structure of BIFETs with dielectric isolation removes this large leakage current component which, together with a noise-free cascode circuit, special FET geometry, and advanced wafer processing, allows far higher ***Difet***® performance compared to BIFETs.

HOW TO IMPROVE PHOTODIODE AMPLIFIER PERFORMANCE

An important electro-optical application of FET op amps is for photodiode amplifiers. The unequalled performance of the OPA128 is well-suited for very high sensitivity detector designs. A few design tips for photodiode amplifiers may be helpful:

1. **Photodiode capacitance should be as low as possible.** See Figure 1: C_J affects not only bandwidth but noise as well. This is because C_J and the op amp's feedback resistor form a noise-gain zero (feedback pole).

2. **Photodiode active area should be as small as possible so that C_J is small and R_J is high.** This will allow a higher signal-to-noise ratio. If a large area is needed, consider using optical "gain" (lens, mirror, etc.) rather than a large area diode. Optical "gain" is essentially noise-free.

3. **Use as large a feedback resistor as possible (consistent with bandwidth requirements) to minimize noise.** This seems paradoxical, but remember, resistor thermal noise increases as:

$$e_{OUT} = \sqrt{4\,k\,T\,B\,R}$$

k: Boltzman's constant = 1.38×10^{-23} J/K
T: temperature (°K)
B: noise bandwidth (Hz)
R: feedback resistor (Ω)
e_{OUT}: noise voltage (Vrms)

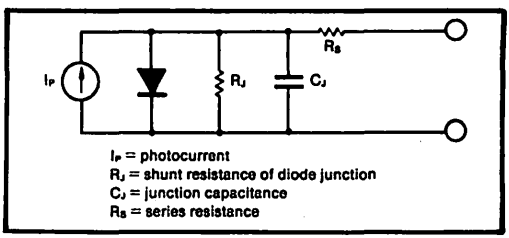


FIGURE 1. Photodiode Equivalent Circuit.

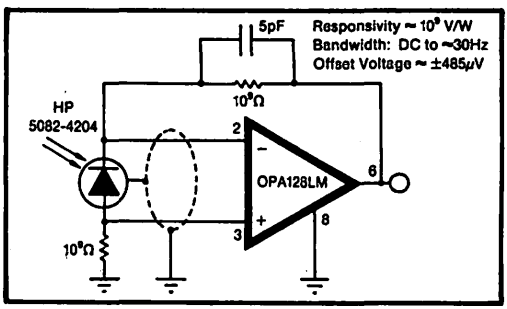


FIGURE 2. High-Sensitivity Photodiode Amplifier.

while transimpedance gain (signal) increases as:

$$e_{OUT} = i\,(signal)\,R$$

Signal-to-noise improves by $\sqrt{R}$.

4. **A low bias current op amp is needed to achieve highest sensitivity.** Bias current causes voltage offset errors with large-feedback resistors. Wide bandwidth circuits with smaller feedback resistors are less subject to bias current errors, but even in these circuits, bias current must be considered if wide temperature range operation is expected. The OPA128LM specs only ±2pA max at +70°C. Bias current also causes shot noise.

$$i_S = \sqrt{2\,q\,i}$$

q: 1.602×10^{19} coulombs
i: bias (or signal) current (A)
i_S: noise current (A rms)

In most circuits, the dominant noise source will be the thermal (Johnson) noise of the feedback resistor.

5. **Diode shunt resistance (R_J) should be as high as possible.** If $R_J \gg R_F$, then the circuit DC gain (noise gain) is 1V/V. Low resistance diodes will cause noise, voltage offset, and drift to be amplified by $1 + R_F/R_J$.

Since diode shunt resistance decreases at higher temperature, it can cause unexpected errors. In Figure 3 a diffused-junction GaAsP photodiode is used to maintain R_J = 3000MΩ at +60°C. Due to its higher bandgap, GaAsP has a flatter R_J versus temperature slope than silicon.

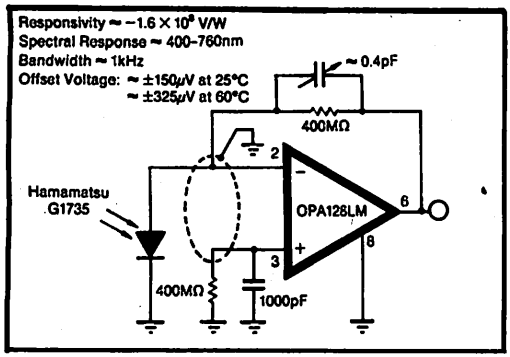


FIGURE 3. Wide-Temperature-Range Photodiode Amplifier.

6. **For highest sensitivity use the photodiode in a "photovoltaic mode".** With zero-bias operation, dark current offset errors are not generated by this (photodiode leakage) current. Zero bias is a slower but higher sensitivity mode of operation. Most photodiodes work quite effectively with zero bias, even those originally designed for reverse-biased operation.

7. **Fastest response and greatest bandwidth are obtained in the "photoconductive mode".** Reverse bias reduces C_J substantially and also reduces or eliminates the slow rise time diffusion "tail" which is troublesome at longer wavelengths. Disadvantages of biased operation are: dark current, 1/F noise component is introduced, and the occasional need for an extra bias supply.

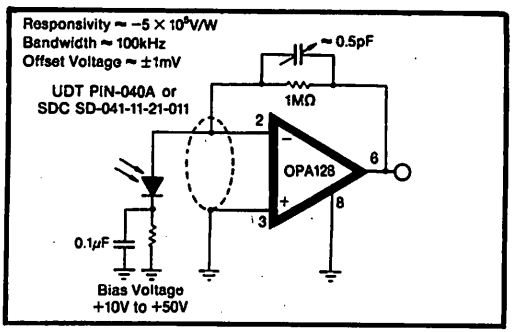


FIGURE 4. Wider-Bandwidth Photodiode Amplifier.

8. **A very high resistance feedback resistor is MUCH better than a low resistance in a T network.** See Figure 5. Although transimpedance gain (e_{OUT}/i_{SIGNAL}) is equivalent, the T network will sacrifice performance. The low feedback resistance will generate higher current noise (i_n) and the voltage divider formed by R_1/R_2

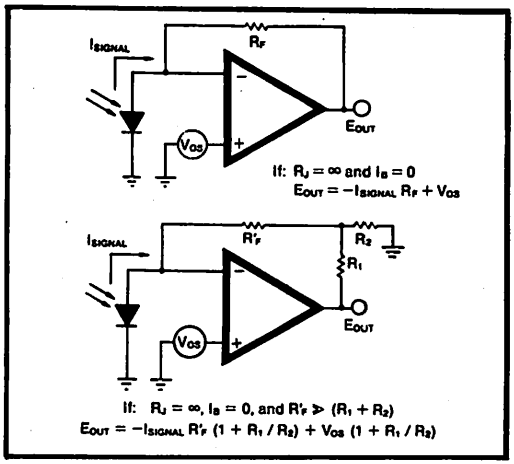


FIGURE 5. Feedback Resistors for Transimpedance Amplifiers.

multiply input offset voltage, drift, and amplifier voltage noise by the ratio of $1 + R_1/R_2$. In most electrometer amplifiers, these input specifications are not very good to start with. Multiplying an already high offset and drift (sometimes as high as 3mV and 50μV/°C) by use of a T network becomes impractical. By using a far better amplifier such as the OPA128, moderate T network ratios can be accommodated and the resulting multiplied errors will be far smaller. Although a single very-high resistance will give better performance, the T network can overcome such problems as gain adjustment and difficulty in finding a large value resistor. A few companies specializing in very-high value resistors are: Victoreen (use their low-capacitance models), Eltec and Cal-R.

9. **Shield the photodetector circuit in a metal housing.** It is a very high impedance, high sensitivity circuit and it requires good shielding and effective power supply bypassing. This is not optional.

10. **A small capacitor across R_F is frequently required to suppress oscillation or gain peaking.** Although it can affect bandwidth, a small amount of capacitance will usually be required to ensure loop stability. This capacitor can be made larger for bandwidth limitation if desired.

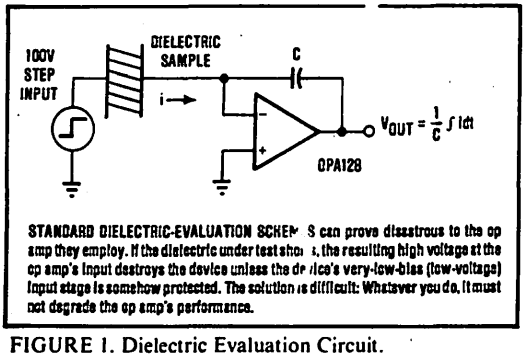
KEY OPA128 SPECIFICATIONS

Bias current	75fA max
Offset voltage	500μV max
Drift	5μV/°C max
Noise	15nV/√Hz at 10kHz

BIFET® National Semiconductor Corp.; *Difet*® Burr-Brown Corp.

DIODE-CONNECTED FET PROTECTS OP AMPS

Providing input-overload protection for sensitive measurement circuits proves difficult when you must not degrade the circuits' performance in the process. It's an especially tricky problem when you're measuring a material's dielectric properties. In such an application (see Figure 1), an ultralow-input-bias-current op amp serves as a current integrator to measure a dielectric's response to a 100V step.



STANDARD DIELECTRIC-EVALUATION SCHEMES can prove disastrous to the op amp they employ. If the dielectric under test shorts, the resulting high voltage at the op amp's input destroys the device unless the device's very-low-bias (low-voltage) input stage is somehow protected. The solution is difficult: Whatever you do, it must not degrade the op amp's performance.

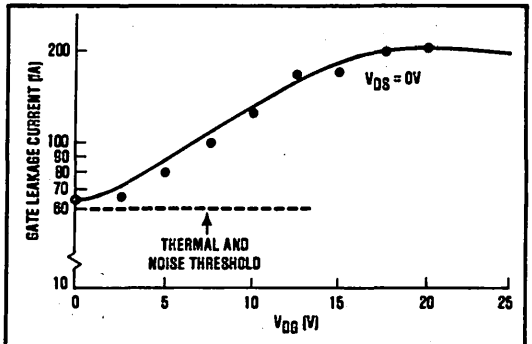
FIGURE 1. Dielectric Evaluation Circuit.

Unfortunately, the op amp is destroyed if the dielectric sample shorts.

For one such measurements setup, the OPA128 serves because its bias current is less than 75fA (75×10^{-15}A) and therefore contributes negligible measurement error. What type of protective device doesn't degrade this op amp's parameters? PN-junction devices usually have leakage currents in the nanoamp range even at very-low bias voltages—a degradation of several orders of magnitude. FETs are generally much better in this respect, and Siliconix's 2N4117A JFET proves the best.

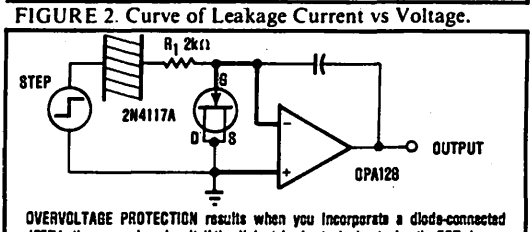
Figure 2 shows an experimentally derived curve of leakage current vs voltage for this device. Note that for voltages comparable to those between an op amp's inputs, the 2N4117A's leakage is compatible with the op amp's bias. (The residual 60fA level at 0V arises from thermal effects and measurement-system noise.)

The overload-protected design resulting from these FET measurements is shown in Figure 3. The diode-connected JFET serves as a shunt across the op amp's input - a scheme that limits the differential input to 0.6V if the dielectric shorts. Resistor R_1 limits the maximum short-circuit current to the 50mA level specified in the FET's data sheet. R_1's effect on measurement accuracy is negligible because the dielectric's impedance is very much greater than the resistor's 2kΩ value.



JFET LEAKAGE CURRENTS can be so low that they don't degrade a low-input bias op amp's parameters. Measurements show that Siliconix's 2N4117A can serve as a voltage limiter when it's diode-connected. The actual leakage is probably somewhat lower than measured, but thermal effects and noise place a limiting threshold on the measurement.

FIGURE 2. Curve of Leakage Current vs Voltage.



OVERVOLTAGE PROTECTION results when you incorporate a diode-connected JFET in the measuring circuit. If the dielectric shorts during testing the FET clamps at 0.6V, saving the sensitive op amp from destruction. R_1's resistance - although high enough to protect the FET against overcurrent failure - is still so small relative to the dielectric's impedance that it doesn't impair measurement accuracy.

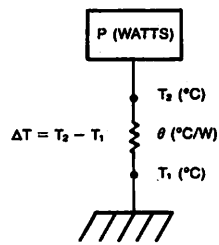
FIGURE 3. Overvoltage Protection Circuit.

HOW TO DETERMINE WHAT HEAT SINK TO USE

A heat sink is normally required when using high power or high voltage amplifiers. The heat sink required depends on the specific application details. Evaluation of heat sink requirements is easy and can lead to cost savings or increased reliability.

A simple thermal model for a power amplifier utilizes an analog to an electric circuit. The "Ohm's law" of this thermal model states that the temperature rise across a thermal resistance is equal to that thermal resistance times the power dissipated:

$$\Delta T = \theta P$$



where: ΔT is the temperature rise
θ is the thermal resistance in °C/W
P is the amplifier's power dissipation in watts.

The power dissipated in the power amplifier depends on the supply voltage, electrical load, and signal conditions. For resistive loads and DC (or slowly varying signals) the maximum dissipation is:

$$P_{MAX} = \frac{V_S^2}{4R_{LOAD}}$$

where: V_S is the supply voltage referred to load ground (one side, not the sum of $+V_S$ and $-V_S$)
R_{LOAD} is the load resistance.

For AC signals or reactive loads the power dissipated is not the same as the power delivered to the load. Refer to Applications Note AN-123 for details on evaluating amplifier dissipation.

The allowable temperature rise is dependent on the ambient temperature conditions and the maximum allowable junction temperature, $T_{J\ MAX}$. This is the maximum semiconductor junction temperature of the internal power transistors as specified by the power amp manufacturer. It normally ranges from 150°C to 200°C. The maximum junction temperature should be considered an absolute maximum. It should be recognized that, as with any electronic component, improved reliability can be achieved by choosing a more conservative operating point.

The ΔT is simply the difference between the maximum ambient temperature ($T_{A\ MAX}$) and the maximum junction temperature (or a somewhat derated $T_{J\ MAX}$).

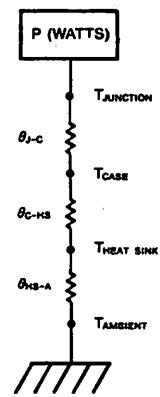
Once the power dissipation and temperature rise are determined, the thermal resistance, θ, can be calculated:

$$\theta_{J\text{-}A} = \frac{\Delta T}{P}$$

e.g.: $T_{J\ MAX}$ = 200°C (from power amp specification)
Choose a $T_{J\ MAX}$ of 180°C for reliability margin.
T_A = 60°C (maximum ambient operating temperature)
P = 25W (depends on $\pm V_S$, load etc.)
$\theta_{J\text{-}A} = (180 - 60) \div 25 = 4.8$°C/W (this is not the required heat sink θ).

$\theta_{J\text{-}A}$ is the total thermal resistance from junction to ambient and is comprised of three major parts:

1. The thermal resistance from junction to case, $\theta_{J\text{-}C}$, is specified by the power amp manufacturer. Note that some power amps specify a lower thermal resistance for AC signal conditions where the dissipation is shared by both internal power transistors.



2. The thermal resistance from the power amp case to the heat sink, $\theta_{C\text{-}HS}$, depends on heat sink mounting surface flatness. Heat sink compound reduces $\theta_{C\text{-}HS}$ in the presence of small surface imperfections. While it is not a substitute for good heat sink workmanship, it does conduct heat better than the air that would otherwise fill the voids resulting from surface irregulari-

ties. Typical values for a TO-3 type package range from 0.1°C/W to 0.5°C/W. Power amps or transistors with electrically hot cases usually require insulating hardware which adds as much as 1.0°C/W to $\theta_{C\text{-}HS}$.

3. The thermal resistance from heat sink to ambient, $\theta_{HS\text{-}A}$, is determined by the heat sink and environmental factors such as air flow or convection currents.

The total thermal resistance, $\theta_{J\text{-}A}$, is the sum of these three thermal resistances. The required θ for the heat sink ($\theta_{HS\text{-}A}$) is equal to the total thermal resistance less the $\theta_{J\text{-}C}$ and $\theta_{C\text{-}HS}$.

$$\theta_{HS\text{-}A} = \theta_{J\text{-}A} - \theta_{J\text{-}C} - \theta_{C\text{-}HS}$$

continuing the previous example:

$\theta_{J\text{-}A}$ = 4.8°C/W (from previous calculation)
$\theta_{J\text{-}C}$ = 2.2°C/W (from power amp specification)
$\theta_{C\text{-}HS}$ = 0.2°C/W (good surface with thermal compound)
$\theta_{HS\text{-}A} = 4.8 - 2.2 - 0.2 = 2.4$°C/W

The required heat sink must have a thermal resistance of 2.4°C/W (or lower) to adequately cool the power amp.

It is conceivable that this calculation might result in a negative number for $\theta_{HS\text{-}A}$. This means that a perfect or infinite heat sink is not good enough. This would result in operation beyond the power derating curve for the power amp—an alternative approach must be selected.

Once the required θ for a heat sink is determined, it may be compared to published data for commercially available heat sinks. This step should be taken with some caution, however. Published specifications for heat sinks vary considerably for essentially identical designs. Heat sink performance varies greatly depending on the mounting configuration, surrounding components, air flow and other environmental factors. Published data may be used as a guideline to performance, but it is prudent to measure actual performance in your application. In fact this may be the only way to effectively evaluate heat sink performance with custom designed heat sinks, fans, stacked circuit boards, high altitude, or other unusual conditions.

It is easy to verify thermal performance by measuring the power amp's actual case temperature under operating conditions. T_{CASE} is measured by placing a thermocouple under one of the mounting screws of the power amp (or at a place on the case specifically indicated by the manufacturer for such a measurement). The junction temperature can then be calculated:

$$T_J = P\theta_{J\text{-}C} + T_{CASE}$$

e.g.: P = 25W (dependent on application)
$\theta_{J\text{-}C}$ = 2.2°C/W (from power amp specification)
T_{CASE} = 95°C (as measured with thermocouple)
$T_J = (25)(2.2) + 95 = 150$°C (safe)

This is the most direct means of assuring that the junction temperature is maintained within safe bounds. This approach still requires knowledge of the power amplifier dissipation. For AC signals, reactive loads, motors or widely varying signal conditions (such as voice or music) this may be difficult to calculate. Application Note AN-123 gives hints on how to handle these situations.

NOISE ANALYSIS OF FET TRANSIMPEDANCE AMPLIFIERS

The availability of detailed noise spectral density characteristics for the OPA111 amplifier allows an accurate noise error analysis in a variety of different circuit configurations. The fact that the spectral characteristics are guaranteed maximums allows absolute noise errors to be truly bounded. Other FET amplifiers normally use simpler specifications of rms noise in a given bandwidth (typically 10Hz to 10kHz) and peak-to-peak noise (typically specified in the band 0.1Hz to 10Hz). These specifications do not contain enough information to allow accurate analysis of noise behavior in any but the simplest of circuit configurations.

Noise in the OPA111 can be modeled as shown in Figure 1. This model is the same form as the DC model for offset voltage (E_{OS}) and bias currents (I_B). In fact, if the voltage $e_n(t)$ and currents $i_n(t)$ are thought of as general instantaneous error sources, then they could represent either noise or DC offsets. The error equations for the general instantaneous model are shown in Figure 2.

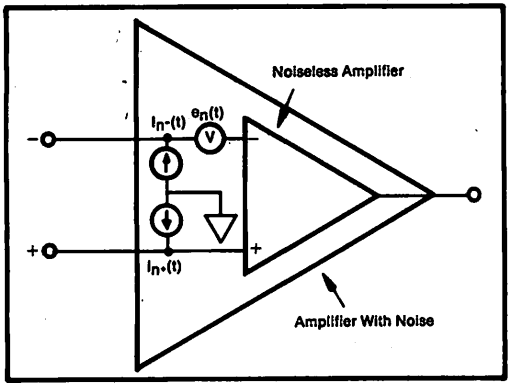


FIGURE 1. Noise Model of OPA111.

If the instantaneous terms represent DC errors (i.e., offset voltage and bias currents) the equation is a useful tool to compute actual errors. It is not, however, useful in the same *direct* way to computer noise errors. The basic problem is that noise cannot be predicted as a function of time. It is a random variable and must be described in probabilistic terms. It is normally described by some type of average—most commonly the rms value.

$$N\ \text{rms} \triangleq \sqrt{1/T \int_0^T n^2(t)\, dt} \qquad (1)$$

where N rms is the rms value of some random variable n(t). In the case of amplifier noise, n(t) represents either $e_n(t)$ or $i_n(t)$.

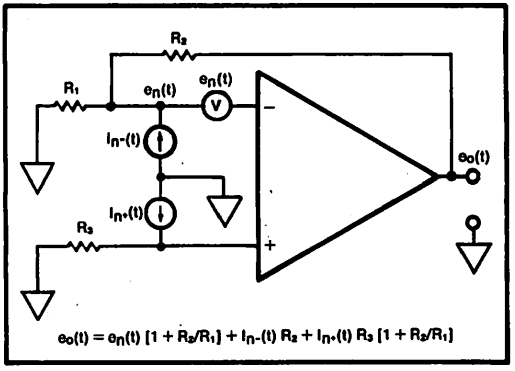


FIGURE 2. Circuit With Error Sources.

The internal noise sources in operational amplifiers are normally uncorrelated. That is, they are randomly related to each other in time and there is no systematic phase relationship. Uncorrelated noise quantities are combined as root-sum-squares. Thus, if $n_1(t)$, $n_2(t)$, and $n_3(t)$ are uncorrelated then their combined value is

$$N_{TOTAL}\ \text{rms} = \sqrt{N_1^2\ \text{rms} + N_2^2\ \text{rms} + N_3^2\ \text{rms}} \qquad (2)$$

The basic approach in noise error calculations then is to identify the noise sources, segment them into conveniently handled groups (in terms of the shape of their noise spectral densities), compute the rms value of each group, and then combine them by root-sum-squares to get the total noise.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. It will be used to demonstrate the above noise calculation method.

CR1 is a PIN photo diode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{IN} when exposed to the light, λ.

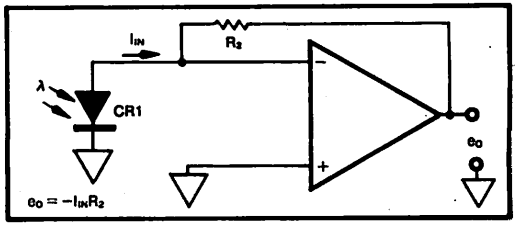


FIGURE 3. Pin Photo Diode Application.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 is what would be expected from stray capacitance with moderately careful layout (0.5pF to 2pF). A larger value of C_2 would normally be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

In Figure 4, e_n and i_n represent the amplifier's voltage and current spectral densities, $e_n(\omega)$ and $i_n(\omega)$ respectively. These are shown in Figure 5.

Figure 6 shows the desired "gain" of the circuit (transimpedance of $e_o/i_{IN} = Z_2(s)$). It has a single-pole

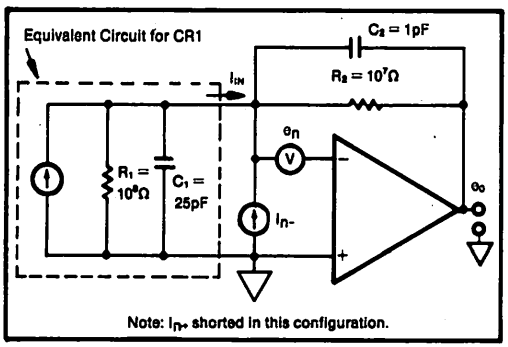
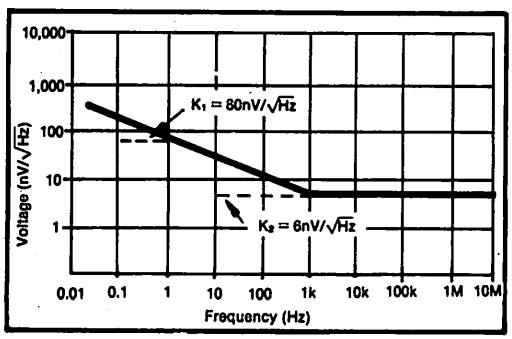
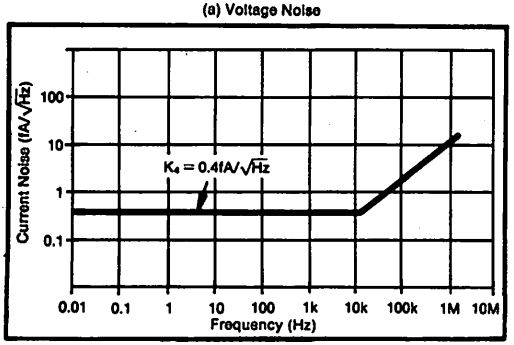


FIGURE 4. Noise Model of Photo Diode Application.



(a) Voltage Noise



(b) Current Noise

FIGURE 5. Noise Voltage and Current Spectral Density.

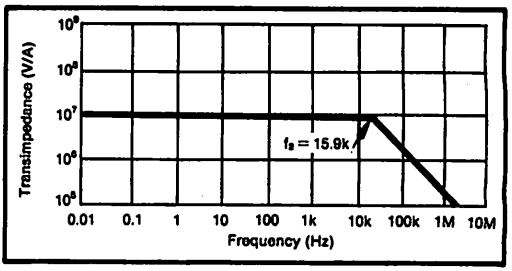


FIGURE 6. Transimpedance.

rolloff at $f_2 = 1/(2\pi R_2 C_2) = \omega_2/2\pi$. Output noise is minimized if f_2 is made smaller. Normally R_2 is chosen for the desired DC transimpedance based on the full scale input current (i_{IN} full scale) and maximum output (e_o max). Then C_2 is chosen to make f_2 as small as possible consistent with the necessary signal frequency response.

Voltage Noise

Figure 7 shows the noise voltage gain for the circuit in Figure 4. It is derived from the equation

$$e_o = e_n\left[\frac{A}{1+A\beta}\right] = e_n\frac{1}{\beta}\left[\frac{1}{1+\frac{1}{A\beta}}\right] \quad (3)$$

where:

A = $A(\omega)$ is the open-loop gain

β = $\beta(\omega)$ is the feedback factor. It is the amount of output voltage feedback to the input of the op amp.

$A\beta$ = $A(\omega)\ \beta(\omega)$ is the loop gain. It is the amount of the output voltage feedback to the input and then amplified and returned to the output.

Note that for large loop gain ($A\beta >> 1$)

$$e_o \cong e_n\ \frac{1}{\beta} \quad (4)$$

For the circuit in Figure 4 it can be shown that

$$\frac{1}{\beta} = 1 + \frac{R_2(R_1C_1s + 1)}{R_1(R_2C_2s + 1)} \quad (5)$$

This may be rearranged to

$$\frac{1}{\beta} = \frac{R_2 + R_1}{R_1}\left[\frac{\tau_a s + 1}{\tau_2 s + 1}\right] \quad (5a)$$

where $\tau_a = (R_1 \parallel R_2)(C_1 \parallel C_2)$ (5b)

$$\frac{1}{\beta} = \left[\frac{R_1R_2}{R_1 + R_2}\right]\ (C_1 + C_2)$$

and $\tau_2 = R_2C_2$. (5c)

Then, $f_a = \frac{1}{2\pi\,\tau_a}$ and $f_2 = \frac{1}{2\pi\,\tau_2}$ (5d)

For very low frequencies ($f << f_a$), s approaches zero and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{R_2}{R_1}. \quad (6)$$

For very high frequencies ($f >> f_2$), s approaches infinity and equation 5 becomes

$$\frac{1}{\beta} = 1 + \frac{C_1}{C_2}. \quad (7)$$

The noise voltage spectral density at the output is obtained by multiplying the amplifier's noise voltage spectral density (Figure 5a) times the circuits noise gain (Figure 7). Since both curves are plotted on log-log scales the multiplication can be performed by the addition of the two curves. The result is shown in Figure 8.

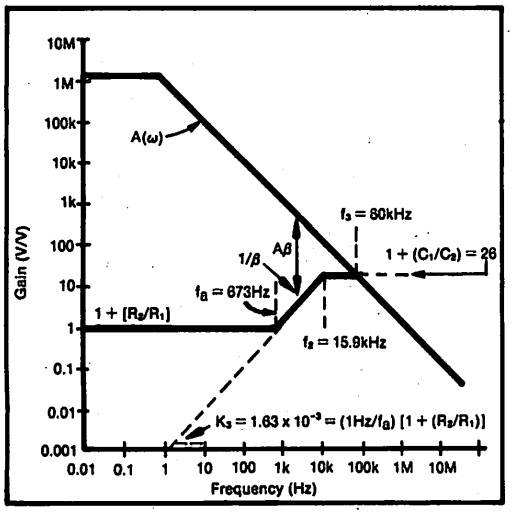


FIGURE 7. Noise Voltage Gain.

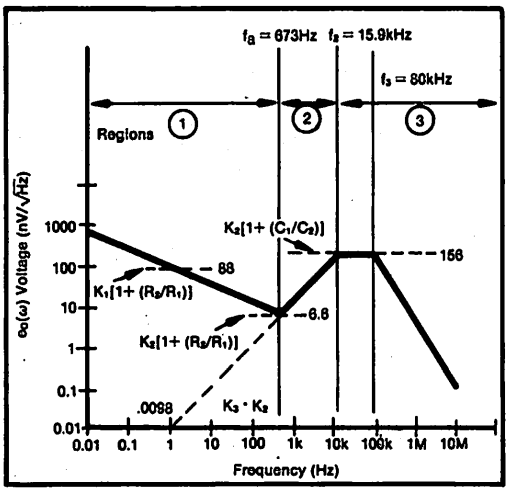


FIGURE 8. Output Voltage Noise Spectral Density.

The total rms noise at the amplifier's output due to the amplifier's internal voltage noise is derived from the $e_o(\omega)$ function in Figure 8 with the following expression:

$$E_o \text{ rms} = \sqrt{\int_{-\infty}^{+\infty} e_o^2(\omega)\, d\omega} \qquad (8)$$

It is both convenient and informative to calculate the rms noise using a piecewise approach (region-by-region) for each of the three regions indicated in Figure 8.

Region 1; $f_1 = 0.01\text{Hz}$ to $f_c = 100\text{Hz}$

$$E_{n1} \text{ rms} = K_1\left[1 + \frac{R_2}{R_1}\right]\sqrt{\ln\left(\frac{f_c}{f_1}\right)} \qquad (9)$$

$$= 80\text{nV}/\sqrt{\text{Hz}}\left[1 + \frac{10^7}{10^8}\right]\sqrt{\ln\left(\frac{673}{0.01}\right)} \qquad (9a)$$

$$= 0.293\mu\text{V}$$

This region has the characteristic of $1/f$ or "pink" noise (slope of -10dB per decade on the log-log plot of $e_n\omega$). The selection of 0.01Hz is somewhat arbitrary but it can be shown that for this example there would be only negligible additional contribution by extending f_1 several decades lower. Note that $K_1(1 + R_2/R_1)$ is the value of e_o at $f = 1\text{Hz}$.

Region 2; $f_a = 673\text{Hz}$ to $f_2 = 15.9\text{kHz}$

$$E_{n2} \text{ rms} = K_2 \bullet K_3\sqrt{\frac{f_2^3}{3} - \frac{f_a^3}{3}} \qquad (10)$$

$$= \left(6\text{nV}/\sqrt{\text{Hz}}\right)(1.63 \times 10^{-3})\sqrt{\frac{(15.9\text{kHz})^3}{3} - \frac{(673)^3}{3}} \qquad (10a)$$

$$= 11.3\mu\text{V}$$

This is the region of increasing noise gain (slope of +20dB/decade on the log-log plot) caused by the lead network formed by the resistance $R_1 \parallel R_2$ and the capacitance $(C_1 + C_2)$. Note that $K_3 \bullet K_2$ is the value of the $e_o(\omega)$ function for this segment projected back to 1Hz.

Region 3; $f > 15.9\text{kHz}$

$$E_{n3} \text{ rms} = K_2\left(1 + \frac{C_1}{C_2}\right)\sqrt{\left(\frac{\pi}{2}\right)f_3 - f_2} \qquad (11)$$

$$= \left(6\text{nV}/\sqrt{\text{Hz}}\right)\left(1 + \frac{25}{1}\right)\sqrt{\left(\frac{\pi}{2}\right)(80\text{K}) - 15.9\text{K}} \qquad (11a)$$

$$= 51.7\mu\text{V}$$

This is a region of white noise with a single order rolloff at $f_3 = 80\text{kHz}$ caused by the intersection of the $1/\beta$ curve and the open-loop gain curve. The value of 80kHz is obtained from observing the intersection point of Figure 7. The $\pi/2$ applied to f_3 is to convert from a 3dB corner frequency to an effective noise bandwidth.

Current Noise

The output voltage component due to current noise is equal to:

$$E_{ni} = i_n \times Z_2(s) \qquad (12)$$

where $Z_2(s) = R_2 \parallel X_{C_2}$ (12a)

This voltage may be obtained by combining the information from Figures 5 (b) and 6 together with the open loop gain curve of Figure 7. The result is shown in Figure 9.

Using the same techniques that were used for the voltage noise:

Region 1; 0.1Hz to 10kHz

$$E_{ni1} = 4 \times 10^{-9}\sqrt{10\text{K} - 0.1} \qquad (13)$$

$$= 0.4\mu\text{V}$$

Region 2; 10kHz to 15.9kHz

$$E_{ni2} = 4 \times 10^{-13}\sqrt{\frac{(15.9\text{kHz})^3}{3} - \frac{(10\text{kHz})^3}{3}}$$

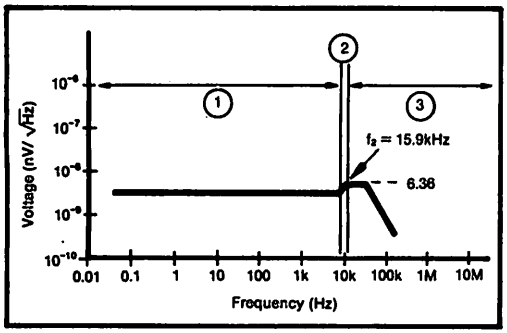


FIGURE 9. Output Voltage Due to Noise Current.

$$= 0.4\mu V \quad (13a)$$

Region 3; f > 15.9kHz

$$E_{ni_3} = 6.36 \times 10^{-9} \sqrt{\frac{\pi}{2}(80kHz) - 15.9kHz}$$

$$= 2.1\mu V \quad (13b)$$

$$E_{ni\ TOTAL} = 10^{-6} \sqrt{(0.4)^2 + (0.4)^2 + (2.1)^2}$$

$$= 2.2\mu Vrms \quad (13c)$$

Resistor Noise

For a complete noise analysis of the circuit in Figure 4, the noise of the feedback resistor, R_2, must also be included. The thermal noise of the resistor is given by:

$$E_R\ rms = \sqrt{4kTRB} \quad (14)$$

K = Boltzmann's constant = 1.38 x 10^{-23} Joules/°Kelvin
T = Absolute temperature (degrees Kelvin)
R = Resistance (ohms)
B = Effective noise bandwidth (Hz) (ideal filter assumed)

At 25°C this becomes

$E_R\ rms \cong 0.13\sqrt{RB}$
E_R rms in μV
R in MΩ
B in Hz

For the circuit in Figure 4

$R_2 = 10^7\Omega = 10M\Omega$
$B = \frac{\pi}{2}(f_2) = \frac{\pi}{2}\ 15.9k$

Then

$$E_R\ rms = (411nV/\sqrt{Hz})\sqrt{B}$$

$$= (411nV/\sqrt{Hz})\sqrt{\tfrac{\pi}{2}\ 15.9kHz}$$

$$= 64.9\mu Vrms$$

Total Noise

The total noise may now be computed from

$$E_{n\ TOTAL} = \sqrt{E_{n1}^2 + E_{n2}^2 + E_{n3}^2 + E_{nR}^2 + E_{ni}^2} \quad (15)$$

$$= 10^{-6}\sqrt{(0.293)^2+(11.3)^2+(51.7)^2+(64.9)^2+(2.2)^2} \quad (15a)$$

$$= 83.8\mu Vrms$$

Conclusions

Examination of the results in equation (16b) together with the curves in Figure 8 leads to some interesting conclusions.

The largest component is the resistor noise E_{nR} (60% of the total noise). A lower resistor value decreases resistor noise as a function of $\sqrt{R}$, but it also lowers the desired signal gain as a direct function of R. Thus, lowering R reduces the signal-to-noise ratio at the output which shows that the feedback resistor should be as large as possible. The noise contribution due to R_2 can be decreased by raising the value of C_2 (lowering f_2) but this reduces signal bandwidth.

The second largest component of total noise comes from E_n (38%). Decreasing C_1 will also lower the term $K_2(1 + C_1/C_2)$. In this case, f_2 will stay fixed and f_a will move to the right (i.e., the +20dB/decade slope segment will move to the right). This can have a significant reduction on noise without lowering the signal bandwidth. This points out the importance of maintaining low capacitance at the amplifier's input in low noise applications.

It should be noted that increasing C_2 will also lower the value of $K_2(1 + C_1/C_2)$, and the value of f_2 (see equation 5b). This reduces signal bandwidth and the final value of C_2 is normally a compromise between noise gain and necessary signal bandwidth.

It is interesting to note that the current noise of the amplifier accounted for only 0.1% of the total E_n. This is different than would be expected when comparing the current and voltage spectral densities with the size of the feedback resistor. For example, if we define a characteristic value of resistance as

$$R_{CHARACTERISTIC} = \frac{e_n(\omega)}{i_n(\omega)} \text{ at } f = 10kHz \quad (16)$$

$$= \frac{6nV/\sqrt{Hz}}{0.4fA/\sqrt{Hz}}$$

$$= 15M\Omega$$

Thus, in simple transimpedance circuits with feedback resistors greater than the characteristic value, the amplifier's current noise would cause more output noise than the amplifier's voltage noise. Based on this and the 10MΩ feedback resistor in the example, the amplifier noise current would be expected to have a higher contribution than the noise voltage. The reason it does not in the example of Figure 4 is that the noise voltage has high gain at higher frequencies (Figure 7) and the noise current does not (Figure 6).

ONE SUPPLY POWERS PRECISION BRIDGE CIRCUIT

Precise amplification and a high common-mode rejection ratio make an instrumentation amplifier well suited to the task of monitoring the output of a resistive transducer bridge. For systems with only one power supply, Figure 1 shows how you can connect the bridge, the instrumentation amp, and an op amp to provide a buffered reference for the instrumentation amp's output.

For linear operation, the amplifier inputs (and outputs) must come within no more than several volts of either ground or V+. Accordingly, the bridge properly biases both amplifier inputs, and the instrumentation amp's high CMRR ensures little error from this large offset.

The OPA111AM buffers the reference node of the bridge and applies that voltage to the instrumentation amp's Reference terminal. (Most instrumentation amplifiers include a Reference terminal, which may be biased to offset the output.) You measure between the amplifier outputs to exclude the fixed output offset.

The op amp output can serve as a reference common for all connections following the instrumentation amp—this output provides low impedance over a frequency range well beyond that of the bridge signal. To handle higher-frequency currents, connect capacitance between the op amp output and ground; if necessary, decouple this capacitance with a small resistor within the op amp's feedback loop.

The error introduced by the additional op amp is small. The input bias current I_B of the op amp creates a bridge error of $I_B \times R/2$, where R is the resistance of one leg of the bridge. Input offset voltage has no effect on the output voltage; it adds to the output offset with respect to ground, which is excluded from the measurement.

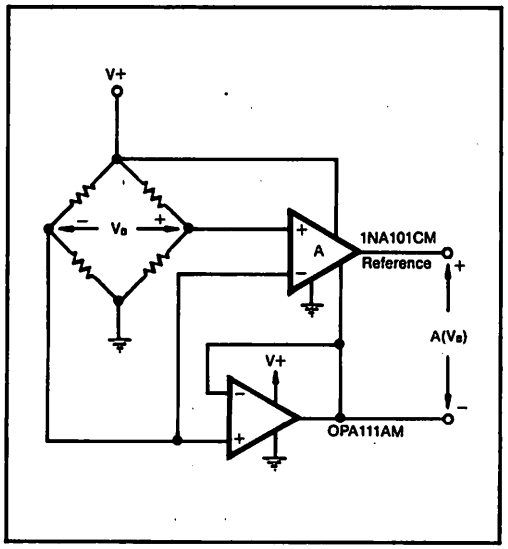


FIGURE 1. Use one power supply to excite the bridge and to develop a buffered output signal in this precision circuit.

PHOTODIODE MONITORING WITH OP AMPS

With their low-input currents, FET input op amps are universally used in monitoring photodetectors, the most common of which are photodiodes. There are a variety of amplifier connections for this purpose and the choice is based on linearity, offset, noise and bandwidth considerations. These same factors influence the selection of the amplifier with newer devices offering very low-input currents, low noise and high speed.

Photodetectors are the bridge between a basic physical indicator and electronics resulting in the largest single usage of FET op amps. As a measure of physical conditions light is secondary to temperature and pressure until the measurement is made remotely with no direct contact to the monitored object. Then, the signals of a CAT scanner, star-tracking instrument or electron microscope depend on light for the final link to signal processing. Photodiodes have made that link economical and expanded usage to detector arrays that employ more than 1000 light sensors. Focus then turns to accurate conversion of the photodiode output to a linearly related electrical signal. As always, this is a contest between speed and resolution with noise as a basic limiting element. Central to the contest is the seemingly simple current-to-voltage converter which displays surprising multidimensional constraints and suggests alternative configurations for many optimizations.

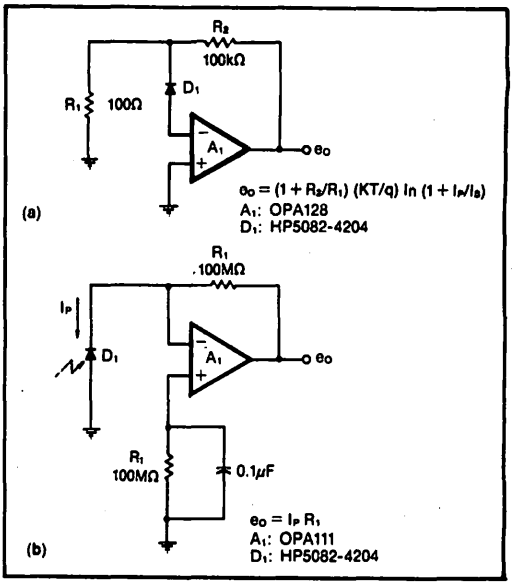


FIGURE 1. Photodiode output can be monitored (a) as a voltage or (b) as a current.

CURRENT-TO-VOLTAGE

The energy transmitted by light to a photodiode can be measured as either a voltage or current output. For a voltage response the diode must be monitored from a high impedance that does not draw significant signal current. That condition is provided by Figure 1a. Here, the photodiode is in series with the input of an op amp where ideally zero current flows. That op amp has feedback set by R_1 and R_2 to establish amplification of the voltage diode just as if it was an offset voltage of the amplifier. While appealing to more common op amp thinking, this voltage mode is nonlinear. The response has a logarithmic relationship to the light energy received since the sensitivity of the diode varies with its voltage.

Constant voltage for a fixed sensitivity suggests current output instead and that response is linearly related to the incident light energy. A monitor of that current must have zero input impedance to respond with no voltage across the diode. Zero impedance is the role of an op amp virtual ground as high-amplifier loop gain removes voltage swing from the input. That is the key to the basic current-to-voltage converter connection of Figure 1b. It provides an input resistance of R_1/A where A is the open-loop gain of the op amp. Even though R_1 is generally very large, the resulting input resistance remains negligible in comparison to the output resistance of photodiodes.

Diode current is not accepted by the input of the op amp as its presence stimulates the high amplifier gain to receive that current through the feedback resistor R_1. To do so the amplifier developes an output voltage equal to the diode current times the feedback resistance, R_1. For that current-to-voltage gain to be high, R_1 is made as large as other constraints will permit. At higher resistance levels, that resistor begins to develop significant thermal DC voltage drift due to the temperature coefficient of the amplifier input current. To compensate this error, an equal resistance R_2 is commonly connected in series with the op amp noninverting input, as shown, and capacitively bypassed to remove most of its noise. The remaining DC error is determined by the mismatches between the amplifier input currents and between the two resistors. A drawback of this error correction is the voltage drop it creates across the diode and the resulting diode leakage current. That leakage can override the correction achieved with R_2, as photodiodes typically have large junction areas for high sensitivity. Leakage current is proportional to that area which can become much larger than the op amp input currents.

Only zero diode voltage can eliminate this new error source but that is in conflict with control of a second attribute of large diode area. Large parasitic capacitance is also present creating often severe amplification of noise as will be described. To reduce that capacitance a large reverse-bias voltage is sometimes impressed on the diode greatly complicating DC stability and making current noise from the photodiode an additional error factor. Larger diode area may actually degrade overall accuracy and higher photo sensitivity should first be sought through optical means such as a package with an integral molded lens. Monitor-circuit configurations that maintain zero diode voltage are also candidates in this optimization and are described with Figures 6, 7 and 9.

The value of the feedback resistor in a current-to-voltage converter largely determines noise and bandwidth as well as gain. Noise contributed directly by the resistor has a spectral density of $\sqrt{4KTR}$[1] and appears directly at the output of a current-to-voltage converter without amplification. Increasing the size of the resistor raises output noise by a square root relationship but also increases output signal by a direct proportionality. Signal-to-noise ratio, then, tends to increase by the square root of the resistance.

Noise from the op amp also influences the output with a surprising effect introduced by high feedback resistance and the diode capacitance. The amplifier noise sources are modeled in Figure 2a as an input noise current i_n and the input noise voltage e_n. The current noise flows through the feedback resistor experiencing the same gain as the signal current. It is the shot noise of the input bias current I_B and has a noise denisty of $\sqrt{2qI_B}$ [1]. Choice of an op amp having input currents in the picoamp range makes this noise component negligible for practical levels of feedback resistance. Input noise voltage of the amplifier would at first seem to be transferred with low gain to the output. That is true at DC where its gain $1 + R_1/R_D$ is kept small by the large diode resistance R_D. Capacitance C_D of the diode alters the feedback at higher frequencies adding very significant gain to e_n. As both the capacitance and the feedback resistance are commonly large, the effect can begin at fairly low frequencies. Figure 2b illustrates the effect with an op amp gain magnitude curve plotted with the reciprocal of the feedback factor or the "noise gain." That gain curve first experiences a response zero due to C_D and begins a rise that is terminated only because of a second parasitic capacitance. Stray capacitance C_S shunts the feedback resistor resulting in a response pole leveling the gain at $1 + C_D/C_S$. For large area diodes C_D can be hundreds of picofarads causing the noise gain to peak in the hundreds as well. That gain continues to higher frequencies until rolled off by the op amp bandwidth limit. As feedback resistance increases, the pole and zero of this gain peaking move together to lower frequencies encompasing a greater spectrum with high gain.

First signs of this gain peaking phenomena are familiar to anyone who has used high resistance op amp feedback in more general circuits. High output to input resistance

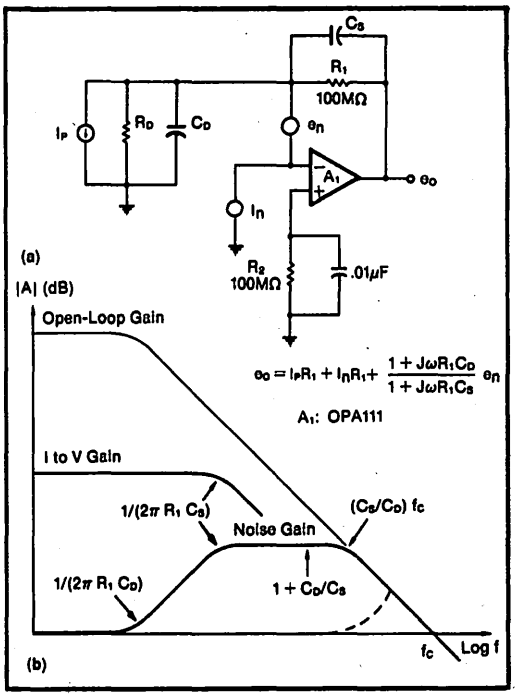


FIGURE 2. Due to (a) diode capacitance in the feedback of the basic current-to-voltage converter, (b) op amp noise receives gain and bandwidth not available to the signal.

with an op amp results in overshoot, response peaking, poor settling or even oscillation all due to the resistance interaction with amplifier input capacitance. Together the resistance and capacitance form another pole in the feedback loop resulting in the classic differentiator feedback response. Shown by the dashed line for more general op amp cases, the associated feedback factor reciprocal intercepts the amplifier open loop magnitude response with a 12dB/octave rate of closure corresponding to feedback phase shift approaching or equal to 180°. The common cure for this condition is a capacitor across the feedback resistor, which for the very high resistances of current-to-voltage converters, automatically results from stray capacitance. Such capacitance degenerates the added feedback pole to control phase shift in the feedback loop.

In understanding current-to-voltage converter noise performance it is important to note that the signal current and the noise voltage encounter entirely different frequency responses. The current-to-voltage gain is flat with frequency until the feedback impedance is rolled off by stray capacitance as shown. Gain received by the amplifier noise voltage, on the same graph, extends well beyond that roll-off and is high in that extended region. The majority of the op amp's bandwidth often serves only to amplify that noise error and not the signal. This is typically the dominant source of noise for higher feedback resistances.

Relative effects of the major noise sources of a current-to-voltage converter can be seen with the curves of Figure 3. Those curves show output noise for the basic current-to-voltage converter of Figure 1b including the effects of the noise gain represented in Figure 2b. Plotted are total output noises for three cases as a function of feedback resistance and each is the rms sum of the components produced by the feedback resistor and an op amp. Represented are three FET op amps having different performance specialties that cover the spectrum of photodiode applications with low noise, low-input-bias current and high speed. While all three types have low-noise designs and low-input currents the OPA111 offers the lowest noise in the FET op-amp class at $6nV/\sqrt{Hz}$ and the OPA128 has the lowest input current at .075pA. Without neglecting performance in these categories the OPA404 design pushes bandwidth to 6.4MHz. Noise due to the op amp is found by integrating the amplifier noise density spectral response over the noise gain response.[2] Also shown, by a dashed line, is the noise due to the resistor alone for the OPA111 and OPA2111 case. This resistor noise curve is different for the other op amps as each amplifier has a different bandwidth rolling off noise due to the resistor.

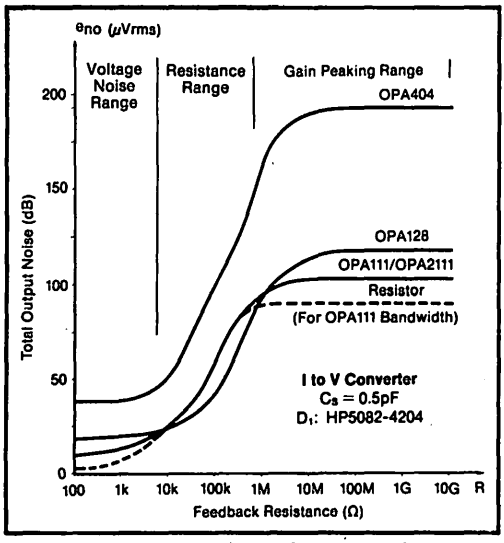


FIGURE 3. As the feedback resistance of a current-to-voltage converter increases, the dominant noise source changes from the op amp to the resistor and back to the op amp under gain peaking conditions.

Different factors control the noise curves for different ranges of feedback resistance. At low resistance levels, the noise curves are largely flat with the op amp voltage noise the dominant contributor. That domination makes initial resistance increases have little effect except for the case of the very low-voltage noise of the OPA111/OPA2111. In this region noise gain peaking has not yet been encountered so the output noise remains small. Between 10kΩ and 1MΩ, resistor noise is dominant and the curves track that error source as the dashed line shows for the OPA111/OPA2111. Here, the curves demonstrate the square root relationship with the resistance and differ only because of amplifier bandwidths. At still higher resistance, noise gain peaking takes effect returning the op amp noise to dominance and boosting the curves higher. That effect is first demonstrated by the increased slope of the OPA404 curve as that amplifier's wide bandwidth first encompasses the peaking. The noise curves level off when essentially the full amplifier bandwidth is encompassed by the gain peaking. Moving to yet higher resistance, resistor noise would return the curves to rising slopes but resistor bandwidth is by then rolled off by stray capacitance. In this upper region, any increase in resistance is accompanied by a matching reduction in noise bandwidth so that the total resistor noise becomes a constant. Variables of diode and stray capacitances alter the point of onset of gain peaking errors but the characteristic shape of the output noise curves remains the same for any case. Each will display ranges dominated by op amp noise, resistor noise and gain peaking effects.

Comparing the curves shows the OPA111/OPA2111 to provide lowest noise in two of the characterisitic ranges. While the OPA128 shows a lower noise curve in the middle range, that is due to the amplifier's lower bandwidth and a bandwidth reduction technique to be described, removes that difference for the OPA111. Where the OPA128 excels is in very low DC error as its input currents are a mere 0.075pA which is 1/20th that of its low-noise contender. The third op amp, OPA404, produces higher total output noise overall but that again is largely a bandwidth phenomenon. The 6.4MHz response of that amplifier accommodates noise over a much greater frequency range. While the noise curve for this amplifier is consistently higher than that of the OPA128, the OPA404 actually has lower noise density but it has six times the bandwidth. That 6.4MHz bandwidth is available to signals for feedback resistances up to 50kΩ and the amplifier still offers the best bandwidth for resistances up to 150kΩ. As the OPA404 is a quad op amp, its economy suggests consideration for use at even higher resistances along with bandwidth reduction that provides more competitive output noise.

Only a five dimensional graph could display the output noise, resistance, DC error, diode area and signal bandwidth considered in current-to-voltage converter design. Each specific application's requirements are evaluated separately with respect to these factors. To avoid sub-optimizing a given design for one factor such as gain, the various effects of increasing feedback resistance are anticipated at each step. Choices such as large diode area are made considering the related capacitance and its effect on output noise and overall circuit sensitivity.

NOISE CONTROL

Gain peaking effects are the primary noise limitation with the commonly preferred high feedback resistances. To limit this effect, or to eliminate the gain rise entirely, additional capacitance is commonly added to bypass the

feedback resistor. The capacitance level required can be very small for some values of R_1 and the relative significance of unpredictable stray capacitance make tuning desirable. Combined, these requirements are a challenge better resolved with a capacitor tee network as described in Figure 4a. It is capable of even sub-picofarad tunable capacitance with little effect on stray capacitance in the tuning operation. The tee uses a capacitive divider formed with C_2 and C_3 to attenuate the signal applied to C_1 at the circuit input. With only a fraction of the output signal on C_1, it supplies far less shunting current to the input node as would a much smaller capacitor. Controlling the attenuation ratio is the tunable C_3 which is the largest of the capacitors so its capacitance value is more readily available in tunable form. Since that capacitor is grounded, it has a shielding advantage to reduce stray capacitance influence while tuning.

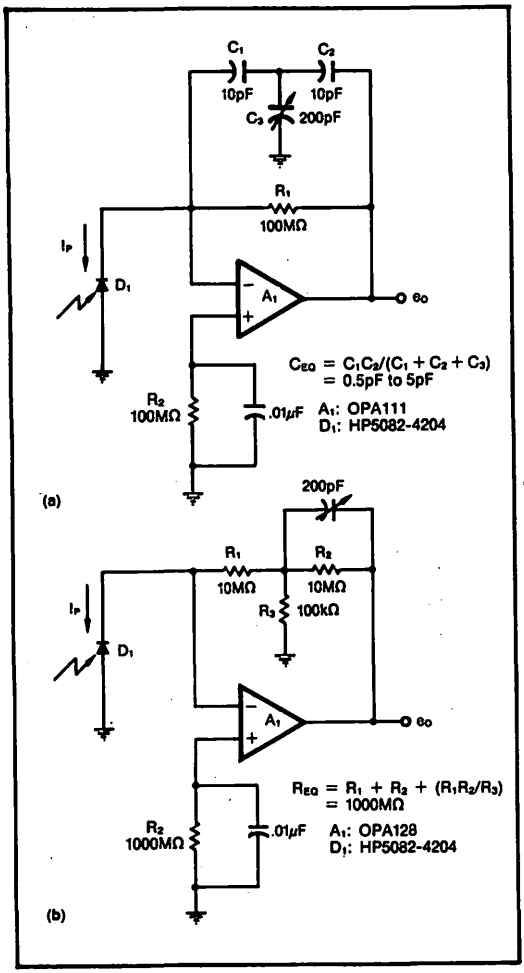


FIGURE 4. Removal of amplifier gain peaking through small capacitive bypass of large feedback resistance is more feasible with (a) a capacitor tee or (b) bypass of one element of a feedback resistor tee.

Another option for practical feedback bypass exists with a resistor tee which is a commonly considered replacement for the high value feedback resistor. The latter is replaced in Figure 4b by elements of more reasonable value but introduces greater low frequency noise. Its operation is the dual of the capacitor tee above with R_2 and R_3 attenuating the signal to R_1 so that the latter appears as a much larger resistor to the input node. A similar opportunity for the DC error compensation resistor R_2 does not exist. DC error due to amplifier input current is no different with the tee so the large compensation resistor is still needed.

Stray capacitance across the feedback is somewhat reduced with the resistor tee by the added physical spacing of the feedback with three elements. Also, stray capacitance across each individual element has much less effect with their lower resistances. Sensitivity to other stray capacitance from the op amp output to its input has the same effect as before.

In the attenuation network of the feedback is the opportunity for intentional bypass with reasonable capacitor values. Bypassing the moderate resistance of R_2 removes the attenuation at higher frequencies leaving the net feedback resistance at the level of R_1. This operation differs from true feedback bypass in that impedance levels off, rather than continuing to fall with frequency, but the dramatic drop in equivalent resistance serves the circuit requirement. Another benefit offered by the resistor tee is more accurate DC error compensation.

Reduced high frequency noise with the tee element bypass is accompanied by an opposing increase at lower frequencies. Below the frequency of the bypass, noise gain is increased by the feedback attenuation of the tee network. That amplifies the noise and offset voltages of the op amp as well as the noise of resistor R_1 by a factor of $1 + R_2/R_3$. Countering the latter is the resistor's smaller value so that this effect is increased only by the square root of the new noise gain. Most important, however, is the bypass capacitor removal of high frequency gain as it eliminates the greatest portion of previous noise bandwidth. In the absence of other means to remove the high frequencies, the bypassed resistor tee provides lower total output noise for the higher ranges of feedback resistance.

Adding feedback capacitance is an effective means of reducing noise gain but it also decreases signal bandwidth by the same factor. That bandwidth is already low with high feedback resistance and the end result can be a response of a kilohertz or less. A more desirable solution to the noise problem is to limit amplifier bandwidth to a point just above the unavoidable signal bandwidth limit. Then, the high frequency gain which only amplifies noise is removed. Op amps with provision for external phase compensation offer this option but those available lack the low-input currents and low-voltage noise needed for photodiode monitoring.

To achieve this bandwidth limiting with better suited op amps, a composite amplifier uses two op amps with the

added one for phase compensation control as in Figure 5a. Note the reversal of the inverting and noninverting inputs of A_1 needed to retain a single phase inversion with two amplifiers in series. With the composite structure internal feedback controls the frequency response of the gain added by A_2. At DC, that feedback is blocked by C_1 and overall open-loop gain is the product of those of the two amplifiers or 225dB for those shown. That gain is rolled off by the open-loop pole of A_1 and by the integrator response established for A_2 by C_1 and R_3. As this is a two pole roll-off, it must be reduced before intercepting the noise gain curve to establish frequency stability. A response zero does this due to the inclusion of R_4. Above the frequency of that zero, R_4 also replaces the integrator response with that of an inverting amplifier having a gain of $-R_4/R_3$. Making that gain less than unity drops the net gain magnitude curve below that of a single amplifier at high frequencies. Graphically, the noise gain response of Figure 5b is moved back in frequency much as if the op amp bandwidth had been reduced.

Eliminated is the shaded area of noise gain, which visually may not appear dramatic, but that is because of the logarithmic-frequency scale. Actually, the associated noise reduction is large because most of the amplifier's bandwidth is represented in this upper end of the logarithmic-response curve. Moving the unity gain crossover of the noise gain from 2MHz to 200kHz, as shown, drops the output noise due to A_1 by about a factor of three. To achieve the same result with feedback bypass, the signal bandwidth would have been reduced a factor of ten. That bandwidth is unaffected with the Figure 5a approach. No noise, or offset, is added by A_2 as this amplifier is preceded by the high gain of A_1. With the exceptionally low noise of the OPA111 input amplifier this improvement reduces noise to the fundamental limitation imposed by that of the feedback resistor. This condition is retained for all practical levels of high feedback resistance. For the second amplifier the wideband OPA404 is shown to continue its attenuating amplifier action well beyond the unity gain crossover of A_1. This avoids a second gain peak that could cause oscillation. Signal bandwidth of the current-to-voltage conversion is essentially unaffected as R_1 has not been influenced.

Where the Figure 5 technique is most useful is with lower level signals that have greater sensitivity to noise. In higher level applications that circuit can encounter a voltage swing limitation but another use of the second amplifier offers similar noise improvement. The swing limitation results from the maximum output voltage limit of A_1 and its attenuation by A_2. If the output of A_1 has a peak swing of 12V and A_2 has the gain of $-1/10$ illustrated, the final output is limited to a 1.2V peak swing. For lower-level signals this will be acceptable as the maximum practical level of feedback resistance already limits output swing.

Higher-level signals are not as senstitive to noise and better tolerate a more straight forward approach to filtering. An active filter following the conventional

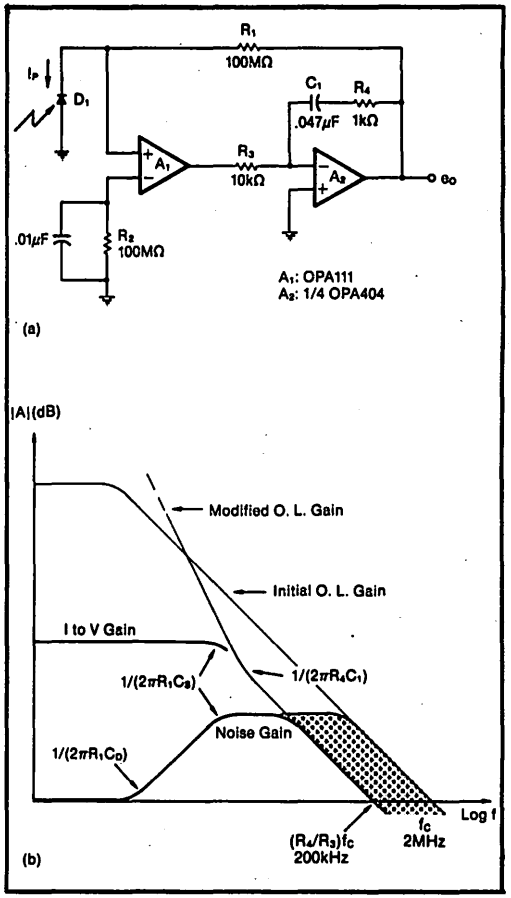


FIGURE 5. Noise reduction results with (a) a composite amplifier that (b) restricts noise bandwidth without reducing that of the signal.

current-to-voltage converter also removes the high frequency noise. Setting filter poles at the frequency of the signal bandwidth results in a system bandwidth that does not extend beyond that of useful information. Such a filter is not enclosed in a feedback loop with the converter so the input noise and offset voltage of the second amplifier are added to the signal.

BANDWIDTH

Signal bandwidth requirements are an integral part of the current-to-voltage converter noise considerations for two reasons. Total output noise increases in proportion to the square root of system bandwidth simply because a broader noise spectrum is encompassed. Added is conflict between optimum signal-to-noise ratio and signal bandwidth. That optimum occurs for very high gain but high gain current-to-voltage converters are bandwidth limited far below the roll-off of the op amp. To the signal current, the amplifier feedback factor is unity which would normally make the full amplifier unity gain bandwidth available. Yet the very high-feedback resistances that produce the desired gain are shunted by stray

capacitances at much lower frequency. Just 0.5pF stray capacitance around a 100MΩ feedback resistor pulls signal bandwidth from megahertz level unity gain cross-overs down to 3.2kHz. To minimize the stray shunting, low capacitance resistors and assembly precautions are used. Mounting the feedback resistor on standoffs reduces capacitive coupling with printed circuit boards and such standoffs are normally Teflon™ insulated to reduce leakage currents. That mounting must be rigid to avoid introduction of noise through the microphonic effects of mechanical stress from vibrations.

There is an ultimate limit to the effects of such measures as capacitive coupling through the air around the resistor body always remains. Bandwidth beyond that imposed by such residual limits requires lower feedback resistance and accompanying lower converter gain. To restore gain, several options are available with a first shown in Figure 6a. A second amplifier with voltage gain is simply added following the current-to-voltage converter to retain the net input to output transimpedance for $R_T = A_V R_1$. Then, the high-value resistance is reduced by a factor equal to the voltage gain for a bandwidth increase by as much as the same factor.

While an obvious alternative, its overall effect on bandwidth and noise are not so immediate. Bounding the upper end of the bandwidth increase is the response limitation of the second amplifier. The bandwidth of the two op amp circuit for a net transimpedance of 100MΩ is plotted in Figure 6b as a function of the voltage gain involved in the overall conversion. Bandwidth initially increases linearly with the voltage gain as the reduction in R_1 diminishes the roll-off effect of stray capacitance. However, the added demands of the voltage gain on A_2 eventually make that amplifier's bandwidth the controlling factor. For a given set of conditions there is an optimum gain. A_V producing the peak bandwidths shown for the three example amplifiers. That peak occurs when the amplifier closed loop bandwidth equals the stray limited bandwidth of R_1. Variables affecting this peak are the net transimpedance R_T and the second op amp unity gain bandwidth f_C. Interrelating the controlling factors at the optimum bandwidth point is the expression defining the choice of R_1:

$$R_1 = \sqrt{R_T / 2\pi C_S f_C}$$

Bandwidth is extended to 100kHz from the original 3kHz using the wideband OPA404 for the second amplifier. That wideband op amp offers the best frequency response in Figure 6 and, although its total output noise result is greater, that is again largely due to the greater available bandwidth. If even greater bandwidth is required, either a faster op amp, with typically poorer noise performance, or lower transimpedance are the choices. Less bandwidth demands are encountered by A_1 with its unity feedback factor so an FET amplifier focused on low noise is used there like the OPA111 shown.

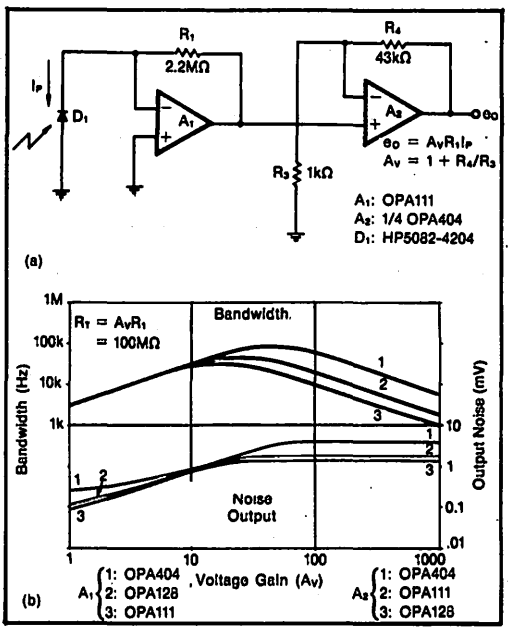


FIGURE 6. For greater bandwidth and the same net transimpedance, (a) voltage gain is added providing (b) bandwidth that increases faster than noise.

The price paid for improved bandwidth through voltage gain is increased output noise from that gain as well as from the presence of the added amplifier. While the lower value of R_1 does reduce its noise density, that effect is counteracted by the increase in bandwidth for a net zero change is resistor noise. That noise is now amplified by the voltage gain of the second amplifier causing an associated increase in output noise proportional to the voltage gain. Added to that is the noise from the op amps with the net result also shown in Figure 6b. Those noise curves are continuations of the ones presented in Figure 3 with the transition beginning at the 100MΩ level for the present example. In the lower gain ranges from one to ten, the noise is first determined largely by the op amps and their gain peaking but those effects give way to resistor noise dominance before the end of this range. Also in that range, the associated signal bandwidth plotted above is controlled by stray capacitance and shows a linear increase with increasing gain due to the corresponding decrease in resistance. Above the gain of ten and before 100, bandwidth begins to drop due to the encounter of A_2 limits. Simultaneous with this drop is a flattening of the output noise curve. Roll-off of the amplifier bandwidth and the simultaneous resistance drop nullify the effect of increasing voltage gain leaving output noise a constant. In the voltage gain range from 100 to 1000 these trends continue and degrade optimum performance since bandwidth is lost while noise remains constant.

While it is accepted that noise degrades with the voltage gain replacement of resistance, the overall circuit figure of merit gains. Including bandwidth in that measure shows that its improvement more than offsets the drop in signal-to-noise ratio. Mentioned before was the fact that the simple current-to-voltage converter suffers from greater bandwidth for the amplifier voltage noise than for the signal current. That discrepancy is removed with Figure 6 as the voltage gain increases and A_2 begins to filter out the higher frequencies. Evidence of this is in the noise curves that increase more gradually than the bandwidth curves in Figure 6b up to the optimum bandwidth point. At this optimum point, no bandwidth is afforded to noise that is not also available to signal. In effect, A_2 now also serves as the output active filter discussed earlier. While each of these curves is drawn for a specific 100MΩ transimpedance and the amplifiers and photodiode specified, similar optimums are considered for any design case.

For some of the more common photodiode applications a significant drawback of the above circuit is the need for two op amps per photodetector. Often hundreds of detectors are employed in a large arrays. As a compromise, one op amp can be made to provide the same transimpedance, still without the very large resistors, if some bandwidth and noise degradations can be accepted. A single op amp can both perform the current-to-voltage conversion and provide the subsequent voltage gain. With traditional techniques the task would be performed as in Figure 7a using R_2 for the conversion and R_3 and R_4 to set voltage gain. Current from D_1 flows in R_2 resulting in a signal voltage at the input of a noninverting amplifier. However, that signal voltage is also across the photodiode and this condition produces a nonlinear response as described before.

Instead, the diode is connected directly between the op amp inputs where zero diode voltage is maintained. Shown in Figure 7b, the resistors perform the same functions as in the last circuit but a linear response results. Current from the photodiode still flows in R_2 developing the same signal voltage. That current also flows into the feedback network but has little effect with the low resistances there. For the resistor values shown an equivalent transimpedance of 100MΩ results, just as with the two op amp example, but bandwidth improvement is less. At 20kHz, it is increased a factor of seven rather than a factor equal to the voltage gain as in Figure 6a. A new bandwidth limitation accounts for the difference and occurs due to the new placement of the high-value resistance. That resistor is now shunted by the common-mode input capacitance of the op amp instead of just the smaller stray capacitance. To maximize bandwidth, this new shunting effect is made to coincide with the amplifier roll-off through choice of R_2 and the voltage gain. A second benefit from this choice is that resistor noise beyond the signal bandwidth encounters a two pole roll-off.

Final output noise from the resistor has the expected increase over the basic circuit by the square root of the voltage gain. Added to that would have been a small

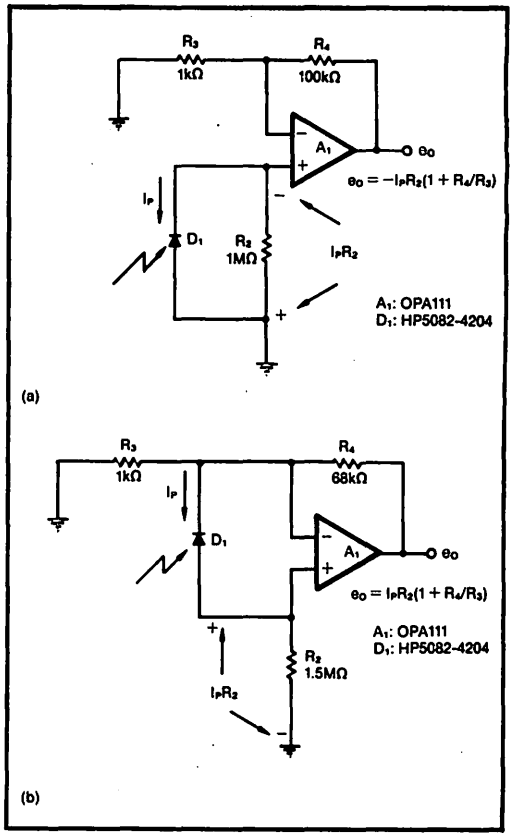


FIGURE 7. Combining current-to-voltage conversion and voltage gain using one op amp, (a) impresses unwanted voltage on the diode that (b) is removed by connecting the diode between the op amp inputs.

component due to the op amp as the normal source of gain peaking is removed. However, a new source is included in the circuit of Figure 7b, again due to the diode capacitance, as modeled in Figure 8a. Amplifier voltage noise e_n is impressed directly across that capacitance developing a noise current that is supplied to R_2. That creates a noise voltage at the input of the noninverting amplifier which is a multiple of e_n. The capacitive feedback network of C_D and C_{ICM} produces a noise gain that peaks at $1 + C_D/C_{ICM}$ and which exists in addition to the normal voltage gain of the noninverting amplifier.

Effects on frequency response are plotted in Figure 8b and they again produce a high-frequency peak in the noise gain. Its incidence is at much higher frequency than with the basic current-to-voltage converter because of the lower resistance involved and it is truncated earlier by the op amp roll-off. For the low capacitance diode used in both example circuits it now encompasses little area in the response plot corresponding to less noise effect. Larger diodes do not escape the effect, however, as represented by the dashed line for a capacitance around 200pF. Even still, the spectrum covered by the peaking is not the high end of the op amp bandwidth as

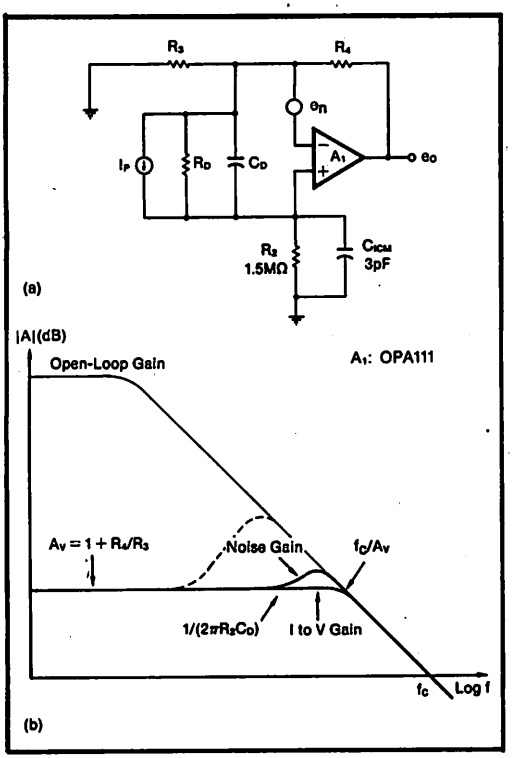


FIGURE 8. Photodiode capacitance (a) adds a positive feedback path to Figure 7b for (b) a new but lesser source of gain peaking.

it was for the basic circuit. Hence, op amp noise does not become the overriding source.

INTERFERENCE

Once diminishing returns impose a limit on reduction of the noise due to the circuit itself, consideration must be given to external noise sources. With its very high resistance a current-to-voltage converter is extremely sensitive to noise coupling from electrostatic, magnetic and radio frequency sources. Those sources require attention to shielding, grounding and component physical location[3] or they could otherwise become the dominant noise contributors. In each case, physical separation of the noise source from the sensitive circuitry is the most important step, but this becomes a compromise warranting other measures as well.

Electrostatic coupling, such as from the power line, supplies noise signals through the mutual capacitances that exist between any two objects. Voltage differences between the objects are impressed on those capacitances and any voltage variation couples a noise current from one to the other. To avoid that error signal, electrostatic shielding is used to intercept the coupled current and shunt it to ground. In this case, ground must be earth ground as that is the common reference for the separate objects. Such shields, however, create parasitic capacitances between the components shielded and the shields must also be returned to the signal common to avoid that coupling. Then shield carried capacitive currents from the output of a current-to-voltage converter are also shunted to ground and represent no bandwidth restriction to the feedback resistor. Even still, the shield produces a capacitance from the converter input to ground, possibly adding to gain peaking and its effect on total output noise.

As electrostatic coupling is most often of power line frequency and common to all points, it is a natural candidate for removal through the common-mode rejection of an op amp. At the line frequency, op amp CMR is very high but it is not utilized by the conventional current-to-voltage converter. This is a result of single-ended rather than differential input configurations, but that can be altered for improved noise rejection and DC error benefits as well. Op amp CMR is not a total replacement for shielding as electrostatic coupling will not perfectly common-mode to amplifier inputs. As a second defense, that rejection capability is most useful in removing the residual coupling that passes through shield imperfections.

The differential input capability of an op amp fits exactly with the signal from a photodiode. Since the diode signal is a current, it is available at both terminals of that sensor and can drive both amplifier inputs as in Figure 9a. Here, the diode current is no longer returned directly to common, but drives the amplifier noninverting input in that path. That creates a second signal voltage to double the circuit gain when $R_2 = R_1$ for compensation. For a given gain level, the resistor value need be only one-half the normal for a similar reduction in error sensitivity to amplifier input currents. This also removes DC voltage from the diode as it is now directly across the inputs of an op amp. With the voltage between those inputs being essentially zero, photodiode leakage current is avoided.

Aside from these benefits is the added improvement in the common-mode rejection of coupled noise. Electrostatic coupling to this current-to-voltage converter is modeled in Figure 9b along with the converter's parasitic capacitances. Zero signal is assumed there to illustrate only the electrostatic coupling effects. The electrostatic noise source, e_e, couples error currents i_e through mutual capacitances, C_M, to the circuit's two inputs. It might seem that the coupling effects would be different to the two points because feedback makes the R_1 input node a virtual zero impedance and the other node is high impedance. Yet, the noise coupling is via currents through capacitances that only depend on voltage signals on the capacitances. Both input nodes have the same voltage due to amplifier feedback, and thus receive the same level of noise current i_e. Those equal currents develop canceling e_{ne} noise voltage effects on the two circuit resistors for a zero final output singal.

Accuracy of the error cancellation is determined by three matching conditions involving the mutual capacitances, the resistors and the parasitic capacitancs shunting them. Matched mutual capacitances are best assured by locating

the resistors equidistant from any significant noise source not effectively blocked by a shield. Equal resistance values assure accurate cancellation of error signals until frequencies are reached where capacitive shunting imbalances net impedances. Shunting R_1 will be only about 0.5pF of stray capacitance but across R_2 is the much larger common-mode input capacitance of the op amp. For the 3pF of the OPA111 and the 50MΩ resistance shown, a pole occurs at about 1kHz, leaving the impedances of interest unbalanced. This shunting by C_{ICM} also imposes a signal bandwidth limitation at a lower frequency than normally encountered. The bandwidth of R_2 is rolled off earlier than that of R_1 creating a response with two plateaus separated by a factor of two in gain.

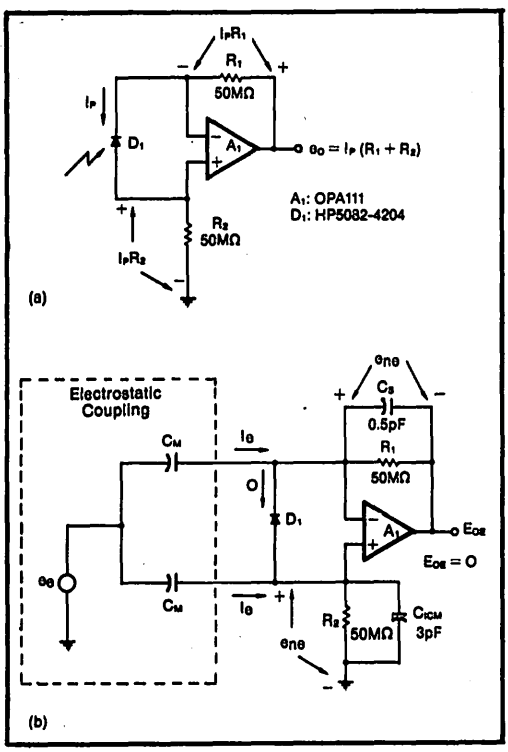


FIGURE 9. Exploiting the CMR capabilities of the op amp, (a) the differential inputs are driven giving (b) rejection of electrostatic coupling.

For the most comon electrostatic coupling at power line frequency, the above capacitive shunting has little effect. To better reject higher frequencies, capacitance can be added around R_1 to restore impedance matching, or signal swing on the common-mode input capacitance can be avoided. The latter option offers a more accurate solution and avoids the bandwidth limitation of C_{ICM} as well by using a second differential connection. Shown in Figure 10, the photodiode is connected between the inputs of two current-to-voltage converters whose outputs drive an INA105 difference amplifier. Again the diode current flows in two equal resistances that will receive equal electrostatic noise coupling. The diode current

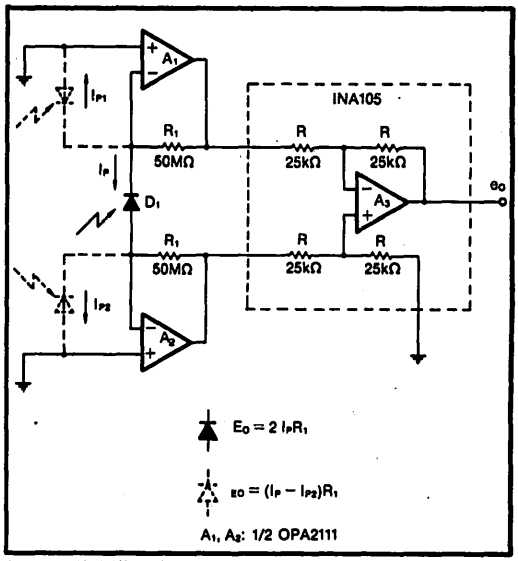


FIGURE 10. Differential inputs with wider band CMR and gain result with virtual grounds across amplifier common-mode input capacitances.

creates a differential output on the resistances but the noise coupling generates a common-mode signal. Supplied to the INA105, those signals are separated with the diode signal passed to the output and the noise rejected.

Retained with the new differential input circuit are the 2:1 lower individual resistance and a zero diode voltage. The latter is assured by the grounded noninverting inputs of both current-to-voltage converters which establishes zero voltage on both diode terminals. These connections also avoid signal swing on common-mode input capacitances for improved bandwidth in electrostatic suppresion and signal gain. Note that those noninverting inputs are not connected through high resistances for input current error correction. That is not necessary, as the input currents of A_1 and A_2 produce matching voltages at their amplifier outputs. Those voltages are a common-mode signal to the input of the INA105, so they too are rejected.

Another function available with the differential structure of Figure 10 is difference monitoring of two photodiodes. Instead of D_1, the two diodes shown in dashed lines are connected separately to the two input current-to-voltage converters. Their currents produce independent voltages at the outputs of A_1 and A_2 where they are processed by the difference amplifier to remove any common-mode portion. Left is an output proportional to the difference between the two input photocurrents as a measure of relative light intensity. A relative intensity measure is the type of signal used in position sensing or optical tracking control to direct feedback correction.

Magnetic coupling of noise can be more difficult to eliminate than the electrostatic, but its effects are also reduced by the differential input connections. Coupling is through mutual inductances in this case, so minimum

sensitive loop area is key to its control, along with shielding and maximum separation of source and receiver. Its effects are not removed by the electrostatic shield, so the first step is control of the source itself.[3] Power transformers that cannot be placed at a distance are internally shielded to largely terminate their magnetic fields at the transformer boundaries. Remaining magnetic coupling is addressed through physical and circuit configurations. High value resistors used in photodiode monitoring are sensitive to this coupling and connections must be kept short between those resistors and high impedance op amp inputs. Coupling effects that remain are made common-mode to be rejected by the op amp through loop size and distance matching. In Figure 9 and Figure 10, the high resistance is divided into two equal elements that are then physically mounted with the same orientation to and spacing from magnetic coupling sources. Noise coupled to the two resistors then causes equal signals that have cancelling effects at the circuit output.

With the third class of noise coupling, radio frequency interference, less can be removed by the amplifiers so shielding and filtering are the best defenses. Sources of RFI may be close to the photodiode monitor because of digital circuitry that is most likely co-resident in the system. Due to the high frequencies involved, op amps have little gain or common-mode rejection remaining for rejection of such signals. Because of this same amplifier limitation, and the basic voltage-to-current converter bandwidth restriction, desired signals will not exist in the radio frequency range. Filtering can then be used to largely remove the unwanted signal if applied in front of the op amp. Later filtering is less effective as the op amp can act like an RF detector separating a lower frequency envelope from a carrier.[4] Further reduction of that noise is achieved with an RF shield and a ground plane layer in printed circuit boards.

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SINGLE-SUPPLY OPERATION OF OPERATIONAL AMPLIFIERS

One of the most common applications questions on operational amplifiers concerns operation from a single supply voltage. "Can the model OPAxyz be operated from a single supply?" The answer is almost always yes. Operation of op amps from single supply voltages is useful when negative supply voltages are not available. Furthermore, certain applications using high voltage and high current op amps can derive important benefits from single supply operation.

Consider the basic op amp connection shown in Figure 1a. It is powered from a dual supply (also called a balanced or split supply). Note that there is no ground connection to the op amp. In fact, it could be said that the op amp doesn't know where ground potential is. Ground potential is somewhere between the positive and negative power supply voltages, but the op amp has no electrical connection to tell it exactly where.

The circuit shown is connected as a voltage follower, so the output voltage is equal to the input voltage. Of course, there are limits to the ability of the output to follow the input. As the input voltage swings positively, the output at some point near the positive power supply will be unable to follow the input. Similarly the negative output swing will be limited to somewhere close to $-V_S$. A typical op amp might allow output to swing within 2V of the power supply, making it possible to output −13V to +13V with ±15V supplies.

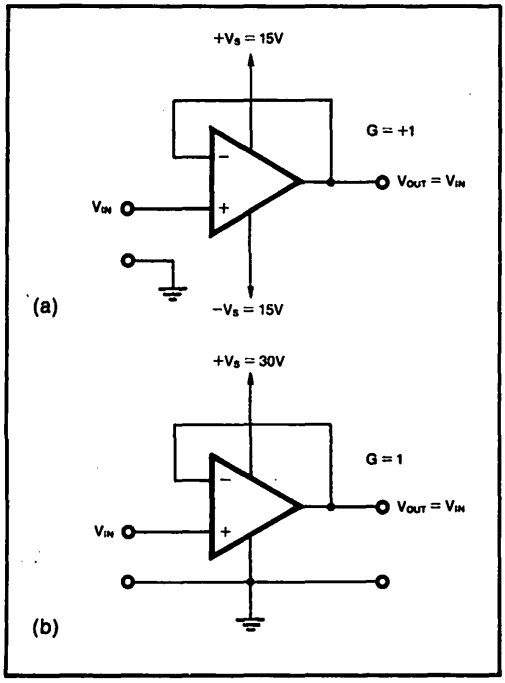


FIGURE 1. A simple unity-gain buffer connection of an op amp illustrates the similarity of split-supply operation (a) to single-supply operation in (b).

Figure 1b shows the same unity-gain follower operated from a single 30V power supply. The op amp still has a total of 30V across the power supply terminals, but in this case it comes from a single positive supply. Operation is otherwise unchanged. The output is capable of following the input as long as the input comes no closer than 2V from either supply terminal of the op amp. The usable range of the circuit shown would be from +2V to +28V.

Any op amp would be capable of this type of single-supply operation (with somewhat different swing limits). Why then are some op amps specifically touted for single supply applications?

Sometimes, the limit on output swing near ground (the "negative" power supply to the op amp) poses a significant limitation. Figure 1b shows an application where the input signal is referenced to ground. In this case, input signals of less than 2V will not be accurately handled by the op amp. A "single-supply op amp" would handle this particular application more successfully. There are, however, many ways to use a standard op amp in single-supply applications which may lead to better overall performance. The key to these applications is in understanding the limitations of op amps when handling voltages near their power supplies.

There are two possible causes for the inability of a standard op amp to function near ground in Figure 1b. They are (1) limited common-mode range and (2) output voltage swing capability.

These performance characteristics are easily visualized with the graphical representation shown in Figure 2. The range over which a given op amp properly functions is shown in relationship to the power supply voltage. The common-mode range, for instance, is sometimes shown plotted with respect to another parameter such as temperature. A ±15V supply is assumed in the preparation of this plot, but it is easy to imagine the negative supply as being ground.

In Figure 2a, notice that the op amp has a common-mode range of −13V to +13.5V. For voltages on the

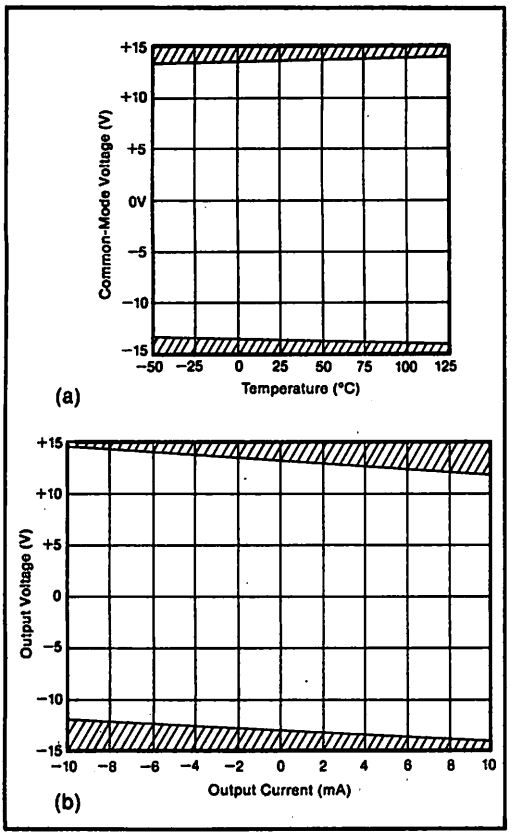


FIGURE 2. The common-mode range of an op amp is usually dependent on temperature. This behavior is shown plotted in (a). Output voltage swing will be affected by output current (b). Often the op amp load is connected to ground, so load current is always positive. Furthermore, as the output voltage approaches zero, load current approaches zero, increasing the available output swing. A split power supply voltage (normally ±15V) is assumed in preparation of these plots.

input terminals of the op amp of more negative than −13V or more positive than +13.5V, the differential input stage ceases to properly function.

Similarly, the output stage of the op amp will have limits on output swing close to the supply voltage. This will be load-dependent and perhaps temperature-dependent also. Figure 2b shows output swing ability of an op amp plotted with respect to load current. It shows an output swing capability of −13.8V to +12.8V for a 10kΩ load (aproximately ±1mA) at 25°C.

So the circuit of Figure 1b is limited to +13V output by output swing capability and −13V by negative common-mode range. A single-supply op amp is specifically designed to have a common-mode range which extends all the way to the negative supply (ground). Also, its output stage is usually designed to swing close to ground.

It would be convenient if all op amps were designed to have this capability, but significant compromises must be made to achieve these goals. Increased common-mode range, for instance, often comes at the sacrifice of performance characteristics such as offset voltage, offset drift, and noise. General purpose applications may tolerate op amp performance with these compromises, but high accuracy or other special purpose applications may require a different approach.

Fortunately, there are many ways to use high performance and special purpose op amps in single-supply applications. As demonstrated in Figure 1b, an op amp with typical common mode and output characteristics functions well on a single supply as long as the input and output voltages are constrained to the necessary limits. Circuit configurations must be used which operate within these limits.

Figure 3 shows a circuit, for instance, which references the input and output to a "floating ground" created with a zener diode. The zener diode is biased with a current set by R_1. Since V_{IN} and V_{OUT} are both referenced to the same floating ground, the zener voltage accuracy or stability is not critical. V_{IN} and V_{OUT} can now be bipolar signals (with respect to floating ground). With $+V = 30V$ and $V_Z = 15V$, operation is similar to standard split supply operation. The load current in this circuit, however, flows to the floating ground where it will add to the zener diode current (negative load currents subtract from zener current). The zener diode must be selected to handle this additional current. If the zener current is allowed to approach zero, the floating ground voltage will fall rapidly as the zener turns off. R_1 must be selected so that the zener diode current remains positive under all op amp load conditions.

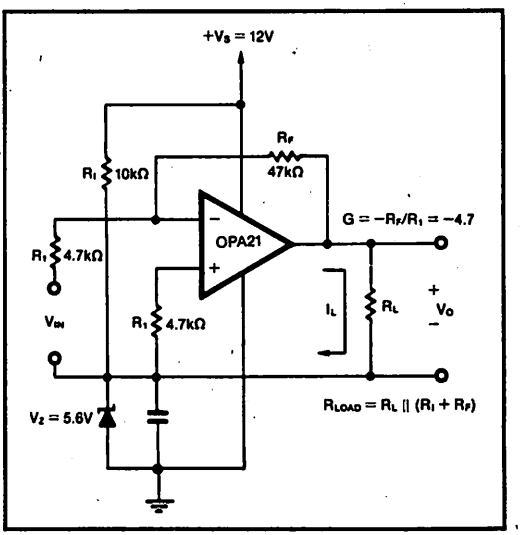


FIGURE 3. Bipolar signals can be handled when input and output are referenced to a floating ground. Changing load current causes a variation in zener current which must be evaluated.

Figure 4 shows operation in a noninverting gain configuration. In this circuit, the feedback components present an additional load to the op amp equal to the sum of the two resistors. This current must also be considered when planning for the variation in current flowing in the zener

diode. Again, the zener current should not be allowed to approach zero or exceed a safe value.

Notice that in this example, a single +12V supply is shown. Often, single-supply applications use supply voltages which are considerably less than the 30V total (±15V) at which the performance of most op amps is specified. While modern op amps generally perform well at less than their characterized voltage, this needs to be verified. Some op amps, although they are specified to operate at lower voltage, suffer degraded power supply and comon-mode rejection as their minimum operating voltage is approached.

Extremes of common-mode voltage on some amplifiers may produce unexpected behavior. Certain types of FET input op amps, for instance, exhibit much greater input bias current when the common-mode voltage relative to either of the power supplies exceeds 15V to 20V. This could occur with single-supply operation of 30V and common-mode voltage unbalanced nearer one supply or the other. The actual amplifier performance should be verified with the expected worst-case common-mode voltage conditions.

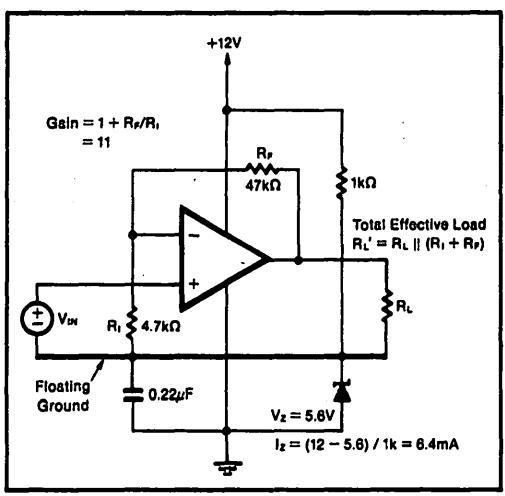


FIGURE 4. As with conventional split-supply operation, a noninverting gain configuration can be achieved. The feedback components create an additional load for the op amp which flows in the zener diode. Basic performance characteristics of the circuit are the same as for split supply operation.

Resistor voltage dividers are sometimes used to establish floating ground (Figure 5). The impedance of the ground is determined by the parallel combination of the divider resistors. Unless these resistors are made very low in value (consuming significant power supply current), this will lead to higher "ground" impedance. But with careful attention to the effects of varying load current in the reference point, this approach may prove useful. In fact, it may not be important in some applications that a truly "solid" ground be established since input and output are referenced to the same node. Good bypassing, however, will help avoid transient disturbances of V_O, or oscillation problems by providing a lower high frequency impedance without low value divider resistors.

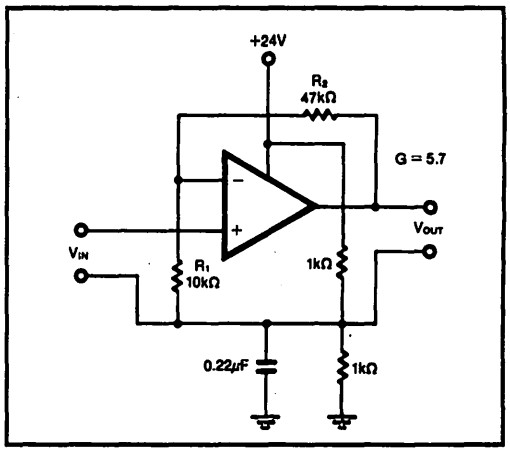


FIGURE 5. Even though the impedance of the voltage divider is in series with R_1 to ground, the gain of this noninverting circuit is determined solely by R_1 and R_2. Since the input and output are referenced to the same floating ground, its impedance does not affect the voltage gain of the circuit.

Appropriate voltage points often exist in related circuitry which can be useful in establishing a floating ground. In Figure 6, a +5V source used to power logic circuitry is used as a floating ground. Beware that most regulators used to supply these voltages are designed to source

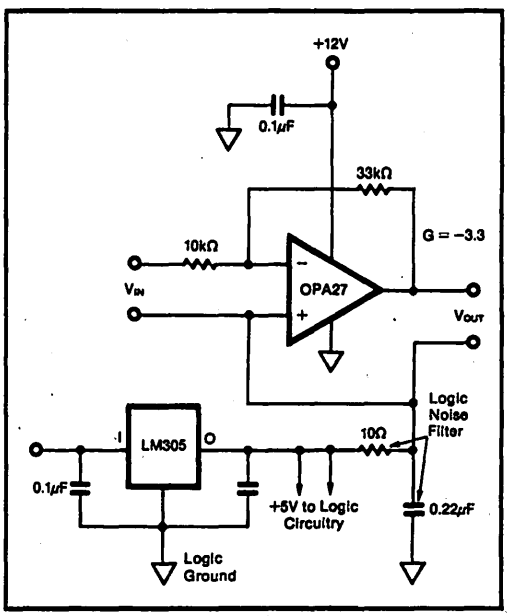


FIGURE 6. Many systems have a +5V logic supply or other appropriate voltage source which can be used as a floating reference potential for analog circuitry. Be sure logic noise does not enter the analog system by providing adequate decoupling network or additional bypassing.

current to a load only. If sufficient op amp load current flows into the 5V line, its voltage will rise. Again, load currents should be evaluated to assure that the floating ground voltage remains well defined. Normally other system components would sufficiently load the regulator to allow for plenty of op amp load current.

Particulary demanding applications may require that a buffer op amp be used to establish a very low impedance floating ground. Input to the buffer (Figure 7) could come from any of the previously discussed techniques. The buffer can both source and sink load current up to the output current limits of the op amp used as the buffer. The closed-loop output impedance of the op amp provides a very solid reference ground. Frequency response and open-loop output impedance characteristics of the buffer op amp will determine the high frequency floating ground impedance. Bypassing the output of the buffer amp may help lower the high frequency impedance, but don't exceed a safe capacitive load of the buffer amp or oscillations may result.

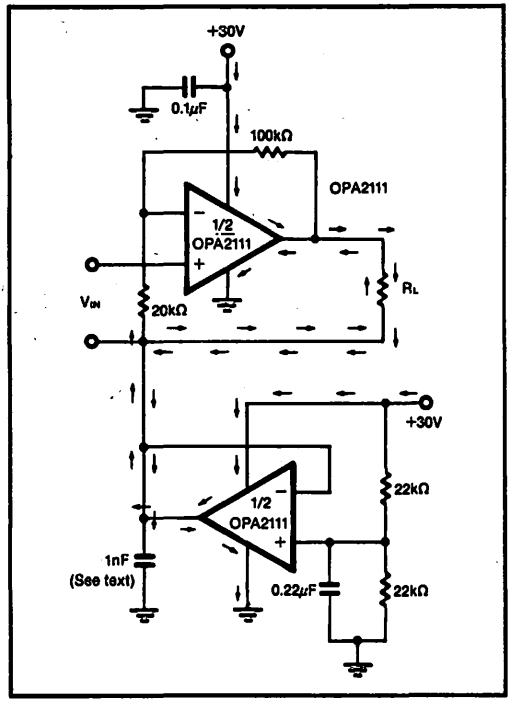


FIGURE 7. A very-low floating ground impedance is provided by using one section of the OPA2111 op amp connected as a unity-gain buffer. Input to the buffer is a voltage divider which can be heavily bypassed. The arrows indicate the direction of positive and negative load current flow.

Figure 8 shows a technique often used with high voltage and high current op amps. Here, an unbalanced power supply is used to produce the desired output voltage swing. In applications such as a programmable power source, the output voltage is required to go all the way to the ground. A small negative supply is used to provide the necessary common-mode voltage and output stage requirements to allow full output swing to ground. A much larger positive voltage supply can now be used to maximize the available output voltage.

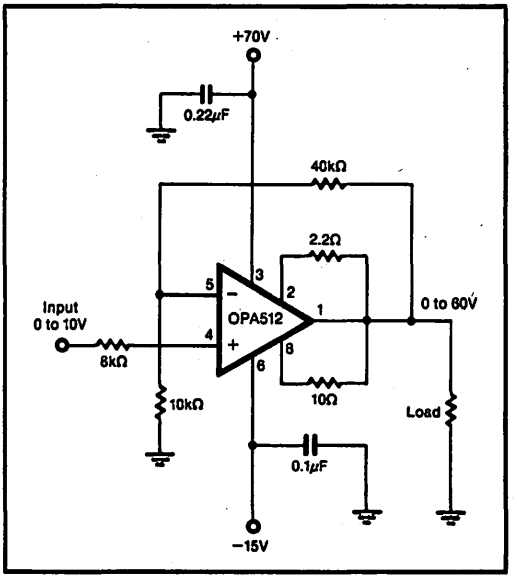


FIGURE 8. Unbalanced power supplies are often used with power op amps to achieve higher unipolar output voltage yet provide output swing down to 0V. The negative supply voltage in this OPA512 circuit is made large enough to provide the common mode voltage and output swing requirements of the application.

A higher current limit (lower value current limit resistor) is set for positive output current in this circuit since the primary purpose is to source current to a load connected to ground. Be sure to consider the safe operating area constraints carefully in this type of operation. Unequal supplies mean that larger voltages will be present across the conducting output transistor, thus requiring greater safe operating area. See *Understanding Power Amplifier Specifications,* page 214, for information on evaluation of safe operating area.

Other signal processing circuits which are normally powered from a split supply can be operated from a single supply as well. These include such devices as instrumentation amplifiers, current transmitters, analog multipliers, log amps, etc. The principles in assuring proper operation are the same as for op amps.

The INA105 difference amplifier provides an instructive example. This device is comprised internally (Figure 9) of a precision op amp and four precision matched resistors. In a majority of applications pin 1 is connected to ground. This is the output voltage reference pin. If pin 1 is referenced to a floating ground using one of the previously described techniques, operation is similar to split-supply operation. Unlike the op amp applications previously described, however, the differential input terminals (pins 2 and 3) will be capable of accommodating common-mode voltages equal to and even

greater than the supply voltages. Voltages applied to the input resistors are divided down, maintaining common-mode voltages to the op amp within operating limits. In this case, the voltage at pin 1 in conjunction with the required output swing determines the technique required for single-supply operation.

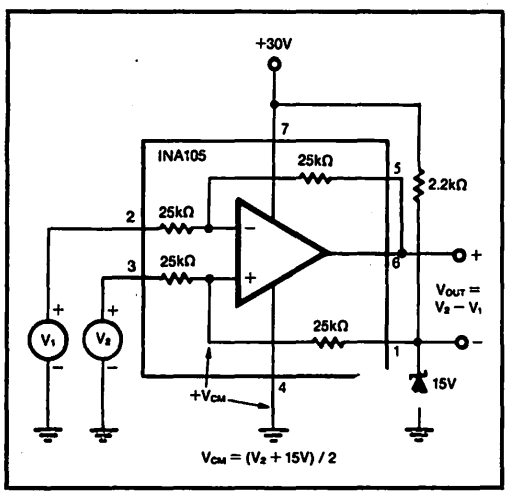


FIGURE 9. The input voltage to this simple difference amplifier is divided down by the input resistors before being applied to the op amp. Thus it is able to handle voltages which are equal to or greater than the power supply voltage.

True instrumentation amplifiers (Figure 10) usually have an op amp at their input. Therefore, common-mode range of the input op amp again becomes a concern. Input voltages must be confined to within the specified common-mode range of the device. The output section of the instrument amp is like the difference amplifier and output voltage swing requirements will dictate the techniques required.

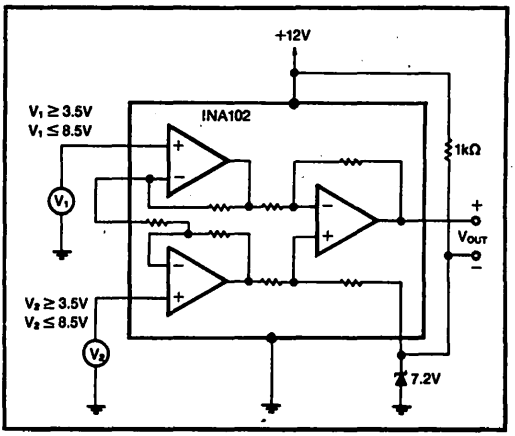


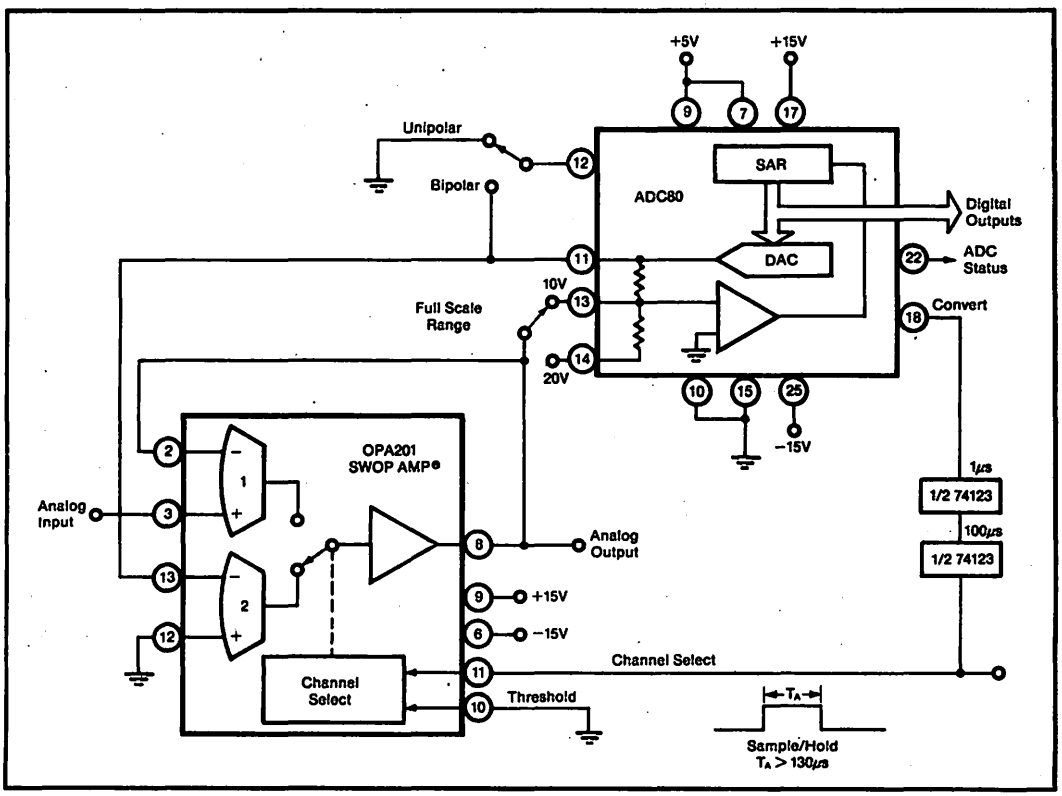
FIGURE 10. Inputs to the instrumentation amplifier are applied directly to the active circuitry of the input op amps and therefore are subject to the common-mode range limitations of these op amps.

SWOP AMP®, ANALOG-TO-DIGITAL CONVERTER MAKE ZERO-DROOP SAMPLE/HOLD

Using a switchable-input op amp (SWOP AMP), a 12-bit A/D converter and two one-shot multivibrators, you can configure a sample/hold amplifier (see circuit diagram) that holds a desired analog sample indefinitely with no droop. Previously, other circuits accomplished this function by using relays in conjunction with the A/D converter. The switchable-input op amp does the same job faster and more reliably.

The high sample command switches the OPA201's input to op amp #1 and triggers a convert command to the A/D converter. The multivibrator delays the sample pulse 100μs before presenting a 1μs-wide convert command to the A/D converter. This delay allows adequate time for large-signal settling in the OPA201; the A/D converter needs an additional 25μs to convert. You can reduce the analog-to-digital conversion time by using a faster A/D converter; ADC84 and ADC85 types, for example, need only 10μs.

SWOP AMP® Burr-Brown Corp.



THE SWOP AMP

A Low Power Op Amp with Multiplexed Inputs

Designing a switching function into a precision analog circuit without compromising accuracy, reliability, or cost can be difficult. Relays offer high accuracy, but are expensive and have limited lifetime compared to semiconductors. FET switches and multiplexers have ON resistance and OFF leakage currents which require detailed attention to impedance levels, especially at high operating temperatures. A new integrated circuit device called a SWOP AMP (SWitchable input OP AMP) combines precision and versatility to provide a nearly ideal switching function in many applications.

WHAT IS A SWOP AMP?

The SWOP AMP (Burr-Brown OPA201) is a precision operational amplifier with two matched input stages and channel select circuitry (see Figure 1). A digital channel-select signal enables one input stage by turning off the bias current in the unselected input stage. Thus only the ON channel can send signals to the following stages. The channel-select circuitry is compatible with a variety of logic families. The applications as shown are for ground-referenced TTL channel-select signals. Actual logic levels used may be referenced to ground, $-V_{CC}$, or virtually any other point by connecting the threshold control pin to the appropriate voltage. See "Inside The OPA201 SWOP AMP" for more information about internal operation and channel selection.

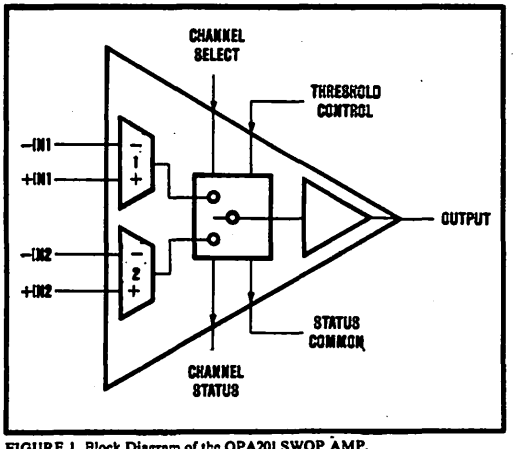


FIGURE 1. Block Diagram of the OPA201 SWOP AMP.

The SWOP AMP is a low power device, typically drawing only 350μA of supply current. The power supply may be either single or split, with a range of 5V to 36V. The wide power supply range and low power, combined with precision performance, makes the SWOP AMP ideal for portable or remote battery powered systems. Isolated systems and robotics are other areas that can benefit from this low cost, small-size analog signal conditioning and steering device.

The key electrical specifications are shown Table I.

INSIDE THE SWOP AMP

A simplified schematic of the OPA201 SWOP AMP is shown in Figure 2. The circuit has four sections: (A) input stage 1, (B) input stage 2, (C) active load and output amplifier, and (D) channel-select circuit. The two

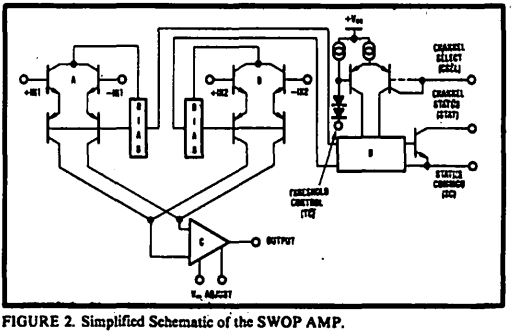


FIGURE 2. Simplified Schematic of the SWOP AMP.

precision differential input stages are identical, with offset and drift laser-trimmed for very-tight matching. The input stages share a balanced, high precision active load and external offset adjust pins, so external offset adjust affects both channels. (Figure 3 shows how an inexpensive CMOS IC may be used to alternately connect one of two independent offset adjust potentiometers.) The input stages also share a gain stage and output amplifier, so the characteristics of the two channels are very nearly identical.

Under control of the channel-select circuitry, only one input stage at a time is active. The selected input stage controls the output amplifier, while the unselected input stage is turned off by deactivating its bias circuitry. With no current in the unselected stage, it has negligible input bias current, and the OFF channel cannot send signals to the output amplifier. Rejection of the signal applied to

TABLE I. OPA201CG SWOP AMP Key Specifications.
At $T = +25°C$, $\pm V_{CC} = 15VDC$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}			35	100	μV
V_{OS} drift	−25°C to +85°C		0.5	1.0	μV/°C
dV_{OS} (match)	$V_{OS1} - V_{OS2}$		25	50	μV
dV_{OS} drift	−25°C to +85°C			1.0	μV/°C
I_b				25	nA
I_{os}				1	nA
Slew Rate			0.2		V/μsec
PSRR		100			dB
CMRR		95			dB
A_{ol}	R1 = 10kΩ, $V_o = \pm 10V$	120	130		dB
Crosstalk	V_{in} "off" = ±12V	120	130		dB

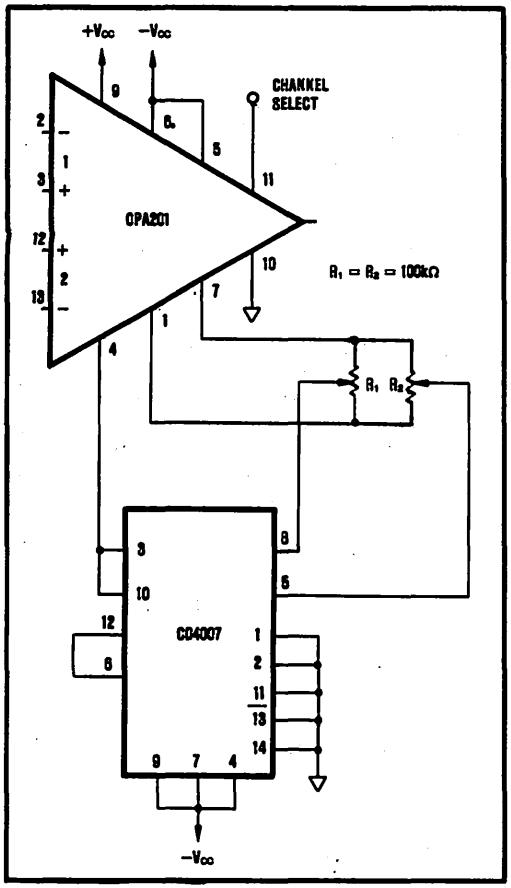


FIGURE 3. Dual Independent Offset Adjust Using a CD4007 to Switch in the Potentiometers. (R1 adjusts only channel 1, R2 adjusts only channel 2.).

the OFF channel's input is outstanding, as shown by the −120dB crosstalk specification. Thus the complete circuit functions as a high precision operational amplifier which can switch between two sets of inputs under control of a one-bit logic signal.

The OFF channel may be modeled as an open circuit in most designs. Input currents are typically under 15pA for input voltages inside the common-mode range. Although crosstalk is specified for voltages equal to the common mode extremes, the same OFF channel rejection characteristics are typically observed for all input voltages between $-V_{CC}$ and $(+V_{CC} - 1V)$.

The channel-select circuitry is versatile yet simple. The trip point for changing channels is set by the threshold control, pin 10. Channel 1 is selected when the channel-select voltage is more than two diode drops above the threshold control voltage, and channel 2 is selected when the channel-select is less than two diode drops above the threshold control voltage. Thus the channel-select voltages are compatible with ground-referenced TTL levels when the threshold control pin is grounded. Connecting the threshold control pin to the $-V_{CC}$ pin is especially useful when low supply voltages are used. For example, a single +5V supply can be used to provide the power for both the SWOP AMP and channel-select controller as well. An open circuit on the channel-select pin will also select channel 1. This allows an open-collector transistor (or phototransistor) to control the channel select without a pull-up resistor. When there is no pull-up resistor, the leakage must be limited to 20μA to ensure that channel 1 is indeed selected (20μA must be sunk to pull the channel-select pin low).

The channel status open-collector output is referenced to the status common pin. When used with a pull-up resistor, it provides a signal that is the logic inverse of the channel-select signal. This comes in handy for such tasks as switching in the dual external offset adjust potentiometers, polarity indicaton in absolute value circuits, and for level-shifting the logic signal. When not used, the channel status is left open and status common is tied to $-V_{CC}$.

APPLICATIONS

Selectable Input Amplifiers

Perhaps the most obvious need for the SWOP AMP is where selectable inputs are required for a system. The simplest circuit of this type is the selectable input buffer shown in Figure 4. Both channels are configured as high input impedance voltage followers. No external parts are required. This circuit is useful for remote or computer-controlled systems where fairly high level signals need to be selected and buffered. For voltage signals, this circuit functions as a near-ideal switch with high input imped-

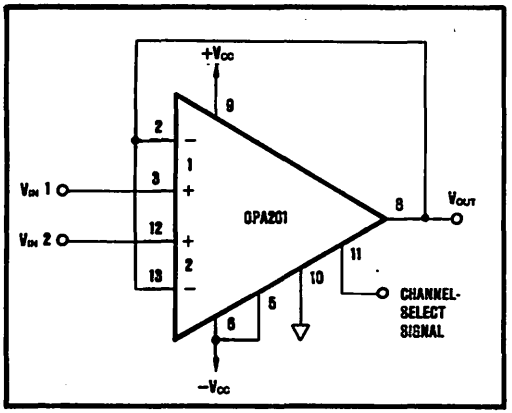


FIGURE 4. Selectable Input Buffer.

ance and low output impedance. The high open-loop gain and CMRR guarantee excellent accuracy and linearity.

The SWOP AMP also provides a minimum-parts approach to amplification of low level signals. Each channel may be configured to provide noninverting or inverting gain using standard op amp design considerations. If the same noninverting gain is desired for both channels, a single set of feedback resistors may be shared and the inverting inputs for each channel tied together as shown in Figure 5a. Different gains may be set with independent feedback networks, or by using only three resistors as shown in Figure 5b. When each channel has independent feedback, the OFF channel's feedback is treated as a component of the load impedance for design purposes.

For dual input inverting amplifiers, independent feedback networks are used. Since the common-mode voltage is always near zero, the input voltages may exceed the supply voltages. This allows a system with low supply voltage to monitor high voltages by using gains less than unity. Figure 5c shows a circuit with gains of −10 and −0.1. Note than V_{in2} will produce ±10V outputs for 100V inputs. The low input bias currents (25nA max) and input offset current (1nA max) make it easy to pick impedances high enough to limit the maximum output current requirement without introducing excessive errors.

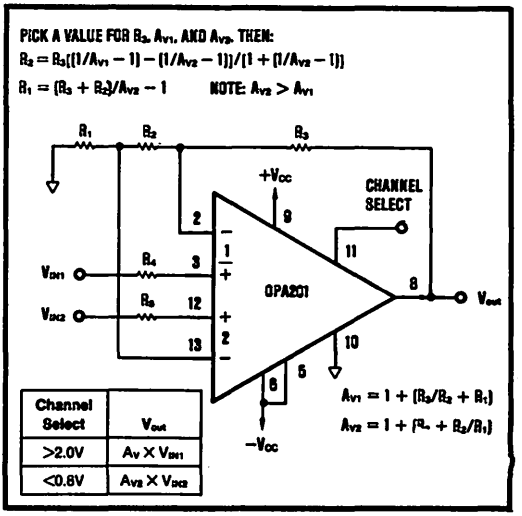


FIGURE 5b. Selectable Input Noninverting Amplifier with Different Gains for Each Channel.

Auto-Zero, Auto-Cal, System Check

The selectable input technique provides a straightforward way to perform software auto-zero of system offset

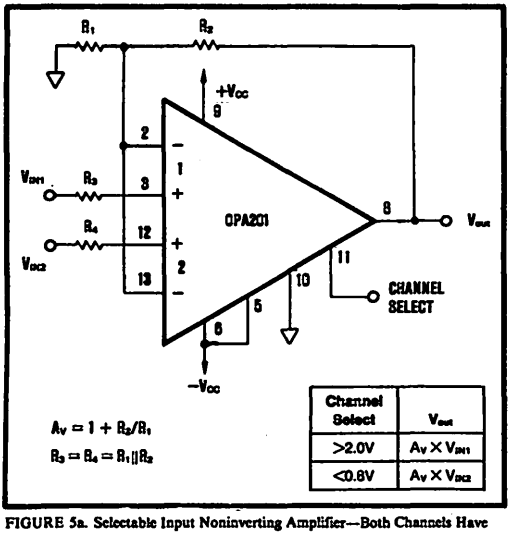


FIGURE 5a. Selectable Input Noninverting Amplifier—Both Channels Have the Same Gain.

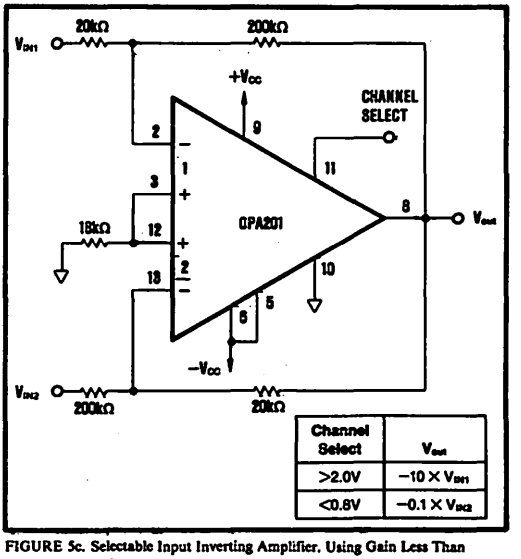


FIGURE 5c. Selectable Input Inverting Amplifier, Using Gain Less Than Unity Allows Inputs to Exceed Supply Voltage.

errors; one channel processes signals, and the other channel has the input grounded (both channels have the same gain). Figure 6 shows the SWOP AMP used to software auto-zero the offset error of a 3656 isolation amplifier. The 3656 provides both signal isolation and isolated power for the SWOP AMP. The gain for the SWOP AMP should be such that the 3656 input voltage is limited to ±5V. A gain of 2 may be provided by the output section of the 3656 to raise the output swing to ±10V if desired. A 4N25 optocoupler isolates the channel select or zero command signal. When the zero-input channel is selected,

$$V_{out} = V_{iso} + (A_V \times V_{OS2})$$

where V_{iso} = iso amp V_{OS},

A_V = SWOP AMP voltage gain = 1 + (R2/R1),

V_{OS2} = SWOP AMP V_{OS} for Ch. 2.

When the signal channel is selected,

$$V_{out} = V_{iso} + (A_V \times V_{OS1})$$

where V_{OS1} = SWOP AMP V_{OS} for Ch. 1.

Subtracting the zero-input V_{out} from the signal V_{out} with software leaves a corrected output voltage

$$V_{out} = (A_V \times V_{in}) + A_V \times (V_{OS1} - V_{OS2})$$
$$= A_V \times (V_{in} + dV_{OS})$$

where dV_{OS} = V_{OS} between the two channels of the SWOP AMP

$= 50\mu V$ max

Notice that the offset of the iso amp (typically 5mV + 200μV/°C) has been removed from V_{out}, and the only offset error is the mismatch between the two input stages in the SWOP AMP (50μV + 1μV/°C max).

Using a signal instead of ground on channel 2's input opens the door to a wide range of system calibration and signal check applications. A reference may be selected for gain calibration, or a specific waveform of some type may be switched in at the front end of a system to verify that the system is functioning properly.

Using a SWOP AMP with a system clock to drive the channel-select pin and switching continuously between a signal input on one channel and grounded input on the other provides a single-chip chopper-modulator system for amplitude modulation. Variations on this idea include synchronous demodulation and quadrature detection systems that have low parts count and high performance.

Selectable Transfer Functions

Start with a selectable-input amplifier with different gains for each channel. Now connect the inputs together and you have a selectable-gain amplifier, extremely useful for extending the dynamic range and resolution of a system. The SWOP AMP allows construction of an amplifier with true precision performance and two gains selected by remote control using only one low cost integrated circuit and a few resistors (Figure 7). In this configuration, the channel-select pin serves a gain select function.

Selectable transfer functions extend beyond selectable gain, with selectable bandwidth being one of the most useful. Smoothing (low pass) or AC coupling (high pass) characteristics may be switched in by a remote controller without the added cost and lower reliability of relays of

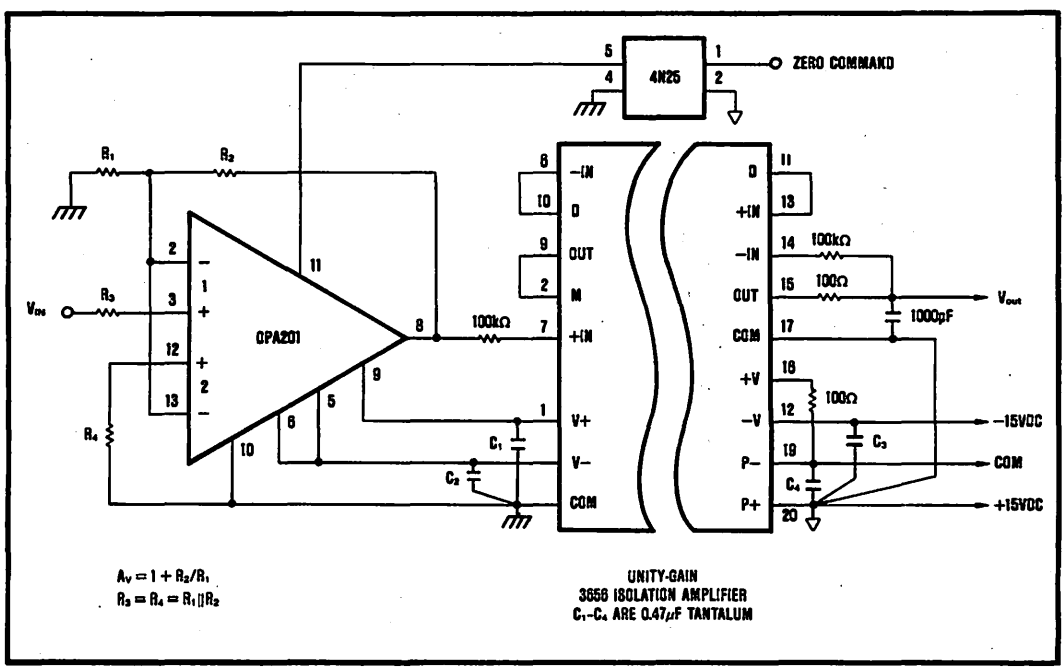
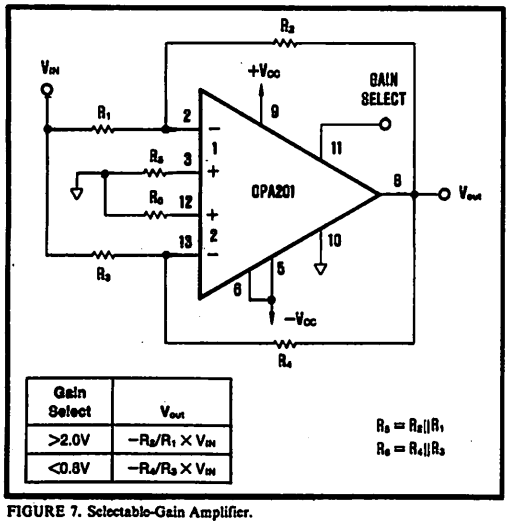


FIGURE 6. Software Auto-Zeroing the 3656 Isolation Amplifier.



Gain Select	V_{out}
>2.0V	$-R_6/R_1 \times V_{IN}$
<0.8V	$-R_6/R_3 \times V_{IN}$

FIGURE 7. Selectable-Gain Amplifier.

FET switches. The whole range of signal conditioning circuits using op amps such as summers, compressors, integrators, and clamping circuits may be switched in remotely using this approach.

Differential Input Circuits

Many applications requiring remote sensing of analog signals are subject to AC pickup and ground loops, and require differential input circuits which can reject common-mode errors and noise. The high gain and CMRR of the SWOP AMP make it ideal for differential-mode circuits. Most of the techniques mentioned so far can be applied in the form of differential amplifiers, with excellent rejection of 50Hz and 60Hz noise. Figure 8 shows a dual-channel low power differential amplifier.

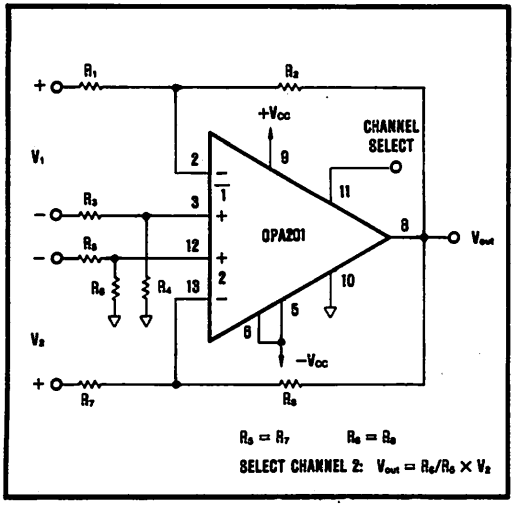


FIGURE 8. Dual-Channel Differential Input Amplifier.

If higher input impedance is required, two SWOP AMPS and a precision op amp can be used to realize a switchable version of the classic three op amp instrumentation amplifier. When the op amp is a low power precision device such as the OPA21, the result is an instrumentation amplifier with dual input, auto-zero, or selectable-gain features, yet requiring only about 1mA of supply current. This hard-to-beat combination of performance, features, and power requirements is shown in Figure 9.

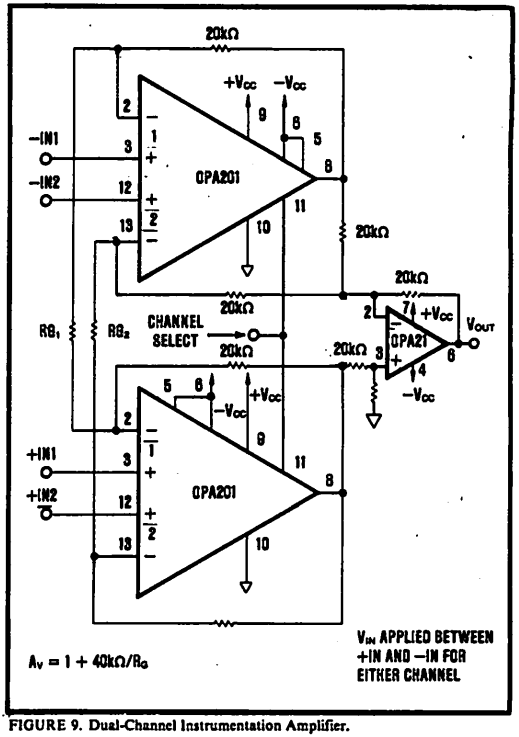


FIGURE 9. Dual-Channel Instrumentation Amplifier.

A Unique Low-Power Sample/Hold, Too

The SWOP AMP can also function as a low power sample-and-hold amplifier, which draws only 10% of the supply current of most sample/holds. This function is especially important where remote A/D conversion is required. As shown in Figure 10, the only external components required are two signal diodes and two capacitors. Gain resistors could be added to one or both channels for gains other than unity. The SAMPLE/HOLD mode control signal is applied to the channel-select pin.

When the channel-select input is high, selecting channel 1, the circuit is in SAMPLE mode. C2 is charged through the diodes until the voltage on C2 equals the input voltage. There is a small offset (about 100mV, due to the diodes) between the output of the circuit and the C2 voltage while in the SAMPLE mode. This doesn't introduce an error when the circuit is used to hold the input for an A/D converter, since the error in HOLD mode is less than 1mV and adjustable to zero. C1 pro-

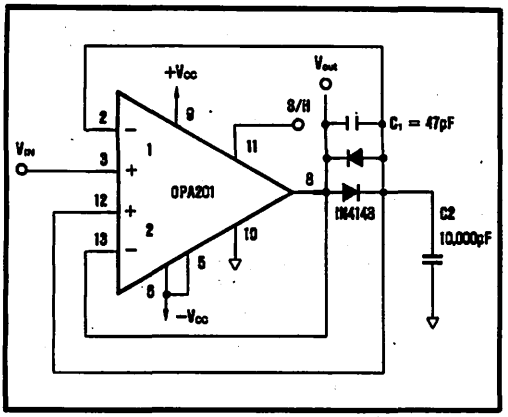


FIGURE 10. Low Power Sample/Hold Amplifier.

vides direct high frequency feedback around the diodes to reduce ringing in the SAMPLE mode.

HOLD mode is selected by taking the channel-select signal low. Now the voltage on C2 (identical to the input voltage when HOLD mode was selected) provides the input voltage to channel 2. Feedback to channel 2 forces the output of the circuit to be equal to the input voltage present when HOLD mode was initiated. The back-to-back diodes now have less than 100μV across them and disconnect the channel 1 feedback path.

Droop is determined by the input bias current and C2, and is less than 2.5mV/msec for C2 = 10,000pF. This means droop is less than 0.1LSB for a 12-bit, 10V full-scale ADC after holding for 100μsec. Acquisition time is limited by slew rate to about 50μsec for a 10V step. Unadjusted zero-scale error is typically under 1mV, and may be adjusted to zero using the offset control and one potentiometer. Simply adjust the offset of the HOLD mode to zero while the input is grounded, with the mode control signal constantly changing between high and low. This procedure nulls both offset voltage and charge transfer offset. Aperture time for the circuit is the time required to switch channels and slew about 100mV to the correct output voltage, about 7μsec total.

UNDERSTANDING POWER AMPLIFIER SPECIFICATIONS

Many of the specifications for a power amplifier are similar to those of a signal amplifier. The key ones describing the power handling ability, however, are less frequently encountered and are often a source of confusion. The purpose of this note is to explain the power handling limits of a power amplifier and to show how to interpret the specifications of these limits.

The power handling limitations are most often due to the limits of the power output transistors. So, to understand these limits, let's focus on an individual output transistor within an amplifier. Figure 1 shows a representative power amplifier with output transistors Q1 and Q2. Q3 and Q4 are current limit transistors which turn on when the voltage drop across their respective sense resistors, R1 and R2, is approximately 0.65 volts. I_{out} is shown flowing out of the amplifier, so Q1 is the "on" device—Q2 is "off" and can be ignored for now.

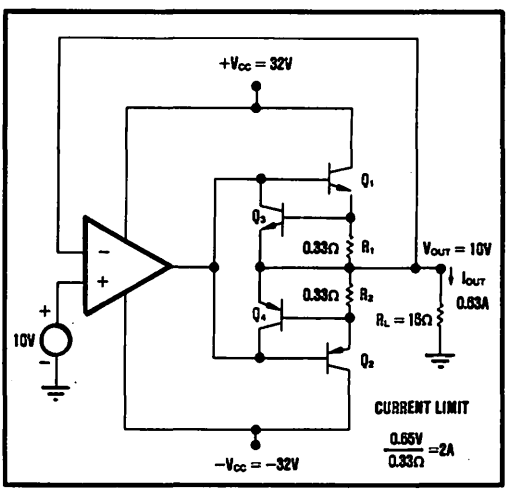


FIGURE 1. This simplified schematic is representative of a wide variety of possible power amplifier circuits.

In evaluating the stress on the amplifier under this condition, the current through and the voltage across the conducting power transistor must be considered. The output transistor current is simply equal to I_{out}. The voltage across Q1, (V_{CE}), however, is not V_{out} but rather $+V_{CC} - V_{out}$. The operating point of the conducting output transistor is usually plotted on a voltage-current plot as shown in Figure 2. In this example, the operating point is $I_{out} = 0.63A$ and $V_{CE} = (32-10) = 22V$ and is shown at point "A" on the voltage-current plot. The voltage drop across R_1 is ignored in the calculation of V_{CE} since it is small compared to the other voltages.

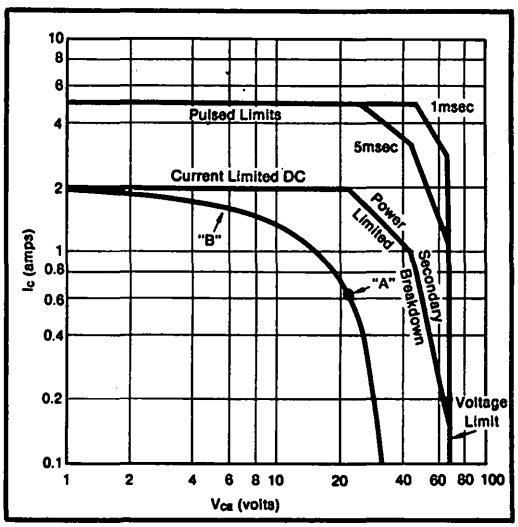


FIGURE 2. The Safe Operating Area for the Burr-Brown 3573 is shown, plotting the limits for collector current (I_C) versus the collector-emitter voltage (V_{CE}) of the conducting transistor.

SAFE OPERATING AREA

The operating limits of Q1 are designated by the boundary line on Figure 2 and the area below this line is called the Safe Operating Area (SOA). In this case, the operating point clearly falls within the SOA of the output transistor.

Note that the limit line is divided into different regions. The current limited region is usually due to bonding wire or hybrid interconnection limitations. Above the amplifier's rated current, internal interconnection wires to the power transistors, power supplies or amplifier output may burn out like a fuse.

As the voltage across the conducting transistor (V_{CE}) increases, the internal power dissipation increases until the power limit of the amplifier is reached. At this point, any increase in V_{CE} must be accompanied by a corresponding decrease in current to maintain constant power dissipation. Note that all points on the power limit line have a constant dissipation (45W in this example). This dissipation limit is due to the thermal resistance of the

power transistor, its attachment, and packaging components. With a case temperature of +25°C, the maximum power dissipation will cause the output transistor to heat to its maximum allowable temperature. Operation at higher case temperatures is possible but the maximum power must be derated (more on this later).

As the constant dissipation line is followed to higher V_{CE}, the secondary breakdown region is entered. At high V_{CE}, current crowding can occur in the emitter structure of the power transistor (Figure 3) leading to isolated hot spots. As a result, the allowable power dissipation must be reduced as V_{CE} increases further. This causes the change in slope of the SOA limit line. It is this power amplifier limitation that is most frequently misunderstood since the safe operating current may be surprisingly low at high V_{CE}. Note that the "5A" power transistor specified by Figure 2 can handle only 0.6A at V_{CE} = 50 volts.

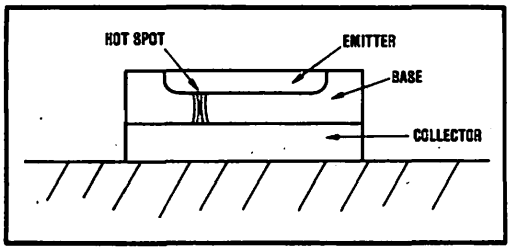


FIGURE 3. At high V_{CE} and I_C, localized hot spots may cause a localized burn-out producing a collector-emitter short—the ultimate result of secondary breakdown.

As shown in Figure 2, under pulsed conditions, larger current or V_{CE} can be handled. This peak capability may apply only to certain regions of the voltage-current curve, so attention must be paid to the exact details of a given situation.

The final limit is the breakdown voltage of the power transistors (or other amplifier circuitry). This breakdown voltage limit cannot be exceeded under any condition. In a power amplifier, the maximum voltage rating is the sum of the positive and negative power supplies (ignoring the signs).

An important conclusion must be drawn from these points: it is the voltage across the conducting transistor, not the amplifier output voltage, which determines the operating point. For instance, it is often desirable to design for safe operation during a short-circuit to ground (Figure 4). Even though the output voltage is zero, the V_{CE} of the conducting transistor is equal to the full power supply voltage, $+V_{CC}$. The current limit, as determined by the choice of R_1 and R_2, must then be set to a value far less than the full rated amplifier current. Alternatively, the power supply voltages could be lowered, allowing safe currents as high as the full rated current to be used.

Example 1:

For the amplifier described by Figure 2, what is the maximum power supply voltage allowing for continuous short circuit to ground? The current limit is set to the maximum continuous 2A rating. Answer: V_{CC} = ±22.5V. If short circuit to either supply must be tolerated, V_{CC} = ±11.25V would be the maximum since the total of both the negative and positive supply would be across the conducting transistor.

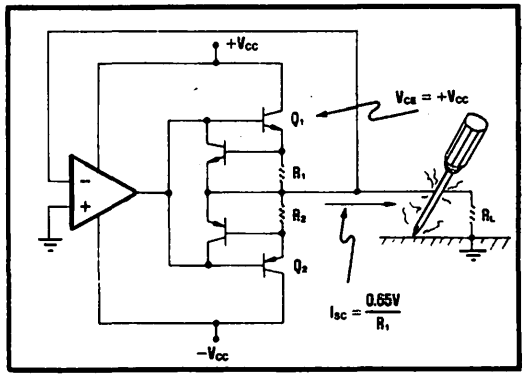


FIGURE 4. Even with no input voltage, a shorted output will cause high currents to flow. The offset voltage of the amplifier provides the "input," driving the output to the current limit set for the device. The current limit must be set low enough to withstand the high V_{CE} in this condition.

TWO TYPES OF SOA PLOTS

The SOA plot shown in Figure 2 is typical of the way power transistor manufacturers specify their devices. They plot I_C versus the V_{CE} voltage for the transistor. Power amplifier specifications, however, sometimes show a safe area curve plotted according to the amplifier output voltage. Since the V_{CE} (the voltage that matters) is determined by the output voltage and the power supply voltage, this type of curve applies only for the stated supply conditions. Each type of presentation has advantages. The second method is sometimes easier to interpret and can convey any differences between positive and negative SOA capability. However, its data is valid only at the stated power supply voltage. The I_C versus V_{CE} plots (Figure 2) are more easily scaled to varying power supply situations and promote a better understanding of the principles involved.

The two types of curves may be compared here. Figure 2 and Figure 5 are for the 3573 power amplifier (used as an example in this note). Differences between the positive and negative SOA are not shown; the lower of the two limits is depicted in Figure 2.

RESISTIVE LOADS

It is often assumed that a circuit designed for safe operation at maximum output voltages or current will be safe under all conditions, but this is not always the case. All conditions of output voltage should be considered, but two situations in particular normally represent the worst case—the maximum load current and the maximum power dissipation.

The worst-case conditions can be found by plotting a load line on the SOA plot. The load line "B" in Figure 2 is for V_{CC} = ±32V and a load resistance of 16Ω. When plotted on the logarithmic scales of an SOA plot, resistive load lines are curved. By finding a few points on the curve (as was done with point "A"), its general shape

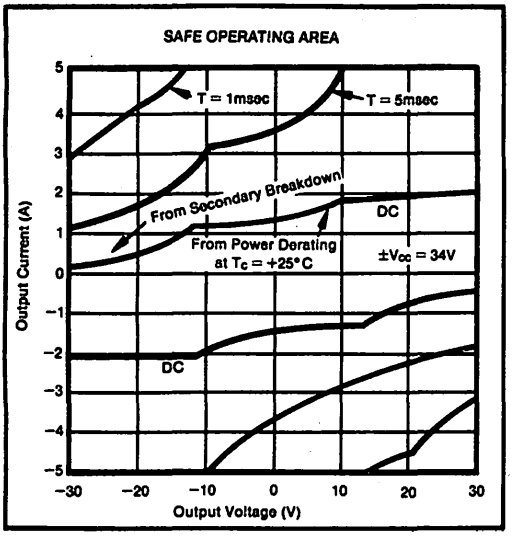


FIGURE 5. The SOA of the Burr-Brown 3573 is shown here plotted according to output voltage. This way of specifying SOA is easy to interpret if the rated power supply voltage is the same as the application in question.

can be found. Then it is easy to spot any SOA violations.

For resistive loads, the maximum current occurs at the maximum output voltage and is usually assumed to be V_{CC}/R load. This presumes that the output voltage can be as great as the power supply voltage. The load resistance must not be made so low that excessive output current will flow. Alternatively, the current limit could be set to a safe value; however this can limit the output voltage swing.

The maximum power dissipation occurs at a V_{out} of $+V_{CC}/2$ or $-V_{CC}/2$. Figure 6 shows how the dissipation changes with V_{out} (V_{out} is shown as a ratio of the power supply voltage). The dissipation is zero for zero output voltage and current and is also zero at maximum output voltage and current (where V_{CE} is zero at amplifier clipping). Of course, this second case is not fully achievable since some voltage is dropped across the transistor at maximum output voltage.

Example 2:

Often it is desirable to apply an unbalanced power supply voltage to a power amplifier. For instance if a 0-50V output is desired, a large negative supply voltage is neither needed nor desired. V_{CC} = +55V and −5V is chosen to allow the necessary voltage swing without exceeding the power supply limits (total of $+V_{CC}$ and $-V_{CC}$). The load resistance is 30Ω. What is the maximum power dissipation?

P_d maximum occurs one-half the supply, 55 volts/2...
$P_d = (55)^2/(4)(30\Omega) = 25.2W$.

Some applications require handling slowly varying DC signals. In this situation, SOA limits must be evaluated with some judgment. If the rate of change of the signal is very slow, DC SOA limits must be observed for the worst case instantaneous condition. More rapidly changing signals must be considered based on the

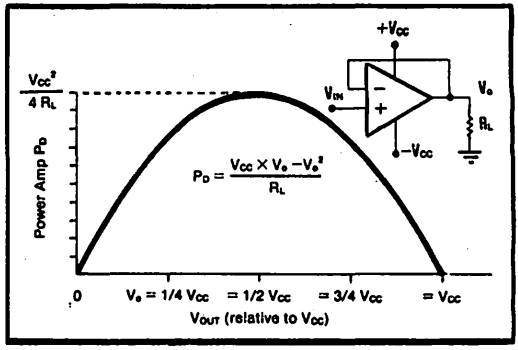


FIGURE 6. The power dissipation for a simple resistive load and DC input signal is at a maximum when the output voltage is VP/2. Despite the larger currents at higher output voltages, the dissipation is actually lower. It approaches zero as the V_{CE} nears zero at maximum output voltage.

approximate dwell time of the most stressful condition. Figure 7 shows how this might be arrived at in a typical situation. The duration and conditions of this point can then be compared to the pulsed SOA limits for safety. For obvious reasons, it is best not to push this type of operation too far. Maximum reliability will be achieved by taking a conservative approach to SOA limits.

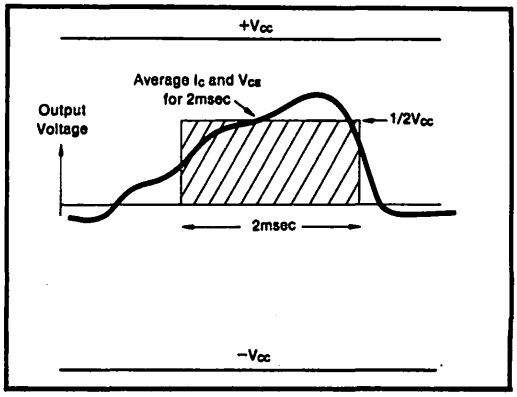


FIGURE 7. A pulsed waveform can be evaluated for safety by a graphical approximation with a rectangular pulse at the worst-case instantaneous point. The duration and conditions are then compared to the pulsed SOA data. Duty cycles greater than approximately 10% should be given plenty of guard band to allow for recovery from any localized heating during the pulse.

AC SIGNALS [SINE WAVE]

Low frequency AC signals (less than 200Hz) should be treated as slowly changing DC as described above, but for high frequencies (roughly 200Hz and above) the average power dissipation should be considered. In this situation, the transistors do not instantaneously change temperature in response to the signal waveform but are heated according to the average transistor dissipation. Figure 8 shows the average total power dissipation for both output transistors as a function of relative output voltage. The shape of this curve is similar to that of Figure 6 for DC conditions but the average dissipations are lower for AC. The instantaneous dissipation at the worst case of $V_{out} = \pm V_{CC}/2$ is the same as for DC, of course, but with AC, this point is passed only for a brief instant. The output voltage which causes the greatest

average dissipation occurs at a peak V_{out} at $2V_{CC}/\pi$. This is the signal level which causes the output to spend the greatest percentage of time near the instantaneous worst case points, $+V_{CC}/2$ and $-V_{CC}/2$.

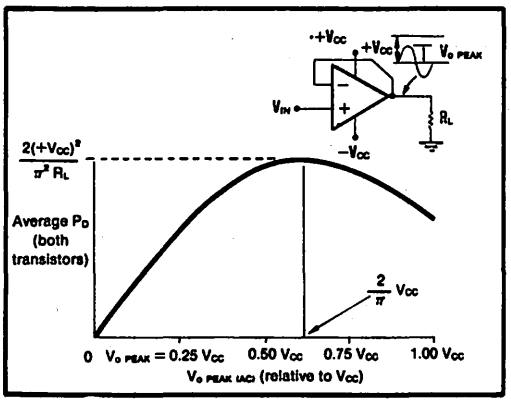


FIGURE 8. The average dissipation under continuous AC signals is a function of the output voltage relative to the supply voltage. Peak dissipation occurs at a peak AC voltage of approximately 0.6V_{CC}. Unlike the DC case, the dissipation does does not approach zero at maximum output voltage, but drops to roughly one-half its highest value.

It is safest to design the whole amplifier system as if the AC voltage to be handled is always at this worst-case signal level. Not all systems, however, need or can tolerate the expense of this over-design. If V_{out} peak will always be equal to 0.85V_{CC}, for instance, Figure 8 shows that the average dissipation will be approximately 25% less than worst case. An audio amplifier would likely dissipate far less than the worst case power because audio signals have high peak voltages relative to the average signal level (high crest factor). The heat sink could then be designed accordingly.

TEMPERATURE DERATING

As previously mentioned, SOA curves are normally based on a +25°C case temperature. Reduced limits for higher case temperatures (T_{case}) may be found by using the temperature derating curve shown in Figure 9. The slope of this curve above +25°C is equal to the junction to case thermal resistance, θ_{j-c}. If the line were extrapolated to the zero dissipation point it would intersect at the maximum chip temperature (T_j max). If the V_{CE} is below the second breakdown region, the derated power dissipation may be read directly from the curve. The maximum current in this situation is simply

$$I = \frac{P \text{ derated}}{V_{CE}}$$

For V_{CE} voltages in the secondary breakdown region, the allowable current at a given operating point may be calculated by

$$I = \text{rated } I_C \frac{T_J \text{ max} - T_{case}}{T_J \text{ max} - 25°C}$$

Example 3:

What is the maximum safe current for the 3573 during continuous short circuit to $-V_{CC}$? Power supply is ±28V, T_{case} (case temperature) is +60°C.

Solution: V_{CE} = total supply voltage = 56V

Rated I_C = 0.35A (from Figure 2)

$$I_C \text{ max} = (0.35A)\frac{150 - 60}{150 - 25} = 0.25A.$$

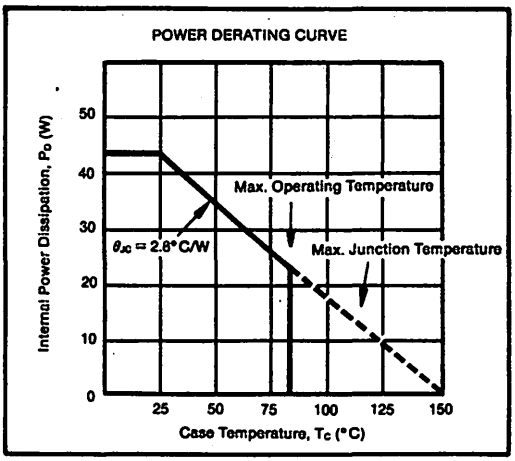


FIGURE 9. The power derating curve indicates that internal dissipation must be reduced at case temperatures greater than +25°C. This reduces the available SOA in the power and second breakdown regions.

Often these calculations are made "in reverse" to find the allowable temperature rise for a required load current. The maximum junction temperature is then used to calculate the heat sink necessary for a required maximum ambient temperature. See the application note on heat sinking (AN-83) for details on these calculations.

Some amplifiers may require a different SOA derating at elevated temperatures. In this case, derating curves are normally shown on the SOA chart as a family of curves (as for pulsed operation). Remember that case temperature must be used for these calculations.

REACTIVE LOADS

Figure 10 shows the AC voltage/current waveforms for an inductive load. Since the load current lags the load voltage by 90°, the peak current occurs when the load voltage is zero. At this instant of maximum current, the voltage across the conducting transistor is equal to the full supply voltage, $+V_{CC}$ (or $-V_{CC}$ at 180°). This obviously leads to much greater power dissipation than with a resistive load.

The average power dissipation can be determined by a simple procedure which is applicable for a wide variety of circumstances. The power dissipated in the amplifier must be equal to the power delivered by the power supplies less the power delivered to the load. If the load is purely reactive the load power is by definition zero. No power can be dissipated in a perfect inductor or capacitor. For complex load impedances the load power can be measured: $P_{out} = (I_{out}\text{ rms})(V_{out}\text{ rms})(\cos\theta)$, where θ is the phase angle between the load voltage and current.

The supply power is easily calculated for sine wave signals and is not sensitive to the type of load impedance, only the load current. Since the power comes from a

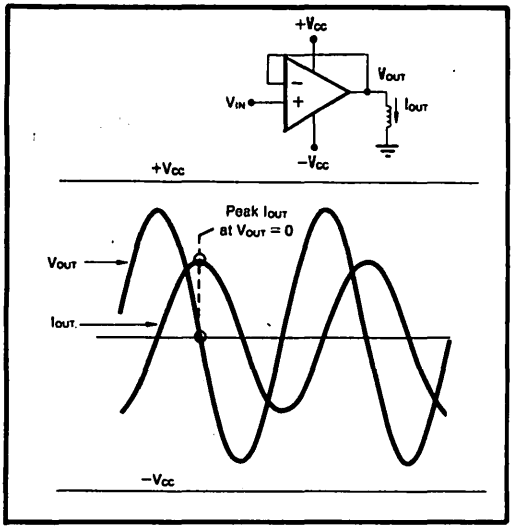


FIGURE 10. In an inductive load, the current waveform lags the applied voltage by 90°, resulting in higher instantaneous and average dissipation.

fixed DC voltage supply, it is equal to V_{CC} times the average (not rms) supply current. For a sine wave this is $2V_{CC}$ (I peak) / π. Each supply provides this for its active half-cycle and "rests" for the opposite half-cycle.

Supply power may also be measured. An average responding meter such as a standard D'Arsonval type can be inserted in the supply lines and will properly read the average supply current even for nonsinusoidal waveforms. The determination of the load power in this case, however, may require some ingenuity. The principle of power in less power out is a valuable one and can be applied to any type of signal or load condition. Try to apply it to your application!

Example 4:

A sine wave is applied to a complex reactive load. The peak load voltage is 30V and the peak load current is 1.75A. $V_{CC} = \pm 35V$. A phase angle of 55° is measured between the load voltage and current. What is the amplifier dissipation?

Power supply power, $P_S = 2(35V)(1.75A)/\pi = 39W$

Load power, $P_{out} = (.707)(30)(.707)(1.75)\cos\theta = 15W$

Amplifier dissipation, $P_d = P_S - P_{out} = 24W$

This is the power dissipated by both output transistors averaged over a full cycle. The dissipation of each individual transistor is half the total. In some cases it may be possible to use this fact to advantage since the junction temperature rise of each transistor is according to its own dissipation, not that of the total amplifier.

DC signals may also present problems with reactive loads. Since any change in load voltage (a step change in DC output for instance) implies a change in V_{CE} without an accompanying change in current. The voltage across an inductor can be instantaneously changed—the current cannot. The result is a temporary condition of high V_{CE} and high current. A similar situation exists with capacitive loads. An attempt to charge a capacitor will lead to high transient currents. In either case, the current must be limited to a safe value based on the SOA curves.

MOTOR LOADS

Motor loads can be particularly challenging since they may present a reactive load as well as reverse EMF to the driving power amp. These situations may be difficult to analyze by the techniques previously described since the power delivered to the load may be converted largely to mechanical power. In fact, sometimes mechanical inertia causes the load to supply power to the amplifier. Consider a DC motor which must be stopped rapidly (Figure 11). The motor produces a reverse EMF which is proportional to its rotational speed. If the applied voltage is suddenly forced to zero, the full negative power supply voltage, $-V_{CC}$, will appear across the conducting transistor and the load current will be the motor EMF divided by the motor series impedance (assuming no current limit).

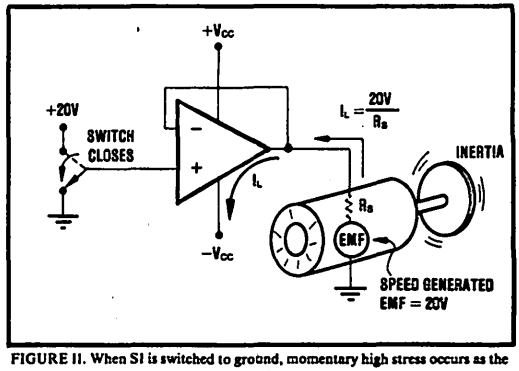


FIGURE 11. When S1 is switched to ground, momentary high stress occurs as the motor EMF forces current into the amplifier which flows to the negative supply. The duration of this condition is dependent on the mechanical inertia and load on the motor.

Such conditions may be difficult to analyze, but can usually be satisfactorily evaluated by empirical tests. Voltage and current measurements can be made under actual load conditions (including mechanical load and inertia to find its duration) to assure operation within the SOA. Figure 12 shows one possible method using a storage oscilloscope to capture the transient condition of maximum stress. Remember, this is not necessarily the point of maximum voltage or current. Points must be plotted on the voltage-current curve to find the highest stress and its duration.

A variety of applications have been presented with associated analysis and measurement techniques. Perhaps no single example shown here will exactly fit your unique situation, but by combining these ideas, most any application can be successfully evaluated.

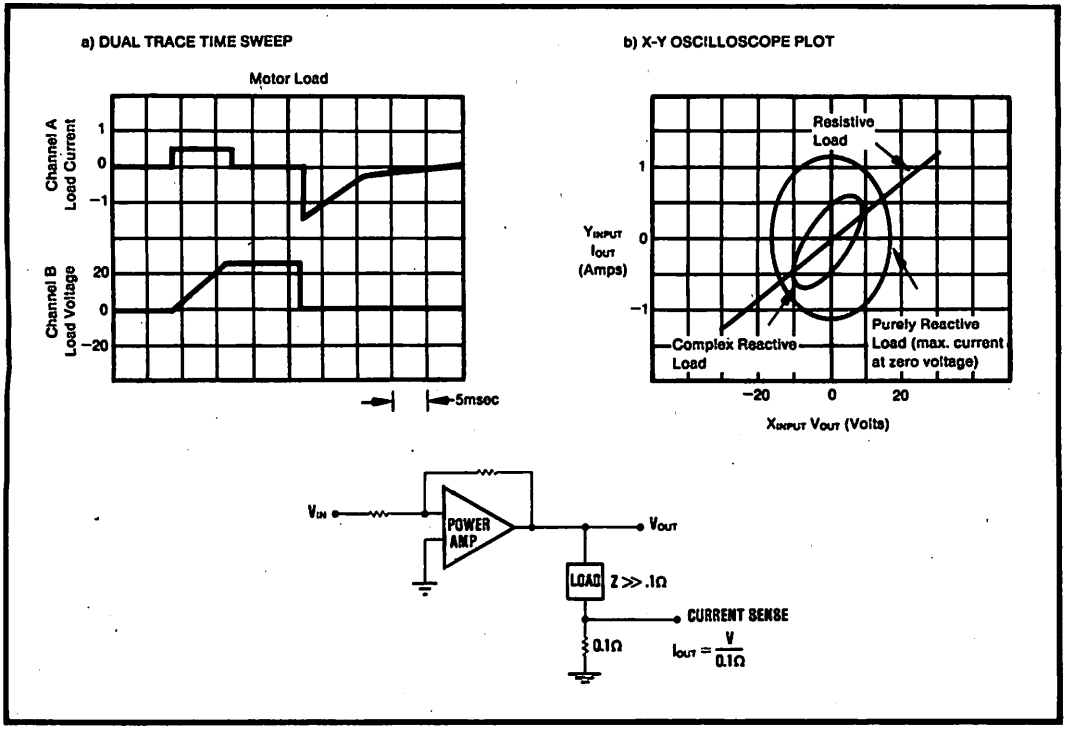


FIGURE 12. Many measurement schemes can be helpful in determining conditions of unusual loads. Setup "a" is useful in analyzing the duration of worst case conditions with motor loads. A storage oscilloscope is used to capture transient waveforms of load current and voltage. The X-Y approach used in "b" may reveal the nature of unknown loads. In both methods, the displayed load voltage must be subtracted from the power supply voltage to find V_{CE}.

VARYING COMPARATOR HYSTERESIS WITHOUT SHIFTING INITIAL TRIP POINT

An operational amplifier is a convenient device for analog comparator applications that require two different trip points. The addition of a positive-feedback network will introduce a precise variable hysteresis into the usual comparator switching action.[1] Such feedback develops two comparator trip points centered about the initial trip point or reference point.

In some control applications, one trip point must be maintained at the reference level, while the other trip point is adjusted to develop the hysteresis. This type of comparator action is achieved with the modified feedback circuit shown in the figure.

Signal diode D_1 interrupts only one polarity of the positive feedback supplied through resistor R_2. Hysteresis, then, is developed for only one comparator state, and one trip point remains at the original level set by the reference voltage, E_R. The second trip point, the one added by hysteresis, is removed from the original trip point by:

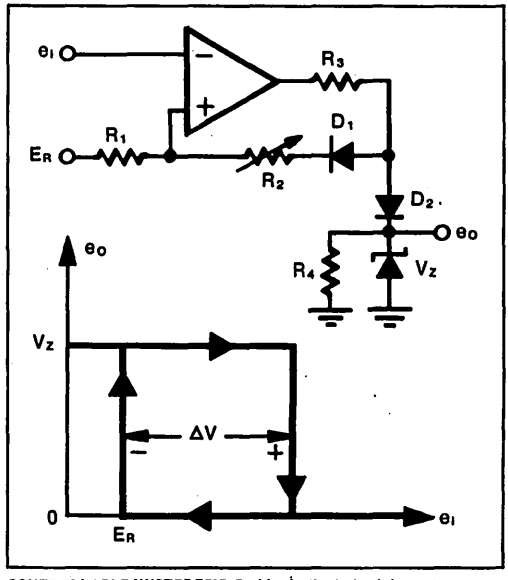
$$\Delta V = R_1 (V_Z - E_R)/(R_1 + R_2)$$

where V_Z, the zener voltage, is greater than reference voltage E_R. Varying resistor R_2 will adjust the hysteresis without disturbing the trip point at E_R.

The circuit's other performance characteristics are similar to the common op-amp comparator circuit. The accuracy of both trip points is determined by the op amp's input offset voltage, input bias current, and finite gain. Resistor R_3 limits the current drain through the zener diode, and resistor R_4 provides a discharge path for the capacitance of diode D_2.

The output signal can be taken either directly from the op amp output or from the zener diode, as shown. With the latter hookup, the output signal voltage alternates between zero and zener voltage V_Z, which might be desirable for interfacing with digital logic circuits. It should be noted, however, this output cannot sink current in the 0-volt state.

Switching speed is determined by the op amp's slewing-rate limit for high-level input-drive signals. When the input drive is a low-level signal, the output rate of change is limited by the gain available to multiply the input signal's rate of change. Both the slew-rate limiting and the gain limiting of switching time are eased if phase compensation is removed from the op amp.



CONTROLLABLE HYSTERESIS. Positive feedback circuit for analog op-amp comparator does not shift the initial reference trip point while introducing hysteresis in the second trip point. The voltage difference, ΔV, between the trip points can be adjusted by varying resistor R_2. When the output voltage is taken from the zener diode, as shown, it switches between zero and V_Z, the zener voltage.

REFERENCE:

1. G. Tobey, J. Graeme, and L. Huelsman, "Operational Amplifier: Design and Applications," McGraw-Hill, 1971.

AUTOMATICALLY TEST THE LINEARITY OF 12-BIT ANALOG-TO-DIGITAL CONVERTERS

ABSTRACT

Determining the linearity or differential linearity error of a 12-bit analog-to-digital converter (ADC) using manual techniques can be a time-consuming and tedious task. An attractive alternative is the automatic integrator servo-loop method described here that can easily test all 4095 codes if desired. The accuracy is completely determined by a digital voltmeter (DVM) which can be easily calibrated.

INTRODUCTION

Static testing of the linearity error or differential linearity error of a digital-to-analog converter (DAC) is relatively easy because for each digital input code there is a unique analog output. An ADC, on the other hand, has a continuous range of analog input voltages that can produce a given output code. This range is determined by the full-scale range and resolution of the ADC and is equal to one least significant bit (LSB). The linearity error is determined by measuring the analog input voltage that causes a transition from one digital output code to the next and comparing this to the ideal transition voltage. The differential linearity error is determined by measuring the difference between any two adjacent transition voltages and comparing this to an ideal one LSB (see Figure 1). A test method that automatically searches for these transitions is described in this application note.

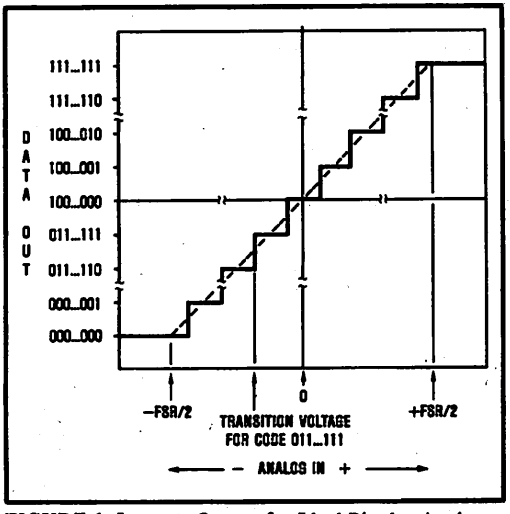


FIGURE 1. Input vs Output for Ideal Bipolar Analog-to-Digital Converter.

THEORY OF OPERATION

The block diagram for a test set which will allow the transition voltage for any given ADC output code to be determined automatically is shown in Figure 2. The ADC under test, the digital comparator, and the integrator form a servo loop. A computer serving as the test controller specifies the code for which a transition voltage measurement is desired. This digital word is called the "target code". The output of the digital comparator is used to control the slope direction of the integrator output voltage. It is configured such that at the end of each conversion by the ADC under test, the integrator output voltage will be set to ramp towards the transition voltage for the target code. A comparator output resulting from an ADC output code less than the target code causes the integrator output to slope in a positive direction. If the ADC output code is equal to or greater than the target code, a negative output slope is forced. Thus, when a new target code is specified by the computer, the integrator output voltage will ramp from its current level towards the transition level for the code, and will lock onto the transition voltage once it is reached.

In its locked state, the integrator output will (ideally)* be a triangle wave, centered on the transition voltage, with a peak-to-peak amplitude of:

$$\Delta V = -(I/C)\Delta t$$

where: I = Integrator input current, ($|+I| = |-I|$)
C = Integrator capacitance
Δt = Conversion interval

Because the DVM acquires the transition voltage by averaging the integrator output, ΔV, which defines the resolution of the test, should be kept small, (1/16 LSB or less).

A locked-loop condition is sensed by successively reading the integrator output. When the voltage difference between successive DVM readings is smaller than a value determined by the $\Delta V/\Delta t$ of the integrator and the time period separating the DVM readings, the loop may be considered locked.

With the computer controlling the DVM as well as providing the target code to the test set, transition voltages for all codes (except code 0) may be acquired automatically. "Transition voltage" in the context of this applications note is defined as the ADC input voltage which causes (with repeated conversions) the digital output

*Converter noise, hysteresis, and asymmetrical integrator input currents will cause the integrator to deviate from the ideal triangle wave.

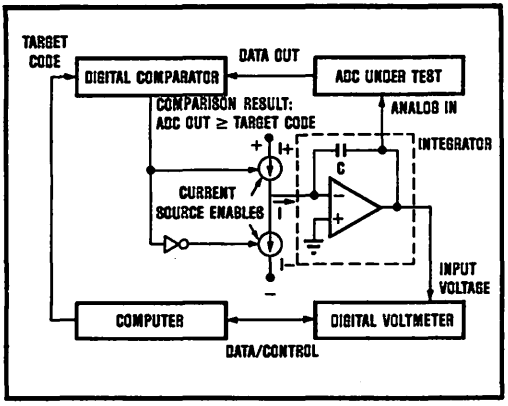


FIGURE 2. Servo-Loop Test Set Block Diagram.

code to be equally distributed between the specified code and the code one less than that specified. Code 0, then, has no transition voltage. Specification of zero as the target code would cause the integrator output to ramp to its most-negative output level and remain there. Once transition voltage readings for all desired codes have been acquired, the computer reduces this data to produce the offset, gain, linearity, and differential linearity parameters for the device under test.

CIRCUIT OPERATION

Figure 3 is the test set timing diagram. Figure 4 is a schematic diagram of a test set designed to test the Burr-Brown ADC803.

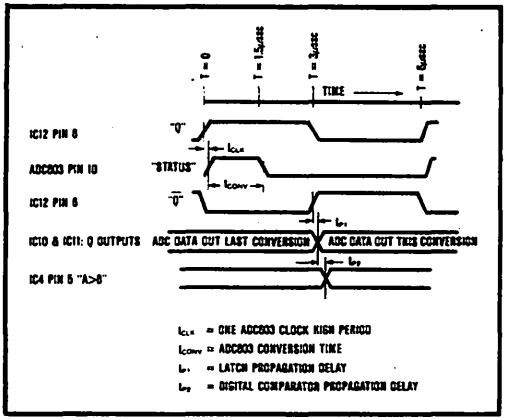


FIGURE 3. Test Set Timing Diagram.

IC12 produces a square wave of 6μsec period, which is used as the system timebase. A rising edge on the Q output of IC12 will initiate a conversion by the ADC under test. When this signal returns low, the ADC will have completed the conversion, and its output code is latched in IC10 and IC11 by the rising edge on the $\overline{Q}$ output of IC12. (The ADC803 is a successive-approximation type converter, so its outputs are dynamic during the conversion period. If its outputs were not latched, an erratic signal would appear at the integrator slope control pin during a conversion.)

The 12-bit digital comparator (IC4-7) is configured in a nibble-parallel fashion to achieve low propogation delays. A straight binary comparison is made with the target code fed to the A comparator inputs, and the latched ADC output fed to the B side. The A > B (Target > ADC output) comparator output is used to control the integrator slope.

IC9 and C21 form the integrator. Current sources R14 (+) and IC8, R8-11 (−) produce the comparator input current. When IC4 pin 5 goes low (ADC output code ≥ Target code), the negative current source (IC8, R8-11) is turned off, and current flows through R14 into the integrator input, causing the integrator output voltage to ramp in a negative direction. The current flow through R14 is equal to 5V/510kΩ, or approximately 10μA. The integrator output slope under these conditions is, then:

$$\Delta V = -(I \div C)(\Delta t)$$
$$= -[(10 \times 10^{-6}) \div (1 \times 10^{-6})][6 \times 10^{-6}]$$
$$= -60\mu V/\text{conversion interval}$$

When IC4 pin 5 goes high (ADC output code < Target code), the negative current source (IC8, R8-11) is turned on, and IC8 pin 11 sinks approximately 20μA. This pin sinks the current from R14, and draws the residual 10μA from the integrator input, causing the integrator output voltage to ramp in a positive direction. The positive and negative current inputs are equal in magnitude, so the positive and negative integrator output slopes are equal as well.

The digital comparator A < B (Target code < ADC output) is used to sense an ADC missing code failure. When the integrator loop is in a locked state, this output should never become active because the integrator slope is switched at the ADC out < Target code, and ADC out ≥ Target code points. Assertion of the ADC out > Target code line indicates that the converter under test has skipped the target code, and its outputs are switching between Target code −1 and Target code +1. R5, C3, and IC1 form a low-pass filter to prevent noise from causing a missing code indication. A missing code state must exist for longer than 30msec in order for the missing code output line to become active.

The ADC803 is configured for 20V full-scale range biopolar operation (±10V input) and a conversion time of 1.5μsec. Closure of the "clock rate adjust" switch will allow adjustment of the conversion time from 800nsec to 2μsec to allow device testing at various operating speeds.

CONSTRUCTION NOTES

The printed circuit layout (Figures 5 and 6) can be photographically copied from this application note. Printed circuit board material is 0.062" thick, double-sided copper-clad, G-10 material. Plated-through holes are required. Figure 7 shows the parts layout and Table I lists all required parts. Figure 4 shows proper digital input connections for use of HP GPIO or PCI3000. Appropriate changes must be made for other input/output systems.

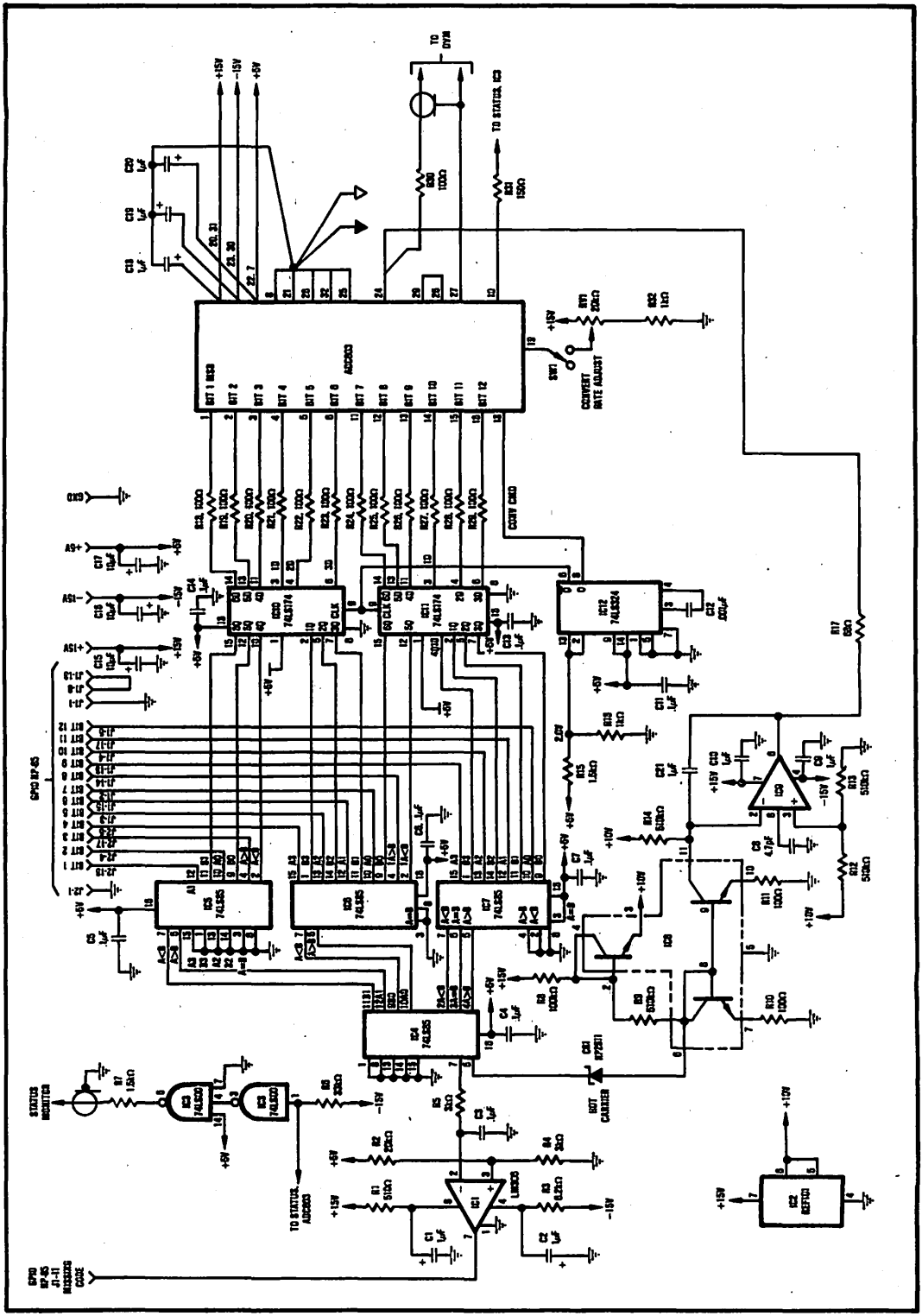


FIGURE 4. ADC803 Test Set.

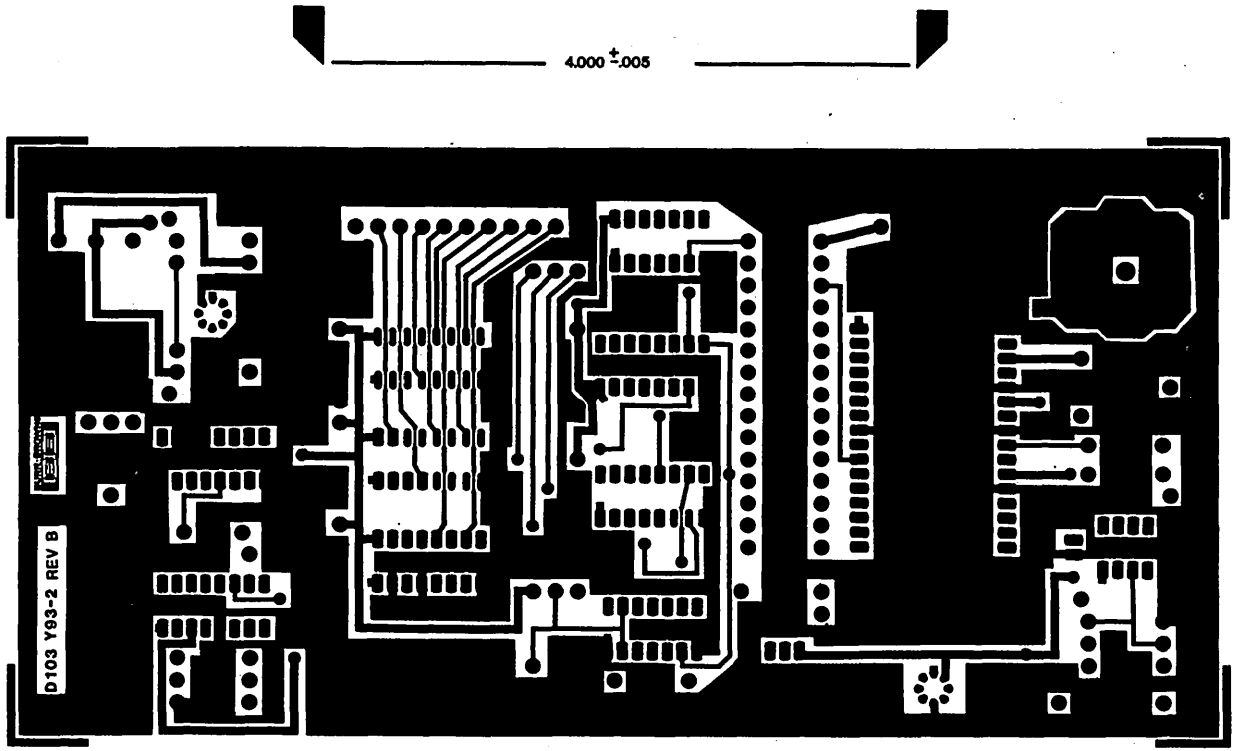


FIGURE 5. PC Board—Top.

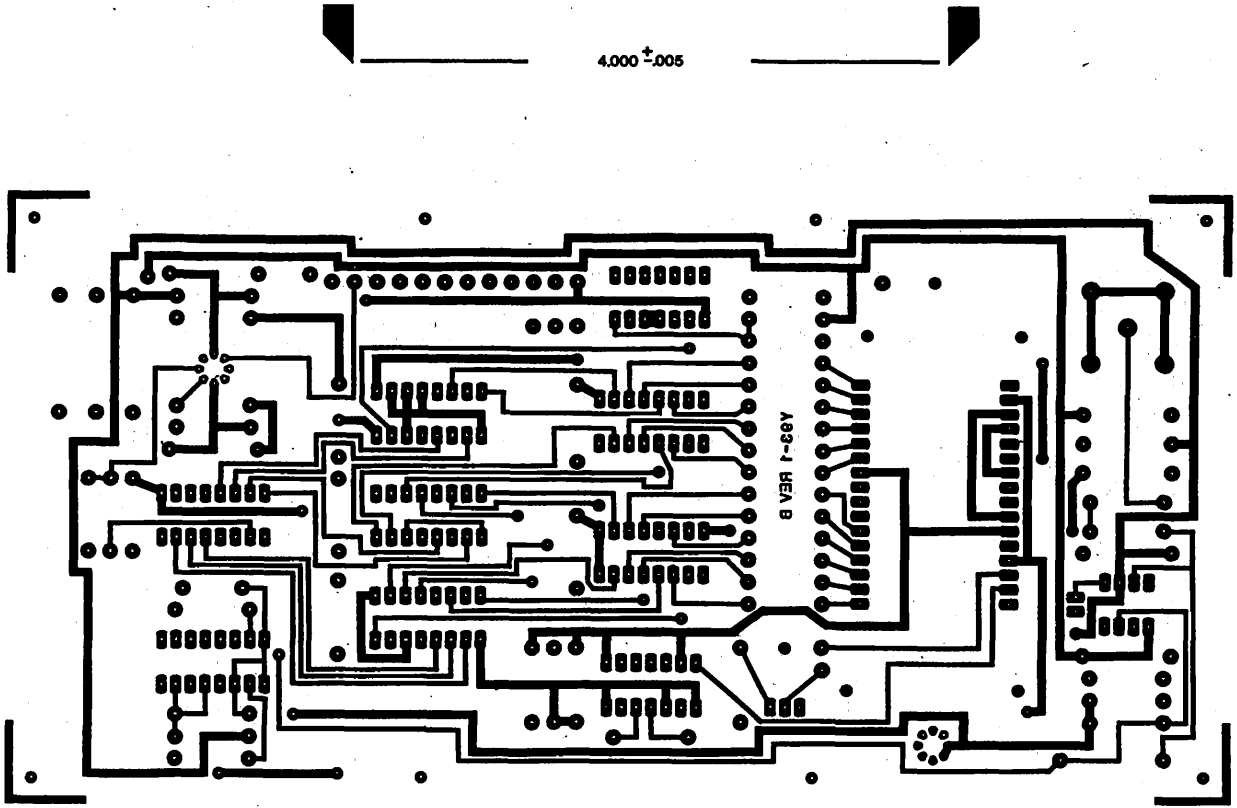


FIGURE 6. PC Board—Bottom.

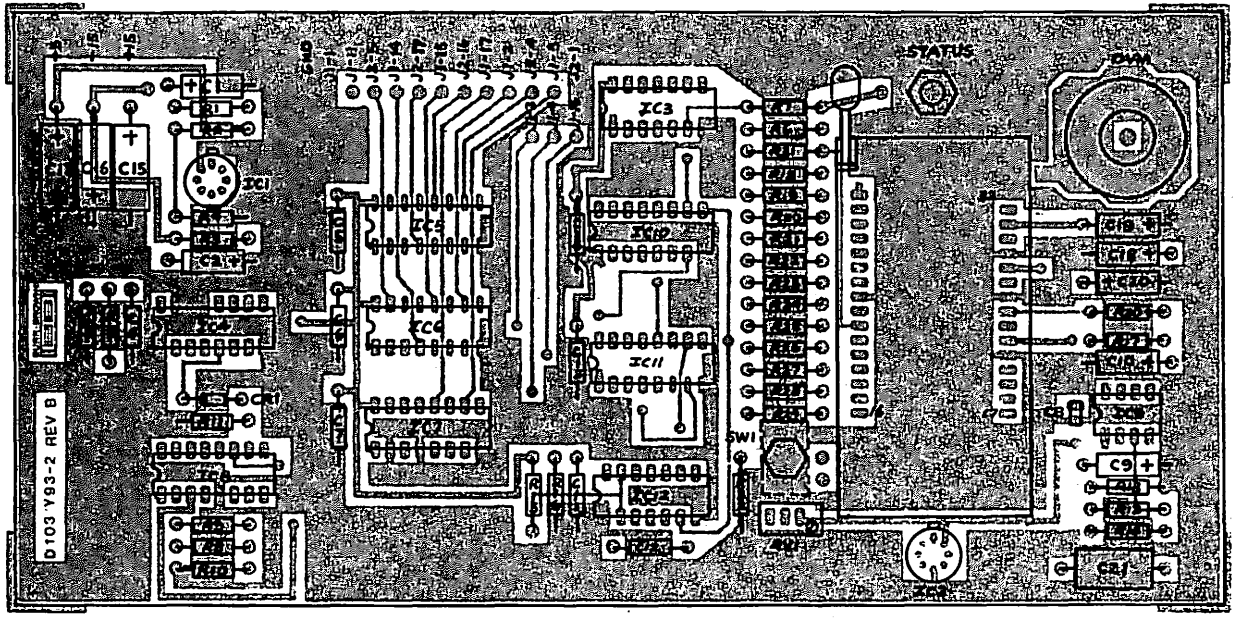


FIGURE 7. PC Board—Component Layout.

TABLE I. Parts List for Test Fixture.

Reference Designation	Quantity	Description	Comments
		MISCELLANEOUS	
	2	8-pin IC socket	Augat 508-AG19D
	2	14-pin IC socket	Augat 514-AG19D
	7	16-pin IC socket	Augat 516-AG19D
	1	BNC connector	Amphenol 31-4558
	1	PC board	See Figures 5 & 6
		RESISTOR, FIXED	
		Comp., ±5%, 1/4W	
$R_{10\text{-}30,\ 10,\ 11}$	13	100Ω	
$R_{16,\ 32}$	2	1kΩ	
R_9	1	100kΩ	
R_{31}	1	150Ω	
R_7	1	1.5kΩ	
$R_{4,\ 5}$	2	3kΩ	
R_6	1	33kΩ	
$R_{8,\ 12\text{-}14}$	4	510kΩ	
R_{17}	1	68Ω	
R_2	1	20kΩ	
R_3	1	6.2kΩ	
		Wirewound, ±%, 1/10W	
R_1	1	510Ω	
R_3	1	6.2KΩ	
		RESISTOR, VARIABLE	
RV_1	1	20kΩ	
		DIODE	
CR_1	1	Hot carrier	HP2811
		INTEGRATED CIRCUITS	
IC_9	1	Op amp	OPA27
IC_3	1	Reference	REF101
IC_1	1	Op amp	LM306
IC_3	1	Quad NAND	74LS00
$IC_{4,\ 5,\ 6,\ 7}$	4	Quad comparator	74LS85
$IC_{10,\ 11}$	2	Hex latch	74LS174
IC_{12}	1	VCO	74LS324
IC_8	1	Transistor array	RCA3127
		CAPACITORS	
$C_{3\text{-}7,\ 13,\ 14}$	9	0.01μF, ceramic, 25V	
C_8	1	0.1μF, ceramic, 25V	
C_{12}	1	0.001μF, ceramic, 25V	
$C_{18\text{-}20}$	3	1μF, solid tantalum, 35V	
$C_{15\text{-}17}$	3	10μF, solid tantalum, 35V	
$C_{1,\ 2,\ 9,\ 10}$	4	1μF, dipped, solid tantalum, 35V	
C_{21}	1	1μF, metalized polycarbon, 35V	

Connect the power supply leads to the circuit board by tack-soldering them directly to the power pads of the ADC under test. This helps to prevent power supply noise generated by other parts of the test circuit from affecting ADC operation.

SOFTWARE FOR USE WITH THE SERVO-LOOP TEST FIXTURE

Writing software for use with servo-loop test fixtures is quite straightforward. A test program which runs on the HP85 computer with GPIO interface is listed in Figure 8. This program tests and reports offset error, gain error, linearity, differential linearity, and missing code errors for all codes.

For machines other than the HP85, the HP85 listing may be used as a model. Formulas for error calculation are shown in Figure 9. Be sure to check the logic sense of your interface. Some invert data out or data in. Finally, in all cases make sure that the converter under test is powered and has warmed up before testing.

```
10  ! "SERVO LOOP TEST FOR ADC803"
20  !
30  ! VARIABLE DEFINITIONS
40  ! A1 = TRANSITION VOLTAGE FOR CODE 1
50  ! A2 = TRANSITION VOLTAGE FOR CODE 4095
60  ! A3 = TEMP. STORAGE OF LAST TRANSITION VOLTAGE
70  ! B = LSB VALUE OF CONVERTER UNDER TEST
80  ! C = CODE: USED AS LOOP CNTR, AND TO PASS TO SUBROUTINE
90  ! C1 = CODE WHERE WORST-CASE LINEARITY ERROR OCCURS
100 ! C2 = CODE WHERE WORST-CASE D.L. ERROR OCCURS
110 ! G = GAIN ERROR
120 ! M = MISSING CODE STATUS PASSED FROM SUBROUTINE
130 ! O = OFFSET ERROR
140 ! T = USED IN SUBROUTINE TO SENSE LOCKED LOOP
150 ! V = TRANSITION VOLTAGE FOR CODE C
160 !
170 !
180 ! " CONFIGURE GPIO PORT "
190 CONTROL 4,0;0     ! NO PARITY
200 CONTROL 4,1;1     ! NO INTERRUPT
210 CONTROL 4,4;192   ! NO HANDSHAKE
220 CONTROL 4,6;0     ! NO DELAY
230 CONTROL 4,8;3     ! ENABLE A&B PORTS
240 CONTROL 4,9;0     ! OUTPUTS UNINHIBITED
250 !
260 ! " CONFIGURE HP3478A DVM: IEEE ADDRESS 23 "
270 OUTPUT 723; F1R1Z0N5D3TESTING
280 !
290 ! " START TEST "
300 !
310 C=1
320 GOSUB 730  ! GET TRANSITION FOR CODE 1
330 IF M= -1 THEN PRINT "CODE 1 MISSING, TEST ABORTED"
340 IF M= -1 THEN STOP
350 A1=V
360 O= A1-(-9.99755)  !OFFSET ERROR IN VOLTS
370 PRINT"OFFSET ERROR=";O; "VOLTS"
380 C=4095
390 GOSUB 730  ! GET TRANSITION FOR CODE 4095
400 A2=V
410 G= (((A2-A1)/19.995117)-1)X100  ! IN % FSR
420 PRINT "GAIN ERROR="; G ;"% FSR"
430 B=(A2-A1)/4094  ! LSB IN VOLTS
440 !
450 !" ACQUIRE TRANSITIONS & COMP. ERRORS "
460 M1=0
470 M2=0   ! SET MAX ERRORS TO 0
480 A3=A1  ! LAST TRANSITION=CODE 1 VT
490 FOR C =2 TO 4095
500 GOSUB 730
510 IF M=-1 THEN PRINT "CODE" ; C ;"MISSING"
520 IF M=-1 THEN GOTO 600 ! SKIP CALCS IF MISSING CODE
530 L=((V-(A1+(C-1)*B))/B)-1 ! LIN.ERR. IN LSBS
540 IF ABS (L)>M1 THEN C1=C
550 IF ABS (L)>M1 THEN M1=ABS (L) ! UPDATE MAX LIN. ERR.
560 D= ((V-A3)/B)-1 ! D.L. ERROR LAST CODE
570 IF ABS (D)>M2 THEN C2=C-1
580 IF ABS (D)>M2 THEN M2=C-ABS(D) ! UPDATE MAX D.L. ERR.
590 A3=V
600 NEXT C
610 PRINT "MAX. LINEARITY ERROR=";M1;"LSBS AT CODE"; C1
620 PRINT "MAX. D.L. ERROR=";M2;"LSBS AT CODE"; C2
630 PRINT "TEST COMPLETE"
640 STOP
650 !
660 ! " SUBROUTINE-ACQUIRE TRANSITION VOLTAGE "
670 ! "              -AND MISSING CODE STATUS"
680 ! " ENTRY    :C: CODE TO ACQUIRE FOR
690 ! " EXIT     :V: TRANSITION VOLTAGE
700 ! "          M: MISSING CODE STATUS
710 ! " INT      :T: TEMP STORAGE
720 !
730 OUTPUT 410 USING "#,W";C
740 ENTER 723;V
750 T=V
760 ENTER 723;V
770 IF ABS (V-T)>.0001 THEN GOTO 750
780 ENTER 410 USING "#,W";M
790 RETURN
800 END
```

FIGURE 8. Test Program for HP85 Computer with GPIO Interface.

$$LSB_{DUT} = \frac{V_{T(2^N - 1)} - V_{T(1)}}{(2^N - 2)} \quad \text{(Volts)}$$

$$\text{Offset Error} = V_{T(1)} - \frac{1}{2}\left(\frac{FSR}{2^N - 1}\right) \quad \text{(Volts) for unipolar converters}$$

$$= V_{T(1)} - \left[\frac{1}{2}\left(\frac{FSR}{2^N - 1}\right) - \frac{1}{2}\ FSR\right] \quad \text{for bipolar converters}$$

$$\text{Gain Error} = \left[\left(\frac{V_{T(2^N - 1)} - V_{T(1)}}{FSR\left[\frac{2^N - 2}{2^N - 1}\right]}\right) - 1\right] \times 100 \quad \text{(\% FSR)}$$

$$\text{Linearity Error}_{CODE} = \frac{V_{T(CODE)} - [V_{T(1)} + ([CODE - 1] \times LSB_{DUT})]}{LSB_{DUT}} - 1 \quad \text{(LSBs)}$$

$$\text{D.L. Error}_{CODE} = \frac{V_{T(CODE + 1)} - V_{T(CODE)}}{LSB_{DUT}} - 1 \quad \text{(LSBs)}$$

where: LSB_{DUT} = LSB value (volts) for converter under test

$V_{T(CODE)}$ = transition voltage for code

N = resolution of converter (number of bits)

FSR = ideal full scale range for converter

FIGURE 9. Formulas for Error Calculation.

DATA CONVERTER TEST METHODS FOR DIGITAL AUDIO APPLICATIONS

Proponents of digital audio claim that it offers overwhelming advantages over conventional analog techniques. The theoretical dynamic range of 96dB (16 bits), lower harmonic distortion, and the elimination of wow, flutter, and crosstalk are some of the significant advantages of digital recording techniques. Digital recording can provide tapes or record discs from which the audio information can be decoded repeatedly, without degradation and wear, by the use of noncontact pickups. Errors caused by dirt or defects can be detected and most can be corrected or at least concealed. Digital audio truly has the potential to reproduce music that even experts cannot distinguish from the original.

Advances in digital technology such as low cost microprocessors and very large scale integration (VLSI) logic have greatly reduced the cost of processing the audio information once it is in digital form. However, the most critical links in a digital audio system are the converters that transform the signal between the analog and digital domains. The digital audio industry requires analog-to-digital (A/D) (record) and digital-to-analog (D/A) (playback) converters with 14- to 16-bit resolution to obtain the desired dynamic range (>90dB) and signal-to-noise ratio. Modular and hybrid converters designed for industrial instrumentation applications, with 14- to 16-bit resolution and corresponding ±1/2LSB integral linearity error, have been available for several years. These converters range in price from about $50.00 for a 14-bit hybrid D/A to over $1000 for a high-speed, true 16-bit A/D. Although many of these converters will perform quite well in a digital audio system, they are much too expensive to be used in a consumer digital audio disc player, for example, that must sell in the $100.00 to $1000.00 price range if it is to compete with high quality analog equipment.

There are two key items involved in bringing the price of these converters down to the required range: (1) an understanding of the specifications required for audio applications and how they differ from those required for traditional instrumentation applications, and (2) high volume which justifies the initial manufacturing expense of higher levels of integration. For example, parameters such as gain accuracy, offset error, integral linearity error, and reference voltage accuracy, with corresponding ultra-low drift of these parameters versus time and temperature, are critical in most general instrumentation applications, but are less important in digitizing audio signals. These also happen to be some of the most difficult and expensive items to achieve in the manufacture of conventional high accuracy data converters. Conversely, in audio applications, we are primarily concerned with wide dynamic range (14- to 16-bit resolution), low total harmonic distortion for both high-level and low-level signals over the full audio spectrum (10Hz to 20kHz), and low differential linearity error near bipolar zero (which reduces the crossover distortion for low-level signals). The temperature stability of these parameters is not as critical as in most instrumentation applications due to the relatively narrow temperature excursions seen by audio equipment. However, they must be stable with time since periodic calibration is impractical.

One of the problems encountered in developing converters specifically for the audio industry is that of agreeing on the definitions for the various specifications applied to converters, as well as agreeing on the test circuits and parameter limits. For example, an audio manufacturer has a specific limit for the total harmonic distortion, however, it is difficult to correlate this with any parameter that is specified for a conventional data converter. In other words, the preferred testing technique, from an audio manufacturer's point of view, is to simply insert the data converter into their digital audio system and verify that the system meets all specifications. This is not desirable from a data converter manufacturer's point of view because of the wide variation in audio system specifications and other sources of system error such as sample/holds, deglitchers, filters, etc.

The test circuits and methods described in this Application Note are used by a number of manufacturers, of digital audio equipment, as well as by data conversion component manufacturers, for evaluating the performance of A/D and D/A converters in digital audio applications.

Harmonic distortion is one of the oldest and most universally accepted methods of measuring "linearity". The test method for a conventional analog circuit is to apply a high purity sine wave to the input of the device under test. The output signal will be modified if the input encounters any nonlinearities. A spectral analysis of this output signal will show that in addition to the original input sine wave, there will be additional components at harmonics or multiples of the input frequency. Total harmonic distortion (THD) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or decibels. This calculation may be accomplished by using a spectrum

analyzer to obtain the level of each harmonic and then performing an rms summation. This voltage is then divided by the fundamental level. An alternative procedure is to use a distortion analyzer which removes the fundamental component and measures the remainder. The remainder will contain both the harmonics and random noise. For low harmonic distortion (<0.005%) this random noise will begin to affect the measured distortion and the measurement is sometimes referred to as THD + N.

The measurement of THD for a D/A converter is inherently more difficult than for an analog component because the input to the device must be in the form of a digital code and, therefore, a pure sine wave cannot be applied directly. Also, the analog output is discontinuous, due to the finite resolution of the converter, which places a limit on the signal-to-noise ratio (SNR) and THD which can be achieved. In a binary D/A converter using a linear quantization scheme, the maximum quantization error is:

$$e_{max} = \frac{1}{2^n} A_{max}$$

where A_{max} is the full scale range (FSR) of the converter output and n is the number of digital inputs or "bits". The SNR, sometimes referred to as dynamic range, is:

$$SNR = \frac{A_{max}}{e_{max}} = 2^n$$

$$SNR\ (dB) = 6.02^n$$

Thus, the SNR can be approximately doubled (6dB) for each added bit of resolution. The maximum achievable SNR will be slightly better than this since the average quantization noise wll be somewhat less than the peak value. The SNR of an ideal n bit converter can be shown to be:

$$SNR\ (dB) = 6.02n + 1.76$$

Thus, the maximum SNR of a 16-bit D/A converter is 98.08dB.

A block diagram of a circuit for measuring the THD of a D/A converter is shown in Figure 1. The digital input codes for the D/A converter that are required to produce a sinusoidal analog output signal with a given amplitude, frequency, and update rate, are stored in the programmable read-only memories (PROM's). Only the codes required to produce one complete cycle of the output waveform need to be stored since the timing control logic and binary counter simply repeat this sequence to produce a continuous output waveform.

The deglitcher and filter are required to smooth the discontinuous output from the DAC and remove higher order harmonics, due to sampling frequency, prior to being measured by the distortion meter. The deglitcher and filter circuits are also used in actual digital audio applications. The programmable gain amplifier between the output of the low-pass filter and the input of the distortion meter is required to amplify the DAC output when measuring the THD of low level (<-40dB) output signals. The exact gain of the amplifier is not important as long as the output signal is large enough so that the distortion meter is operating in its optimum range.

A BASIC program for computing the digital input codes as well as printing the Ideal DAC Output (volts), Ideal Sine Wave Output (volts), and Quantizing Error (volts), which is simply the differnce between the ideal sine and ideal DAC outputs, is shown in Figure 2. A sample output is shown in Figure 3.

It is important to test the THD of a DAC with both high and low level outputs to completely characterize the device. This is due to the fact that a full scale THD measurement alone can effectively "mask" differential linearity problems due to the averaging effect of the distortion meter. The test conditions used by a number of digital audio equipment manufacturers are:

f_o = 420Hz, Update Freq. = 44.1kHz
(1) V_o = 0dB (±FS)
(2) V_o = -20dB
(3) V_o = -60dB

Since data conversion component manufacturers already have the capability of measuring the linearity error of D/A converters, it is desirable to have an expression that relates this error to the THD. If we assume that the error due to the test circuit in Figure 1 is negligible, then the

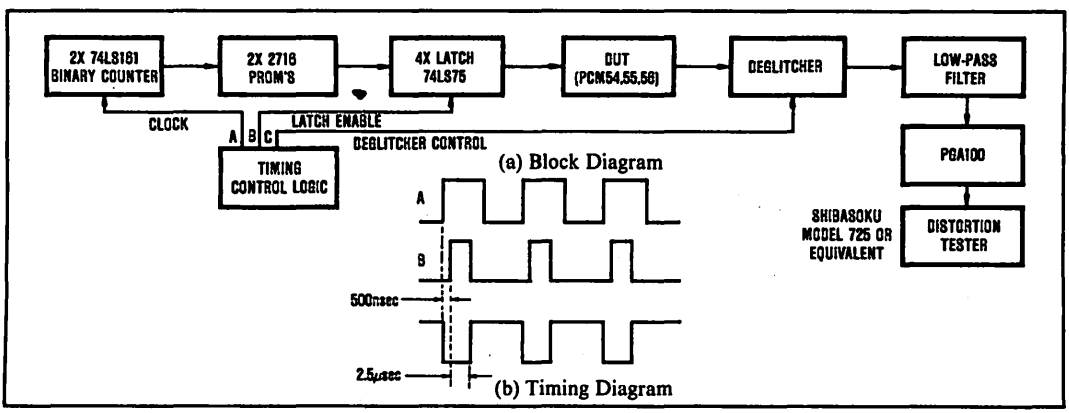


FIGURE 1. Block Diagram and Timing Diagram for Digital-to-Analog Total Harmonic Distortion Test Circuit.

```
10   REM THIS PROGRAM CALCULATES THE HEX CODES FOR ANY TEST FREQUENCY AT ANY UPD
ATE FREQUENCY.
20   REM THE UPDATE FREQUENCY, TEST FREQUENCY, TEST FREQUENCY AMPLITUDE, DAC RES
OLUTION AND FULL SCALE RANGE ARE NEEDED.
30   DEG                    ' PUTS COMPUTER IN DEGREE MODE
40   DIM Num_code(500),Ideal_sine(500),Ideal_dac(500),Quant(500),Dac_code(500)
50   DIM Hex_code$(500)
60   PRINT "THIS PROGRAM WILL CALCULATE THE CODES NECESSARY TO REPRODUCE A SINE-
"
70   PRINT "WAVE WITH A DAC.  WHEN PROMPTED, ENTER: THE UPDATE FREQUENCY, TEST"
80   PRINT "FREQUENCY, AND AMPLITUDE OF THE SINE-WAVE BEING DIGITIZED.  ALSO, TH
E"
90   PRINT "THE FULL SCALE RANGE AND THE RESOLUTION OF THE DAC BEING USED."
100  PRINT
110  INPUT "WHAT IS THE UPDATE FREQUENCY IN KHz?",Update_freq
120  Update_freq=Update_freq*1000
130  INPUT "WHAT IS THE TEST FREQUENCY IN KHz?",Test_freq
140  Test_freq=Test_freq*1000
150  INPUT "WHAT IS THE AMPLITUDE OF THE TEST SIGNAL IN db?",Aap
160  INPUT "WHAT IS THE FULL SCALE RANGE OF THE DAC IN VOLTS?",Fsr
170  INPUT "WHAT IS THE RESOLUTION OF THE DAC?",Res
180  PRINT USING "12A,X,5D,X,2A,11X,10A,X,5D,X,2A";"UPDATE FREQ=";Update_freq;"h
z","TEST FREQ=";Test_freq;"hz"
190  PRINT USING "17A,X,MDD.D,X,2A,6X,4A,X,2D.D,X,2A";"SIGNAL AMPLITUDE=";Aap;"db","
FSR=";Fsr;"v"
200  PRINT "RESOLUTION=";Res;"bits"
210  PRINT
220  Num_code=Update_freq/Test_freq      'CALCULATES THE NUMBER OF CODES REQUIRED
 TO REPRODUCE THE TEST FREQUENCY
230  Peak_amp=.5*Fsr*10^(Aap/20)         'CALCULATES THE AMPLITUDE OF THE TEST FR
EQUENCY IN VOLTS.
240  Lsb=Fsr/2^Res    'CALCULATES THE VALUE OF THE LSB IN VOLTS
250  Msb=2^Res/2  'CALCULATES THE DECIMAL CODE FOR THE MSB
260  FOR I=1 TO Num_code 'THIS IS THE LOOP TO CALCULATE THE CODES
270  Ideal_sine(I)=SIN(2*3.14*Num_code*I)*Peak_amp
280  Dac_code(I)=Ideal_sine(I)/Lsb
290  Diff=Dac_code(I)-INT(Dac_code(I))
300  IF Diff>.5 THEN Add
310  Dac_code(I)=INT(Dac_code(I))
320  GOTO 340
330 Add: Dac_code(I)=INT(Dac_code(I))+1
340  Ideal_dac(I)=Dac_code(I)*Lsb
350  Quant(I)=Ideal_sine(I)-Ideal_dac(I)  'THIS IS THE QUANTIZING ERROR OF THE DA
C
360  Dac_code(I)=Dac_code(I)+Msb  ' THIS IS THE ACTUAL DECIMAL CODE FOR THE BIT
370  NEXT I
380  FOR I=1 TO Num_code  ' DECIMAL TO HEX-DECIMAL CONVERSION
390  Code=Dac_code(I)
400  FOR J=1 TO 4
410  Code=Code/16
420  Hex=FRAC(Code)
430  Code=Code-Hex
440  Hex=Hex*16
450   IF Hex>9 THEN Hex=Hex+55
460   IF Hex<10 THEN Hex=Hex+48
470   Code$(J)=CHR$(Hex)
480  NEXT J
490  Hex_code$(I)=Code$(4)+Code$(3)+Code$(2)+Code$(1)
500  NEXT I
510  PRINT USING "4X,5A,12X,5A,10X,10A,6X,7A,6X,3A";"IDEAL","IDEAL","QUANTIZING"
,"DECIMAL","HEX"
520  PRINT USING "4X,5A,13X,5A,11X,10A,3X,7A,7X,4A";"SINE","DAC","ERROR","CODE",
"CODE"
530  PRINT USING "4X,6A,11X,6A,11X,10A";"(VOLT)","(VOLT)","(VOLT)"
540  PRINT
550  FOR I=1 TO Num_code
     .
     .
560  PRINT USING 580;Ideal_sine(I),Ideal_dac(I),Quant(I),Dac_code(I),Hex_code$(I)
570  NEXT I
580  IMAGE MDD.DDDDDD,7X,MDD.DDDDDD,9X,M.DDDDDD,9X,DDDDD,9X,4A
590  END
```

FIGURE 2. BASIC Program for Computing the Ideal DAC Output, Ideal Sinewave Output, Quantizing Error, and Hex Code.

```
THIS PROGRAM WILL CALCULATE THE CODES NECESSARY TO REPRODUCE A SINE-
WAVE WITH A DAC.  WHEN PROMPTED, ENTER: THE UPDATE FREQUENCY, TEST
FREQUENCY, AND AMPLITUDE OF THE SINE-WAVE BEING DIGITIZED.  ALSO, THE
THE FULL SCALE RANGE AND THE RESOLUTION OF THE DAC BEING USED.

WHAT IS THE UPDATE FREQUENCY IN KHz? 1
WHAT IS THE TEST FREQUENCY IN KHz? .1
WHAT IS THE AMPLITUDE OF THE TEST SIGNAL IN db? 0
WHAT IS THE FULL SCALE RANGE OF THE DAC IN VOLTS? 10
WHAT IS THE RESOLUTION OF THE DAC? 16
UPDATE FREQ=  1000 hz            TEST FREQ=   100 hz
SIGNAL AMPLITUDE=   0 db         FSR= 10 v
RESOLUTION= 16 bits

    IDEAL        IDEAL      QUANTIZING   DECIMAL     HEX
    SINE          DAC         ERROR       CODE       CODE
    (VOLT)       (VOLT)       (VOLT)
  2.938926     2.938995     -.000069      52029      CB3D
  4.755283     4.755249      .000034      63932      F9BC
  4.755283     4.755249      .000034      63932      F9BC
  2.938926     2.938995     -.000069      52029      CB3D
  0.000000     0.000000      .000000      32768      8000
 -2.938926    -2.938995      .000069      13507      34C3
 -4.755283    -4.755249     -.000034       1604      0644
 -4.755283    -4.755249     -.000034       1604      0644
 -2.938926    -2.938995      .000069      13507      34C3
  0.000000     0.000000      .000000      32768      8000
```

FIGURE 3. Sample of Program Input and Output.

rms value of the DAC output error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}$$

Where n is the number of update points for one full cycle of the sine wave, $E_L(i)$ is the linearity error of the DAC at each sample point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as:

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\%$$

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital input word of interest. However, this expression does not mean that the worst-case linearity error of the DAC is directly correlated to the THD. Table I shows the measured and calculated distortion for a Burr-Brown PCM D/A at ±FS, −20dB and −60dB output. Although the correlation between measured and calculated values is usually quite good in a well designed converter, it is usually better to actually measure the THD whenever possible since this includes the effects of dynamic settling time and noise which may be significant for low level signals.

TABLE I. Comparison of Measured Versus Calculated THD for a PCM Digital-to-Analog Converter.

OUTPUT LEVEL	MEASURED THD	CALCULATED THD
0dB	0.0018	0.0020
-20dB	0.013	0.015
-60dB	1.38	1.30

A block diagram for a THD test circuit for A/D converters is shown in Figure 4. This circuit is very similar to the DAC tester with the differences being that the PROM's and binary counter are replaced by a low distortion audio oscillator, sample/hold, and A/D converter (device under test), and the DAC under test in the previous circuit is replaced by a true 16-bit D/A converter. Although this test circuit is easier to use than the DAC THD tester because it does not require the computation of any digital codes, it does have more sources of error that can affect the accuracy of the distortion measurement. Both the DAC and ADC tester have errors caused by the deglitcher, low-pass filter, and measurement technique used by the Shibasoku 725 distortion meter which limit the lowest achievable THD measurement to about 0.002%. In addition, the ADC tester contains errors due to the audio oscillator, sample/hold, and 16-bit DAC which limit the lowest THD measurement of the ADC test circuit to about 0.003% for signals near ±full scale range for the 16-bit reference DAC. When testing an ADC for low level distortion (<-40dB) the same problem is encountered as with the DAC tester in that the distortion meter requires a minimum input signal of about 30mV. However, with small signals, the 16-bit reference DAC introduces a considerable amount of distortion that cannot be separated from the errors of the ADC under test. Therefore, simply amplifying the output of the low-pass filter is not the optimum solution. If we could amplify the digital signal being sent to the DAC, the DAC output would be near its full scale range, where the distortion is much less, and the

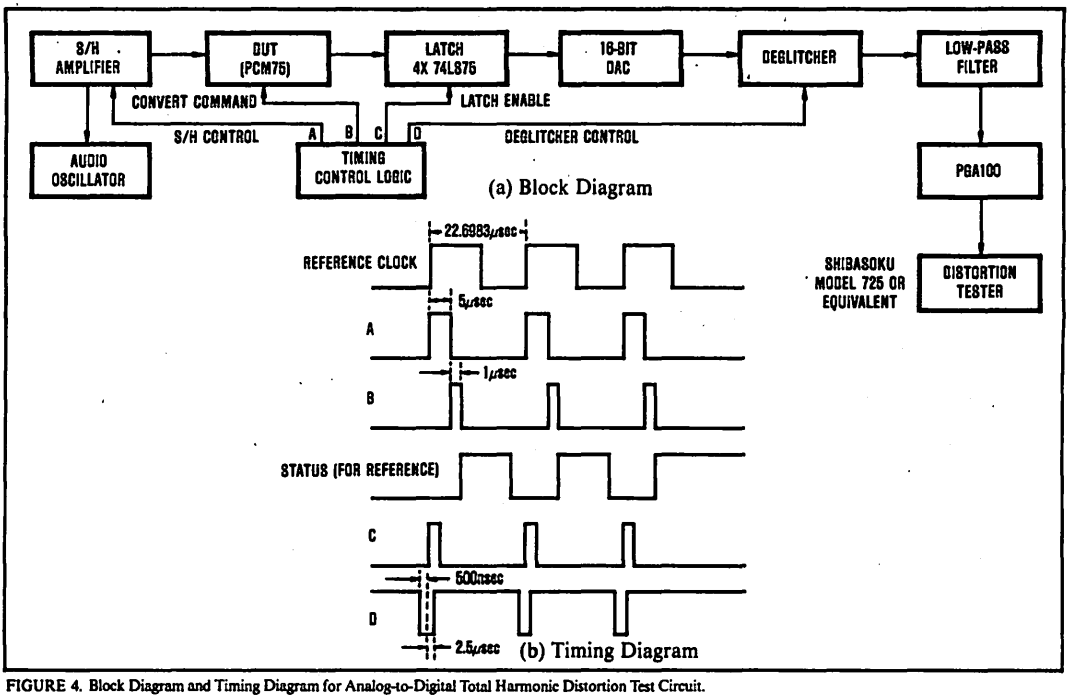


FIGURE 4. Block Diagram and Timing Diagram for Analog-to-Digital Total Harmonic Distortion Test Circuit.

output signal would be large enough for the distortion meter to read directly.

Let's consider the input code being presented to the DAC when a low level (<30mV) input signal is applied to the ADC under test. Except at the major carry, where the analog input signal passes through zero volts, only the 5 or 6 least significant bits (LSB's) are changing. The MSB is important because it indicates that the analog signal is either positive or negative, but bits 2 through 8 do not contain any significant information. If the lower 6 bits of the ADC output are connected to the more significant bits of the reference DAC input (connect bit 16 to bit 10, bit 15 to bit 9, ..., and bit 10 to bit 4) the digital output from the ADC is effectively amplified by about 36dB. Not only does this eliminate the need for another stage of amplification, but since the more significant bits of the reference DAC are much more accurate than the least significant bits, the effect of the DAC linearity errors on the overall distortion measurement will be greatly reduced. The implementation of this technique is shown in Figure 5.

A complete circuit implementation of a distortion test circuit for both DAC's and ADC's is shown in Figure 8.

Another important specification for both D/A and A/D converters in audio applications is differential linearity error (DLE). DLE is the deviation from an ideal 1LSB change from one adjacent analog output state to the next. This is particularly important at bipolar zero (or the "major carry") since excessive DLE at this point can cause audible crossover distortion for low level signals. The waveform in Figure 6(a) shows a -60dB output signal (±5mV at 400Hz) from a 16-bit DAC with more than

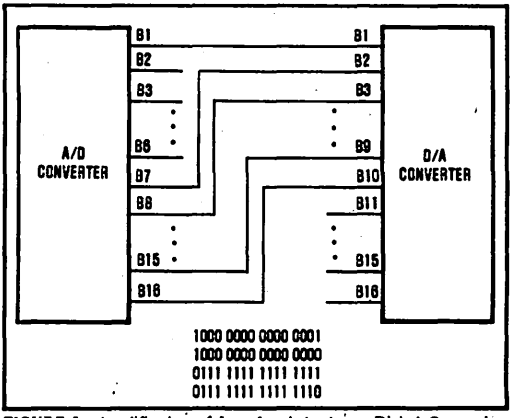


FIGURE 5. Amplification of Low Level Analog-to-Digital Output by Digitally Offsetting Reference Digital-to-Analog Converter.

3LSB's of DLE at bipolar zero. The discontinuities in the sine wave, measured at the output of the low-pass filter (see Figure 1), are just barely visible at the zero crossing points. The output signal is then amplified by 100 by the programmable gain amplifier and connected to the distortion meter where the fundamental component is removed with a notch filter.

The waveform in Figure 6(b) is the error signal from the distortion meter after a further amplification of 10dB. The effect of the excessive DLE at the major carry is clearly seen as large spikes in this waveform. Figure 8 displays the same waveforms for a 16-bit DAC with less than 1/4LSB of DLE at bipolar zero. The small errors seen in the error signal are primarily caused by the

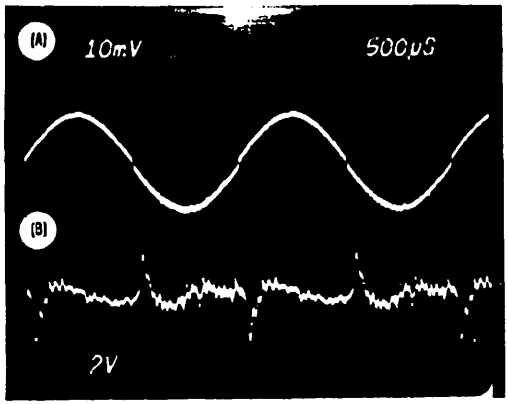


FIGURE 6. (a) −60dB Output Signal from a 16-Bit DAC with >3LSBs of DLE at Major Carry. (b) Amplified Error Signal Showing Large Discontinuities at Zero Crossing Points.

quantization uncertainty due to the finite resolution of the DAC. Excessive DLE error can usually be detected by a low level THD measurement (<-40dB), but a THD measurement near full scale will tend to "mask" this problem due to the averaging effect of the distortion meter. To ensure that this error will not present a problem, the DLE at bipolar zero should be specified.

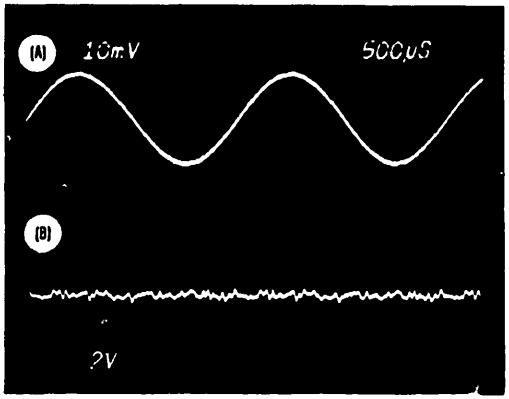


FIGURE 7. (a) −60dB Output Signal from a 16-Bit DAC with <1/4LSB DLE at Major Carry. (b) Amplified Error Signal.

The parameters of a data converter designed for audio applications should be stable over a moderately wide temperature range and over long periods of time to avoid undesirable periodic readadjustment. As mentioned previously, gain drift and offset drift, or minus full scale drift, are relatively unimportant in audio applications. Even a shift of 1% in these parameters, which is totally undesirable periodic readjustment. As mentioned previously, gain drift and offset drift, or minus full scale shift in the bipolar zero, or midscale point, can result in an audible difference in THD for low level signals. The important specifications for the PCM54, PCM55, 56 and PCM75, which were designed and specified for digital audio applications, are shown in Table II. The majority of the gain and offset drift in the the PCM54/55/56/75 is due to the drift of the internal reference zener diode. However, these products are designed so that the overall gain and offset drift due to the reference are in equal but opposite directions, resulting in a bipolar zero voltage that is virtually unaffected by variations in the reference voltage. Both the DLE and THD are dependent upon the matching and tracking of resistor ratios and upon matching and tracking of V_{BE} and h_{FE} of the current source transistors. These ratios are very stable with time and temperature and the circuits are designed so that any absolute shifts in these parameters have virtually no effect on the DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. In addition, the current density in these resistors is very low to further enhance their long-term stability. Actual life test data on the PCM54/55/56 after 1000 hours at +85°C indicates almost no perceptible shift in THD for both high and low level signals.

TABLE II. Important Specifications for the PCM75, PCM54, and PCM55, 56, Which Were Designed and Specified for Digital Audio Applications.

SPECIFICATION	PCM75KG (A/D)	PCM56 (D/A)	PCM 54/55 (A/D)	UNITS
Differential Linearity Error at Bipolar Zero	±0.0015	±0.001	±0.001	% of FSR
Total Harmonic Distortion				
V_O = ±FS at F = 400Hz				
14-Bit Resolution	0.006			%
16-Bit Resolution	0.004	0.002	0.002	%
V_O = ±15dB at f = 400Hz				
14-Bit Resolution	0.025			%
16-Bit Resolution	0.015			%
V_O = −20dB at f = 400Hz				
16-Bit Resolution	———	0.02	0.02	%
V_O = −60dB at f = 400Hz				
14-Bit Resolution	———			%
16-Bit Resolution	———	2.0	2.0	%
Conversion Time				
14-Bits	15			µsec
16-Bits	17			µsec
Settling Time				
20V Step		1.5	3	µsec

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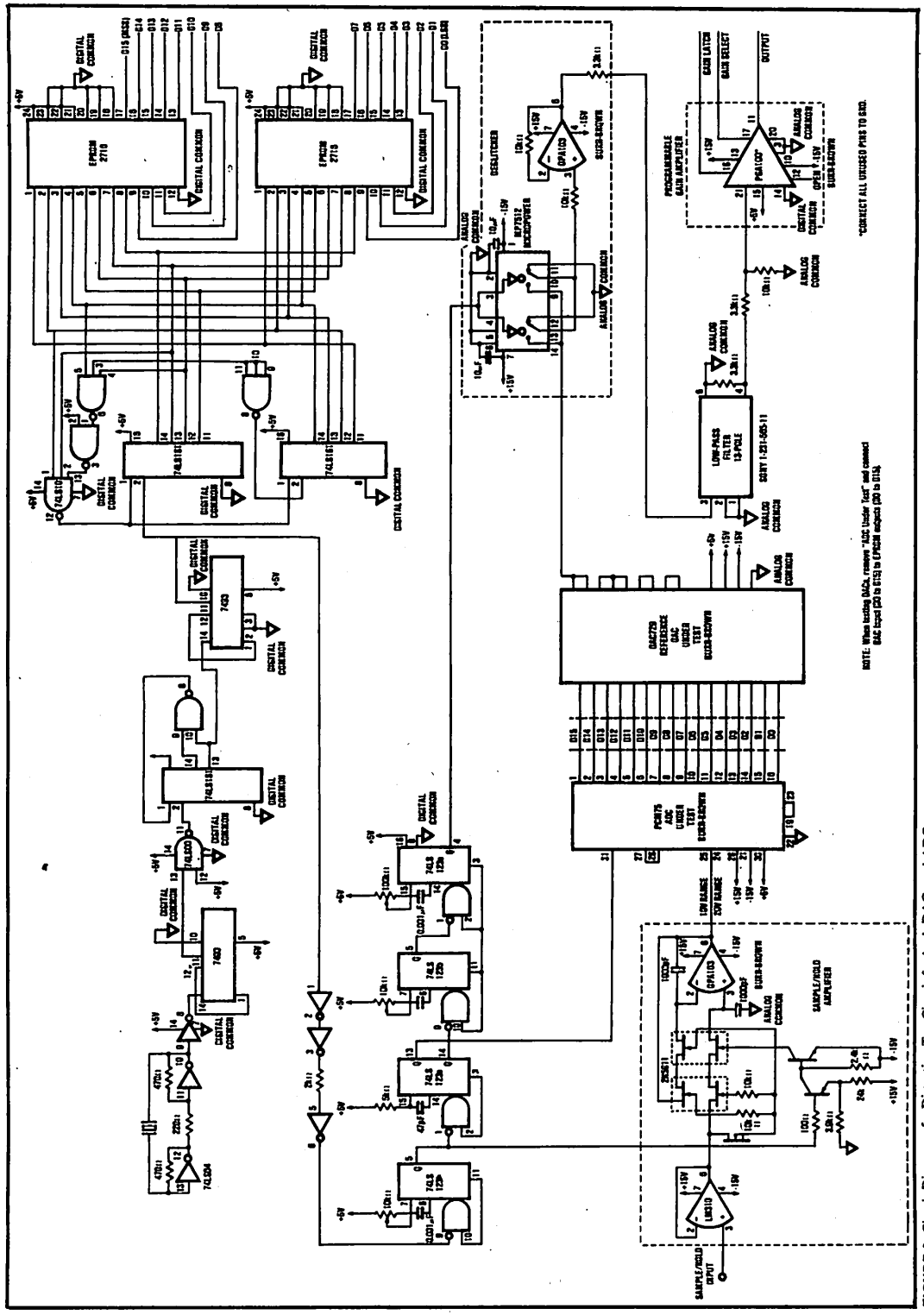

FIGURE 8. Circuit Diagram of a Distortion Test Circuit for both DACs and ADCs.

DYNAMIC TESTS FOR A/D CONVERTER PERFORMANCE

This article describes useful theory and techniques for evaluating the dynamic performance of A/D converters. Four techniques are discussed: (1) beat frequency, (2) histogram analysis, (3) sine wave curve fitting, and (4) discrete finite Fourier transform.

The key to confidence in the quality of a waveform recorder is assurance that the analog-to-digital converter (ADC) encodes the signal without degrading it. Dynamic tests that cover the frequency range over which the converter is expected to operate can provide that assurance. The results of the dynamic tests give the user a model of resolution versus frequency for the recorder. More elaborate models of failure mechanisms can be obtained by varying the conditions of the tests.

All of the dynamic tests used for the 5180A Waveform Recorder use sine waves as stimulus. Sine waves were chosen primarily because they are the easiest to generate in practice at the frequencies of interest with adequate fidelity. While it may be possible to generate a square wave, for example, whose function is known to the 10-bit resolution of the 5180A, no square wave generators exist that can guarantee the same waveshape to 10-bit resolution at 10MHz from unit to unit. Another motivation for choosing a sine wave stimulus is the simple mathematical model a sine function provides for analysis. This benefit greatly simplifies the algorithms used for data analysis.

Four dynamic tests for waveform recorder characterizations are presented here: beat frequency testing,[1] histogram analysis,[2] sine wave curve fitting,[3,4] and discrete finite Fourier transform.[5] The last three tests operate in the same way. A sine wave source is supplied to the waveform recorder and one or more records of data are taken. A computer is then used to analyze the data. The tests differ primarily in the analysis algorithms and consequently in the sort of errors brought to light. Critical to the success of these tests is the purity of the sine wave source. Synthesized sources are necessary to provide the short-term and long-term stability required by the dynamic range of the ADC. Passive filters (a six-pole elliptical filter is used for 5180A tests) are required to eliminate harmonic distortion from the source.

These tests provide the most stressful conditions for the ADC with the input signal amplitude at full scale. Generally speaking, nonlinear effects increase more quickly than the signal level increases because of the nonideal large-signal DC behavior of the ADC components and the higher slew rates large amplitudes imply.

BEAT FREQUENCY TESTING

The beat frequency and envelope tests are qualitative tests that provide a quick, simple visual demonstration of ADC dynamic failures. An input frequency is selected that provides worst-case range changes and maximal input slew rates that the ADC is expected to see in use. The output is then viewed on a display in real time.

The name "beat frequency" describes the reasoning behind the test. The input sinusoid is chosen to be a multiple of the sample frequency plus a small incremental frequency (Figure 1). Successive samples of the waveform step slowly through the sine wave as a function of the small difference or beat frequency (Figure 2). Ideally,

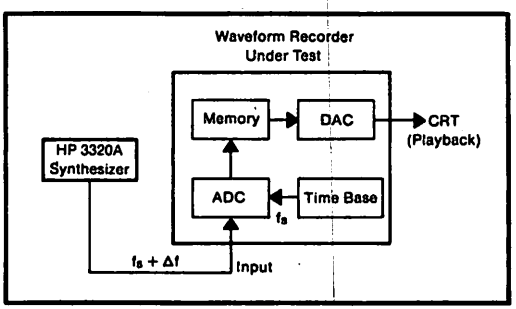

FIGURE 1. Beat frequency test setup.

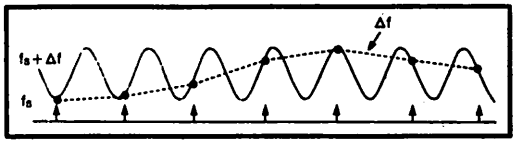

FIGURE 2. When the input frequency is close to the sample rate f_s, the encoded result is aliased to the difference or beat frequency Δf.

the multiplicative properties of sampling would yield a sine wave of the beat frequency displayed on the waveform recorder's CRT. Errors can be seen as deviations from a smooth sine function. Missing codes, for example, appear as local discontinuities in the sine wave. The oversize codes that accompany missing codes are seen as widening in the individual codes appearing on the sine wave. By choosing an arbitrarily low beat frequency, a slow accurate DAC may be used for viewing the test output. For best results, the upper limit on the beat frequency choice is set by the speed with which the beat frequency walks through the codes. It is desirable to have one or more successive samples at each code. This

alleviates the settling constraint on the DAC and ensures that the display covers all possible code failures. For a 20MHz sample rate and a 10-bit ADC, this implies a 3kHz maximum beat frequency for a minimum of one sample per code bin.

Although the usual input frequency for a beat frequency test is near the sample rate, the analog bandwidth of the ADC may be measured by setting the carrier to a number of different multiples of the sample rate. The band limit is observed as a rolloff in amplitude as the carrier frequency is increased.

The envelope test differs from the beat frequency test in the choice of input frequency that the ADC encodes. Instead of a multiple of the sample frequency, an input frequency near one-half the sample rate is used. Now the ideal output is two out-of-phase sine waves at the beat frequency (Figure 3). This means that successive samples

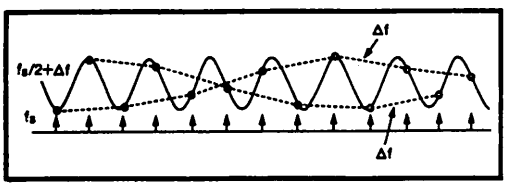

FIGURE 3. When the input frequency is near one-half the sample rate, the envelope of the difference frequency results.

can be at the extreme ends of the ADC range, which is useful for examining slew problems that might not appear when successive samples are at adjacent codes. To avoid placing the same stress on the DAC used for display, a bank of D flip-flops removes every other sample before the data arrives at the DAC. Thus only one phase of the beat frequency remains.

Figure 4 shows 5180A beat frequency test results for a 10.0031MHz input sine wave sampled at 10MHz. For comparison, Figure 5 shows a 10.0031MHz sine wave being sampled at 10MHz by a commercially available 8-bit, 20MHz ADC.

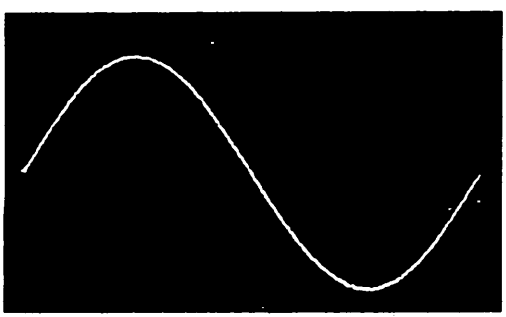

FIGURE 4. A beat frequency display produced by the 5180A Waveform Recorder with a 10.0031MHz input frequency and a 10MHz sample rate. The smooth sine wave indicates freedom from dynamic errors.

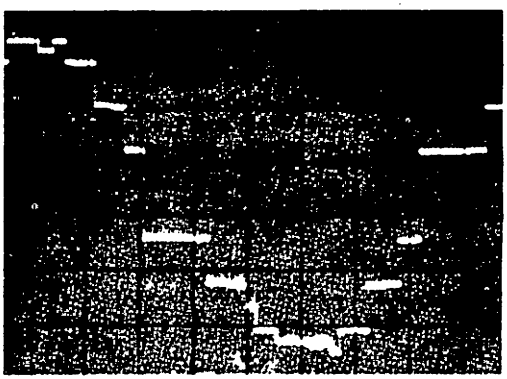

FIGURE 5. A beat frequency display for a commercially available 10MHz, 8-bit ADC with a 10.0031MHz input.

HISTOGRAM TESTING

A sine-wave-based histogram test provides both a localized error description and some global descriptions of the ADC. Using the histogram test, it is possible to obtain the differential nonlinearity of the ADC, to see whether any missing codes exist at the test frequency, and to get a measure of gain and offset at the test frequency. Of the sine-wave-based tests presented here, the histogram test yields the best information about individual code bin size at an arbitrary frequency.

A statistically significant number of samples of the input sinusoid are taken and stored as a record (Figure 6). The frequency of code occurrence in the record is then plotted as a function of code. For an ideal ADC, the shape of the plot would be the probability density function (PDF) of a sine wave (Figure 7) provided that the input and sample frequencies are relatively independent. The PDF of a sine wave is given by:

$$p(V) = \frac{1}{\pi\sqrt{A^2-V^2}}$$

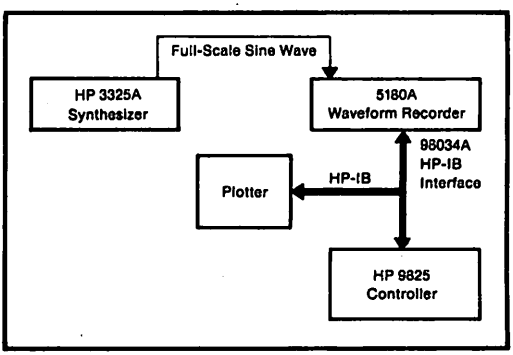

FIGURE 6. Setup for histogram test.

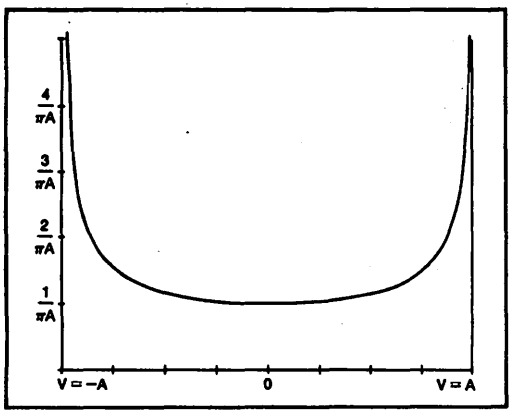

FIGURE 7. Sine wave probability density function.

where A is the sine wave amplitude and V is the independent variable (voltage). For a real ADC, fewer than the expected number of occurrences for a given code bin indicates that the effective code bin width is smaller than ideal at the input frequency.* No occurrences indicate that the code bin width is zero for that input. A greater-than-expected number of occurrences implies a larger-than-ideal code bin width.

What is a statistically significant number of samples? We can determine significance from probability theory. For a given input PDF and record size, each bin of an ideal ADC has an expected number of occurrences and a standard deviation around that expectation. The confidence that the number of occurrences is close to the expectation is equal to the probability that the occurrences fall within the appropriate number of standard deviations. The ratio of the standard deviation to the expectation (and thus the error for a given confidence) decreases with more samples. To get the confidence for the entire range, the probabilities for all codes lying within the desired error are multiplied together.

For an ideal 10-bit ADC, 100,000 samples would give us a 12% confidence that the peak deviation from the input PDF is less than 0.3LSB and a 99.9% confidence that the peak deviation is less than 0.5LSB. The notion of confidence relies on the input's being a random process. We can model the sine wave input as random process only if the input and sample frequencies are relatively independent.

The specification of greatest interest that can be calculated using the histogram test is differential nonlinearity. Differential nonlinearity is a measure of how each code bin varies in size with respect to the ideal:

$$\text{Differential nonlinearity} = \frac{\text{actual P (nth code)}}{\text{ideal P (nth code)}} - 1$$

where actual P(nth code) is the measured probability of occurrence for code bin n, and ideal P(nth code) is the ideal probability of occurrence for code bin n. The code bin number n goes from 1 to 2^N, where N is the number of ADC bits. Using the probability of occurrence eliminates dependence on the number of samples taken. To calculate the probability for each code in the actual data record, the number of occurrences for each code is divided by the number of samples in the record. The ideal probability of occurrence is what an ideal ADC would generate with a sine wave input. For each code bin, this is the integral of the probability density function of a sine wave over the bin:

$$P(n) = \frac{1}{\pi}\left[\sin^{-1}\left(\frac{B(n-2^{N-1})}{A2^N}\right) - \sin^{-1}\left(\frac{B(n-1-2^{N-1})}{A2^N}\right)\right]$$

where n is the code bin number, B is the full-scale range of the ADC, and N is the number of ADC bits. To avoid large differences in code probability caused by the sinusoid cusp, a sine wave amplitude A is chosen that slightly overdrives the ADC.

A judicious choice of frequency for the input sinusoid in this test is necessary for realistic test results. An input frequency that is a submultiple of the sample frequency violates the relative independence criterion and will result in sampling of the same few codes each input cycle. Using an input frequency that has a large common divisor with the sample frequency generates similar problems since the codes repeat after each cycle of the divisor frequency. Ideally the period of the greatest common divisor should be as long as the record length.

A 5180A histogram is shown in Figure 8 for an input sine wave at 9.85MHz. For comparison, Figure 9 shows data from a commercially available, 8-bit 20MHz ADC for an input sine wave at 9.85MHz, while Figure 10 shows data from an 8-bit, 100MHz ADC taken at 9.85MHz.

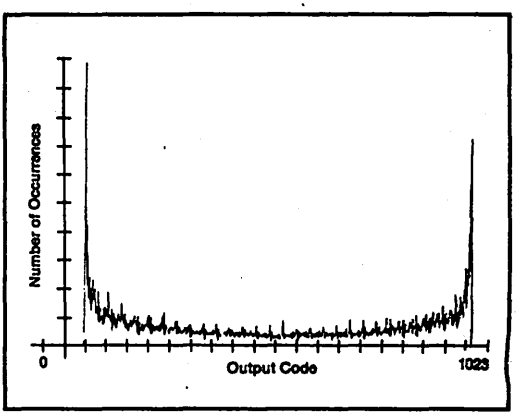

FIGURE 8. A 100,000-sample histogram for a 5180A with a 9.85MHz sine wave input. All discontinuities are less than 1LSB.

*Histogram testing can be thought of as a process of sampling and digitizing the input signal and sorting the digitized samples into bins. Each bin represents a single output code and collects samples whose values fall in a specific range. The number of occurrences or samples collected in each bin varies according to the input signal. If N is the number of ADC bits, there are 2^N bins. Ideally, if B is the full-scale range of the ADC in volts, each bin corresponds to a range of sample sizes covering $B/2^N$ volts. In a real ADC, the bins may not all have the same width.

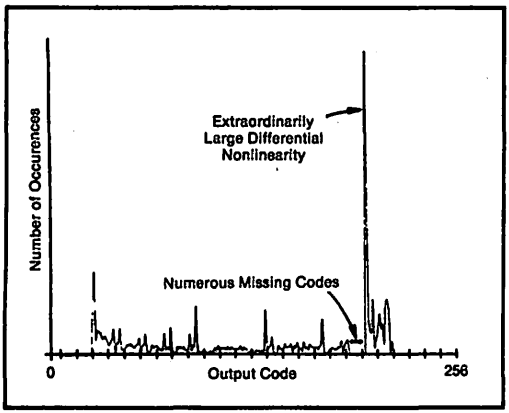

FIGURE 9. A 100,000-sample histogram plot for a commercially available 20MHz, 8-bit ADC with a 9.85MHZ input. Large differential nonlinearities and numerous missed codes are apparent.

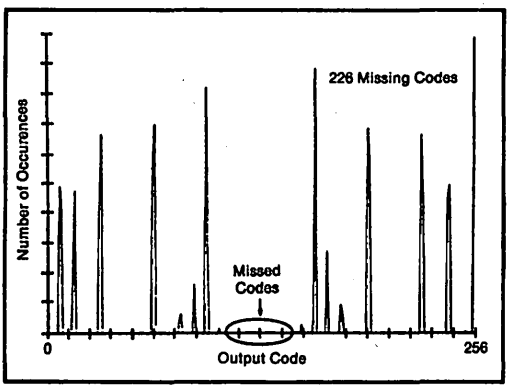

FIGURE 10. A 100,000-sample histogram plot for a 100MHz, 8-bit ADC with a 9.85MHz input sampled at 20MHz. Extremely large differential nonlinearities and numerous missed codes are apparent.

CURVE FITTING

The curve-fit test is a global description of the ADC. This means that the errors measured by the test are averaged to give a general measurement of the ADC transfer function. The result of this test is a figure of merit called the number of effective bits for the ADC. The effective bit number is a general measure of how much an ADC's nonlinearity has impaired its usefulness at a given frequency.

The number of effective bits is obtained by analyzing a record of data taken from a sine wave source (Figure 11). The analysis consists of generating a sine wave in software that is a best fit to the data record. Any difference between the data record and the best-fit sine wave is assumed to be error (Figure 12). The standard deviation of the error thus calculated is compared to the error an ideal ADC of the same number of bits might generate. If the error exceeds the ideal, the number of effective bits exhibited by the ADC is less than the number of bits it digitizes. Errors that cause degradation in this test are nonlinear effects such as harmonic distortion, noise, and aperture uncertainty. Gain, offset, and phase errors do not affect the results since they are ignored by the curve-fit process.

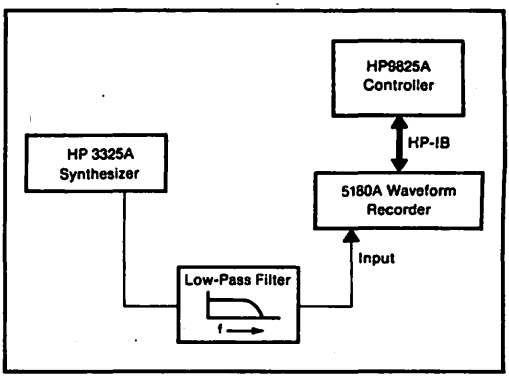

FIGURE 11. Setup for the curve-fit test and the discrete finite Fourier transform (DFT) test.

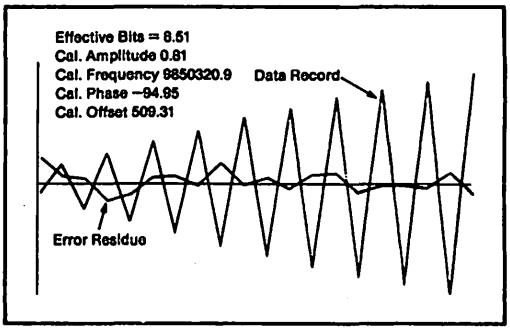

FIGURE 12. The first 20 points of the curve-fit data record and the error residue from a fitted sine wave.

The number of effective bits is computed using expressions for average errors as follows:

$$\text{Effective bits} = N - \log_2\left(\frac{\text{actual rms error}}{\text{ideal rms error}}\right)$$

where N is the number of ADC bits. The ideal rms error is not actually computed for the input waveform, but is assumed to be the quantization noise exhibited by an ideal ADC with a uniform-probability-density (UPD) input such as a perfect triangle wave. The ideal error is found from the expectation of squared error for a rectangular distribution. A rectangular distribution is used since that represents a UPD taken over an ideal code bin. The result thus obtained is:

$$\text{Ideal rms error} = \frac{Q}{\sqrt{12}}$$

where Q is the ideal code bin width. Although the input sine wave is not a UPD function, the UPD assumption is still valid since it is locally applied over each code bin. The deviation from a UPD over each code bin is very

small, so the errors in using sine waves to approximate UPD inputs are negligible.

The actual rms error is simply the square root of the sum of the squared errors of the data points from the fitted sine wave. The actual rms error is given by:

$$E = \sum_{k=1}^{m} [x_k - A\cos(\omega t_k + P) - C]^2 \quad (1)$$

where E is the actual rms error, x_k and t_k are the data points, m is the number of data points in the record, and the fitted sine wave parameters are amplitude A, frequency ω, phase P, and offset C.

Equation 1 is also used to find the best-fit sine wave by minimizing the error E. The error is minimized by adjusting the fit parameters: frequency, phase, gain, and offset. This is done by taking the partial derivative of E in equation 1 with respect to each of the four parameters. The error minimum occurs when all of the derivatives are equal to zero. This gives the four simultaneous equations:

$$\sum_{k=1}^{m} x_k \cos(\omega t_k + P) = A\sum_{k=1}^{m} \cos^2(\omega t_k + P) + C\sum_{k=1}^{m} \cos(\omega t_k + P) \quad (2)$$

$$\sum_{k=1}^{m} x_k = A\sum_{k=1}^{m} \cos(\omega t_k + P) + nC \quad (3)$$

$$\sum_{k=1}^{m} x_k t_k \sin(\omega t_k + P) = A\sum_{k=1}^{m} t_k \cos(\omega t_k + P)\sin(\omega t_k + P) + C\sum_{k=1}^{m} t_k \sin(\omega t_k + P) \quad (4)$$

$$\sum_{k=1}^{m} x_k \sin(\omega t_k + P) = A\sum_{k=1}^{m} \cos(\omega t_k + P)\sin(\omega t_k + P) + C\sum_{k=1}^{m} \sin(\omega t_k + P) \quad (5)$$

Equations 2 and 3 result from gain and offset adjustments. These are substituted into the other two equations, 4 and 5, giving two nonlinear equations:

$$\frac{\sum_{k=1}^{m} (x_k - \bar{x}) t_k \sin(\omega t_k + P)}{\sum_{k=1}^{m} (x_k - \bar{x}) \cos(\omega t_k + P)} = \frac{\sum_{k=1}^{m} [\cos(\omega t_k + P) - \bar{a}] t_k \sin(\omega t_k + P)}{\sum_{k=1}^{m} [\cos(\omega t_k + P) - \bar{a}] \cos(\omega t_k + P)} \quad (6)$$

$$\frac{\sum_{k=1}^{m} (x_k - \bar{x}) \sin(\omega t_k + P)}{\sum_{k=1}^{m} (x_k - \bar{x}) \cos(\omega t_k + P)} = \frac{\sum_{k=1}^{m} [\cos(\omega t_k + P) - \bar{a}] \sin(\omega t_k + P)}{\sum_{k=1}^{m} [\cos(\omega t_k + P) - \bar{a}] \cos(\omega t_k + P)} \quad (7)$$

$$\text{Where } \bar{a} = \sum_{k=1}^{m} \cos(\omega t_k + P)$$

These are solved iteratively to give values for the parameters. The difference between the right and left sides of equation 6 is defined as error parameter R and the difference between the right and left sides of equation 7 is defined as error parameter S. An approximation algorithm using a first-order Taylor series expansion drives R and S to zero. This approximation algorithm requires an initial guess for frequency and phase close to the solution to ensure convergence to the best-fit sine wave. For frequency, the frequency of the generator output in Figure 11 is used as a guess. For phase, a guess is based on an examination of the data record by a software routine.

Although the result of this process is a single figure of merit, some enlightenment can be gained about the error components in the ADC by varying the test conditions. White noise produces the same degradation regardless of input frequency or amplitude. That is, the error term in equation 1 is independent of test conditions for this sort of error. Another way of identifying noise in this test is by the randomness in the error residue, or the difference between the best-fit sine wave and the data taken.

Aperture uncertainty is identifiable because it generates an error that is a function of input slew rate. When this is the dominant error causing a low number of effective bits, the number of effective bits will vary linearly with both input frequency and amplitude. If the input waveform is sampled only at points of constant slew rate, such as zero crossings, then the aperture uncertainty corresponds to the amount that the effective bits decline as a function of slew rate.

Harmonic distortion is usually a nonlinear function of amplitude and frequency. Its distinguishing characteristic is the presence of the harmonics (or aliased harmonics if the fundamental is close to the Nyquist frequency) in the error residue. The amplitudes of the harmonics can be extracted by fitting the error residue with best-fit sine waves of the important harmonic frequencies. The impact of noise and aperture uncertainty in the presence of large distortion errors can be assessed by effective bit values and error residues with the fitted harmonics removed.

The greatest pitfall in the curve-fit test is using an input frequency that is a submultiple of the sample frequency. Since the same codes are sampled at exactly the same voltage each cycle, the locally uniform probability distribution assumption is violated. In the worst case, a submultiple of one-half, the quantization error would not be measurable at all. From a practical standpoint, this also defeats the global description of the test by sampling only a handful of codes.

Another potential pitfall is lack of convergence of the curve-fit algorithm. There are a few occasions where this can become a problem, such as when the data is very poor or the computational resolution is inadequate.

Figure 12 shows the error plot for a 5180A curve-fit test taken at a 9.85MHz input frequency. The number of effective bits associated with this error is 8.51.

FFT TESTING

The fast Fourier transform (FFT) is used to characterize an ADC in the frequency domain in much the same way that a spectrum analyzer is used to determine the linearity of an analog circuit. The data output for both techniques is a presentation of the magnitude of the Fourier spectrum for the circuit under test. Ideally the spectrum is a single line that represents the pure sine wave input and is devoid of distortion components generated by the circuit under test. There are, however, significant differences between the spectrum analyzer and ADC spectra

because of the sampling operation of the ADC.

The Fourier transform of a signal x(t) that is continuous for all time is defined as

$$X(f) = \int_{-\infty}^{\infty} x(t)e^{-i2\pi ft}dt$$

and includes the amplitude and phase of every frequency in x(t). The Fourier transform cannot be used in this form for an ADC, however, because x(t) is only digitized at a finite number of points, M, spaced Δt apart. Instead, the discrete finite transform (DFT) must be used. It is defined as

$$XD(f) = \sum_{m=0}^{M-1} x(m\Delta t)e^{-i2\pi f(m\Delta t)}\Delta t$$

There are significant differences between X(f) and XD(f). While X(f) has infinite spectral resolution, XD(f) has a discrete frequency resolution of $\Delta f = 1/m\Delta t$ because of the finite number of points in the data record. The finite record size also accounts for another difference between X(f) and XD(f) whenever a nonintegral number of cycles of X(t) is contained in the record. Since the DFT assumes that the record repeats with a period of $M\Delta t$ (to satisfy the Fourier transform condition that x(t) be continuous for all time) sharp discontinuities at the points where the start of one record joins the end of the preceding record cause the spectral components of X(f) to be spread or smeared in XD(f).

The smearing, called leakage, can be explained as follows. The finite record size of x(t) can be considered the consequence of multiplying x(t) by a rectangular function having unity amplitude during the time period $M\Delta t$ that the record is acquired and zero amplitude elsewhere. Since multiplication of two functions in one domain (time, in this case) is equivalent to convolution in the other, the spectrum of XD(f) is derived by convolving X(f) with W(f), the Fourier transform of the rectangular function. W(f) is the familiar sinx/x function (see Figure 13 for |W(f)|), consisting of a main lobe surrounded by a series of sidelobes whose amplitudes decay at a 6dB-per-octave rate. It is these sidelobes that are responsible for leakage. Even if the spectrum of X(f) is a single line, the sidelobes of W(f) during the convolution smear the energy in the single line into a series of spectral lines spaced $1/M\Delta t$ apart whenever the frequency of x(t) is not an integral multiple of $1/M\Delta t$.

Leakage can be reduced by multiplying the data in the record by a windowing function that weights the points in the center of the record heavily while smoothly suppressing the points near the ends. Many different windowing functions exist that offer various tradeoffs of amplitude resolution versus frequency resolution. A function commonly used with sine waves is the Hanning window, defined by $|(1/2)(1-\cos 2\pi t/M\Delta)|$. Notice in Figure 13 that both the window and its derivative approach zero at the two ends of the record and that the transform's main lobe is twice as wide as that of the rectangular function, while the amplitudes of the sidelobes decay by an additional 12dB per octave. The reduced level of the sidelobes reduces leakage, but the wider main lobe limits the ability to resolve closely spaced frequencies. Furthermore, the shape of the main lobe can attenuate the spectral amplitudes of X(f) by as much as 1.5dB. However, for the DFT testing to be described here, the Hanning window was selected as a good compromise between frequency and amplitude resolution.

The third difference between the spectra of X(f) and XD(f) is the limited range of frequencies displayed for XD(f). The sampling process causes the two-sided spectrum of X(f), symmetrical about the origin, to be replicated as the sampling frequency f_s and at all of its harmonics. If X(f) contains components that exceed $f_s/2$, then these components are folded back, or aliased, onto spectral lines below f_s, causing aliasing errors. The frequency $f_s/2$ is sometimes called the Nyquist frequency, referring to the Nyquist criterion, which requires the sampling rate to be twice the highest frequency present

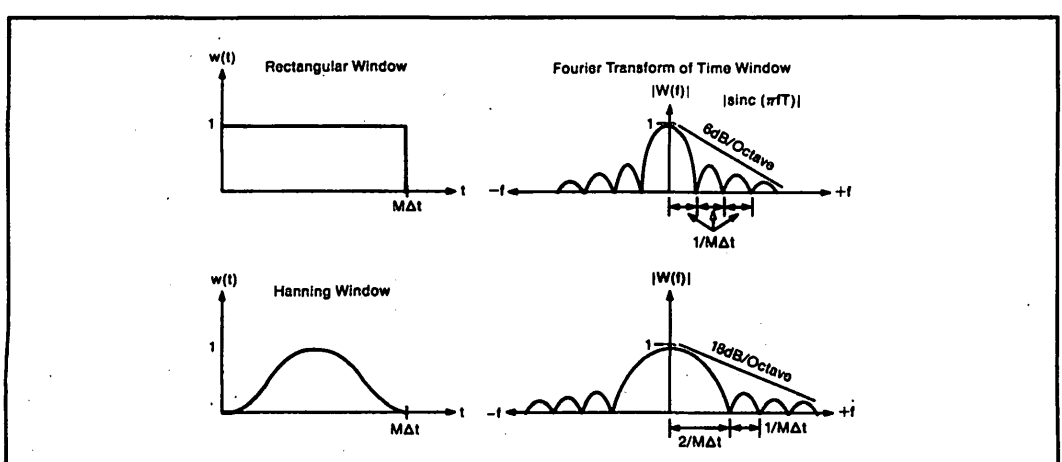

FIGURE 13. Time-domain and frequency-domain representations of rectangular and Hanning windows.

in the input signal to define the waveform uniquely. The result is that the spectrum of XD(f) is displayed only from DC to $f_s/2$ and the maximum input frequency must be limited to less than $f_s/2$ to avoid aliasing.

Figure 14 presents the magnitude of the spectra derived from the DFT for perfect 10-bit and 6-bit ADCs given a pure sinusoidal input. Useful information about the ADCs' performance can be derived from three features of the spectra: the noise floor, the harmonic level, and the spurious level.

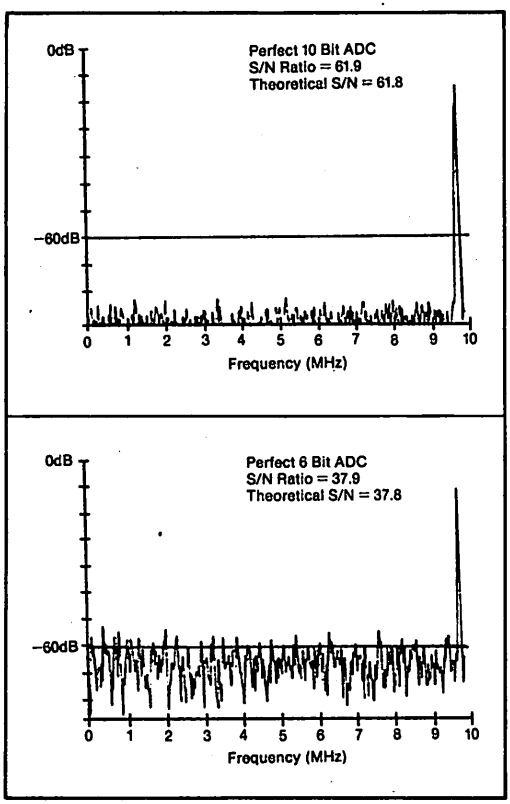

FIGURE 14. FFT plots for 0.85MHz data quantized by perfect 10-bit (top) and 6-bit (bottom) ADCs. The signal-to-noise ratio computed in each case agrees closely with the theoretical value of 6N + 1.8dB where N is the number of ADC bits.

Two classes of noise sources determine the level of the noise floor. The first is called quantization noise. This is the error, bounded by $\pm 1/2$LSB, that is inherent in the quantization of the input amplitude into discrete levels. As can be seen in Figure 14, even ideal ADCs have noise floors determined by quantization noise. The higher the number of bits, the smaller the error bound and, therefore, the lower the noise floor.

All real-life ADCs have noise floors that are higher than that solely from quantization noise. The second class of noise source includes wideband noise generated within the ADC, along with other sources. In a parallel-ripple ADC, for example, such things as misadjustment between the first-pass and second-pass ranges (exceeding the redundancy range) or inadequate DAC settling can cause localized code errors or differential nonlinearities in the ADC's status transfer function. Furthermore, localized code errors can increase in amplitude and in the number of codes affected under dynamic input conditions. Aperture jitter is another major source of dynamic error; the magnitude of this localized code error is dependent upon the slew rate of the input at the time of sampling. Each of these localized code errors can be modeled as a sharp discontinuity in the time domain that when transformed into the frequency domain results in a broad spectrum that raises the height of the noise floor above that caused by quantization noise alone.

The second feature of the DFT-derived spectrum that indicates an ADC's level of dynamic performance is the harmonic content. Static and dynamic integral nonlinearities cause curvature in the ADC's transfer function. If the input frequency f_{in} is much lower than the Nyquist freqency ($f_s/2$), then the harmonic components will be in the expected locations: $2f_{in}$, $3f_{in}$, etc. If, on the other hand, the harmonics of f_{in} are greater than $f_s/2$, then these frequencies will be aliased onto components below $f_s/2$. Take, for instance, a 20-megasample-per-second (f_s) ADC with an input of 9.85MHz. The second harmonic at 19.7MHz is aliased to 0.3MHz, the third harmonic at 29.55MHz is aliased to 9.55MHz, the fourth at 39.4MHz is aliased to 0.6MHz, and so on.

Care must be exercised in selecting the input frequency for the DFT test. An incorrectly chosen frequency can alias one of its harmonic components on to the fundamental and thereby understate the harmonic distortion (in the example above, an input of exactly 5MHz would place the third harmonic at the fundamental frequency). The input frequency should be chosen so that the harmonics are far enough away to be easily resolvable from the fundamental, whose energy has been spread into several adjacent bins ($1/M\Delta t$ locations) by the Hanning window. This accounts for the 0.15MHz offset from 10MHz used in the example of Figure 14.

The third feature of the DFT-based spectrum that is indicative of the ADC's level of dynamic performance is the spurious content. Spurious components are spectral components that are not harmonically related to the input. For example, a strong signal near the ADC may contaminate the ADC's analog ground somehow and thereby appear in the spectrum. The nearby signal will not only appear as itself, but because of nonlinearities within the ADC, can combine with the input signal to form sum and difference terms resulting in intermodulation distortion.

The combined effects of noise floor, harmonic distortion and spurious errors are reflected in the ADC's rms signal-to-noise ratio, which can be derived from the DFT magnitude spectrum. The signal energy is determined by summing the energy in all the bins associated with the fundamental. The noise energy is the sum of the energy in all other bins. By taking the logarithm of the ratio of signal energy to noise energy and multiplying by

20, the signal-to-noise ratio for the ADC can be calculated. An ideal N-bit ADC having quantization noise only is theoretically known to have a signal-to-noise ratio equal to (6N + 1.8)dB, which sets an upper bound. A signal-to-noise ratio below this ideal limit is indicative of errors of all types that the ADC produces.

The FFT test setup is presented in Figure 11. A full-scale sine wave of a properly chosen frequency is applied to the ADC under test. The low-pass filter ensures a spectrally pure input. A 1024-point record sampled at the maximum sampling rate is then taken and given to the computer, which calculates the DFT using an FFT algorithm. The spectral magnitude is plotted as a function of frequency.

Figure 15 shows the graphical outputs for the 5180 for full-scale sine wave input at 0.95MHz and 9.85MHz. As might be expected, the distortion increases with increasing frequency. Harmonic and spurious components are typically better than −60dBc below 1MHz and −54dBc at 9.85MHz. The latter spectrum at 9.85MHz is the frequency-domain representation for one of the most demanding tests of an ADC, called the envelope test, which was described earlier.

Figure 16 presents, for comparison, the test results for commercially available digitizers: a 20-megasample-per-second, 8-bit ADC and a 100-megasample-per-second, 10-bit ADC with a full-scale, 9.85MHz sine wave input, sampled at 20 megasamples-per-second. The numerous large harmonic components, both odd and even, are indicative of severe harmonic distortion errors resulting from integral nonlinearity in the transfer functions of both of these ADCs.

A rule of thumb has evolved that uses the DFT-based spectrum as a quick overview of an N-bit ADC's dynamic performance. If all harmonic and spurious components are at least 6N dB below the full-scale amplitude of the fundamental, then the ADC is performing satisfactorily, since each error component has a peak-to-peak amplitude smaller than an LSB. If, on the other hand, harmonic or spurious components are less than 6N dB down, or if the noise floor is elevated, then other tests can be performed that are better at isolating the particular integral and differential nonlinearity errors. In particular, the FFT test an be followed by the histogram test or the beat frequency test (or envelope test), as conditions warrant.

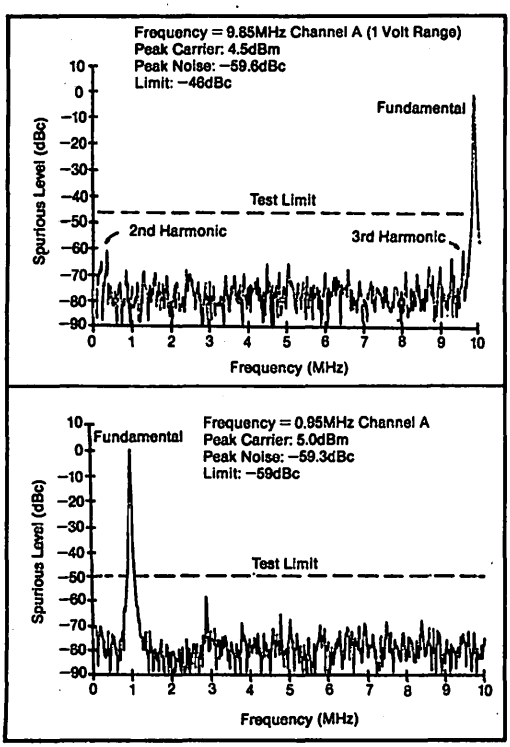

FIGURE 15. DFT plots for the 5180A with input frequencies of 9.85MHz (top) and 0.95MHz (bottom). The low harmonic distortion indicates very low integral nonlinearity.

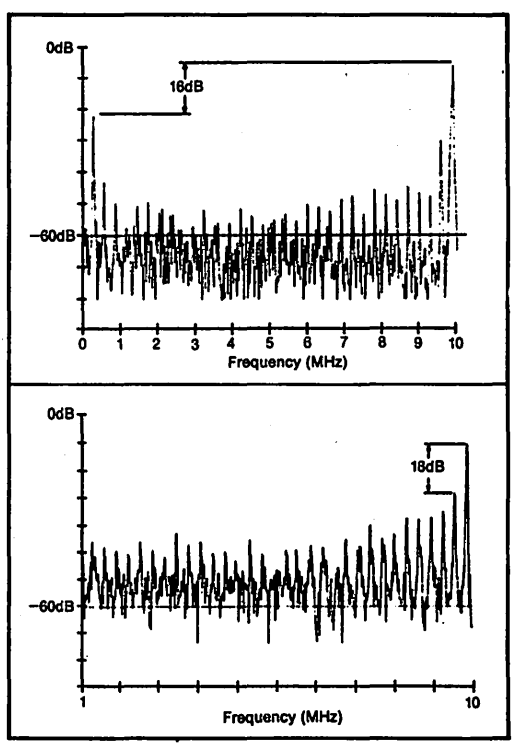

FIGURE 16. DFT plots for a 20MHz, 8-bit ADC (top) and a 100MHz, 8-bit ADC (bottom). Full-scale input sine waves at 9.85MHz were sampled at a rate of 20MHz. The high levels of harmonic distortion indicates severe integral nonlinearities.

CONCLUSION

The four sine-wave-based ADC tests described provide information about the quality of any recorder. The tests may be used to isolate specific failures, even at high speed and fine resolution (Figure 17). The tests are simple to run, requiring only a synthesized generator and an HP-IB computer.

Error	Histogram	DFT	Sine Wave Curve-Fit	Beat Frequency Test
Differential Nonlinearity	Yes—shows up as spikes	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Missing Codes	Yes—shows up as bins with 0 counts	Yes—shows up as elevated noise floor	Yes—part of rms error	Yes
Integral Nonlinearity	Yes (could be measured directly with a highly linear ramp waveform)	Yes—shows up as harmonics of fundamental aliased into baseband	Yes—part of rms error	Yes
Aperture Uncertainty	No—averaged out. Can be measured with "locked" histogram	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Noise	No—averaged out. Can be measured with "locked" histogram	Yes—shows up as elevated noise floor	Yes—part of rms error	No
Bandwidth Errors	No	No	No	Yes—used to measure analog bandwidth
Gain Errors	Yes—shows up in peak-to-peak spread of distribution	No	No	No
Offset Errors	Yes—shows up in offset of distribution average	No	No	No

FIGURE 17. Summary of the errors exposed by the dynamic tests.

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SETTLING TIME

One of the most difficult quantities to measure properly is settling time. This parameter becomes even more difficult when extremes in resolution or time are encountered. Digital-to-analog converters with 12-bit resolution are commonplace today and settling times of under 50nsec are claimed by numerous manufacturers. Operational amplifiers with 100nsec settling times are available from several suppliers. Determining the performance of these components can become quite a challenge if settling time is to be measured accurately without the test circuit and the accompanying instrumentation interferring with the measurement. The accurate determination of settling time is important because it can be one of the limiting factors that determines the throughput rate of the system. Many designers develop their own high speed analog-to-digital converters when it is difficult to purchase one to suit their needs. Among the important components that are needed for the design are sure to be operational amplifiers and a digital-to-analog converter (DAC). A clear determination of the settling performance of these devices is of critical importance.

There are many different ways to measure settling time. Techniques and circuits are shown and discussed that enable the accurate measurement of DAC's, operational amplifiers, and arbitrary waveforms. The article will build from the straightforward method of measuring settling time by use of an oscilloscope towards a technique which lends itself to automatic data logging of fast waveforms. This Application Note provides a perspective of when it is necessary to employ one technique versus another because there is no point in developing a computerized measurement when an oscilloscope reading will do the job.

Settling time as used herein is the time between when the signal begins to change and when the signal permanently enters a prescribed error band. Generally, it is not too difficult to determine when the input signal begins to change. It should be noted that this definition is with respect to the waveform itself compared to using the input signal, which causes the final output, whether the reference be a digital or analog signal. Using the input as the reference will yield the same results except the signal will be delayed by some additional amount. Delay in a system does not usually limit the throughput response of a system in the way that settling time does.

Practical circuits that measure the settling time of high frequency operational amplifiers and DAC's are shown. These are working circuits that can be used either during the development phase or the manufacturing phase of a product. A technique is shown that can automatically measure settling time as well as other AC properties such as rise time or overshoot.

LIMITATIONS OF AN OSCILLOSCOPE

The most straightforward way to measure settling time is to use an oscilloscope to view the waveform in question. This measurement is simple and direct but has limited dynamic range. A disadvantage of this method is that a modern real-time oscilloscope will overload when the input signal exceeds the selected peak-to-peak sensitivity by a factor of about 50 times. For example, assume that the selected sensitivity of the oscilloscope is set for 2mV/cm and the screen has 8cm of vertical deflection capability. This means that a waveform of 16mV x 50 = 800mV would overload the oscilloscope. On the most sensitive range, it would be possible to resolve about 0.8mV so it would be possible to measure the settling time of an 800mV change to ±0.1% accuracy. This approximately corresponds to a 10-bit DAC. This indicates that a direct measurement of settling time is limited to measuring a 10-bit DAC. Clamping techniques which can extend the dynamic range to 12 bits do not work effectively for measuring settling times under 100nsec because these are generally limited to 1V to 2V output signals. Operational amplifiers will require additional circuitry as will DAC's of greater resolution. The following paragraphs deal with the special circuitry that is needed for higher resolution DAC's and operational amplifiers.

MEASURING THE SETTLING TIME OF A HIGH SPEED 12-BIT DAC

A typical high speed 12-bit DAC will have a 2V output swing and an LSB of about 0.5mV. Many manufacturers have products of this type that settle to 1/2LSB accuracy in 35nsec. As pointed out before, there are now two problems. Accuracy of 1/2LSB or 0.25mV resolution cannot be resolved by typical high speed oscilloscopes and a 2V waveform would overload the instrument anyway. The way to solve this problem is to amplify the signal so that 1/2LSB is discernible and then to limit that output to prevent the oscilloscope from overloading. Emitter-coupled amplifiers are ideal for this because wideband gains along with excellent settling properties are attainable. Figure 1 is a schematic of an amplifier designed for this purpose. The amplifier in this schematic has two emitter-coupled amplifier stages separated by emitter followers. This amplifier has a bandwidth of 130MHz with a gain of 40 when driving a 50Ω termination.

Consider the effect of using this amplifier on the high speed DAC that was previously mentioned. The LSB of this DAC is about 0.5mV and when amplified, the effective weight of the LSB is 20mV. The output stage of this

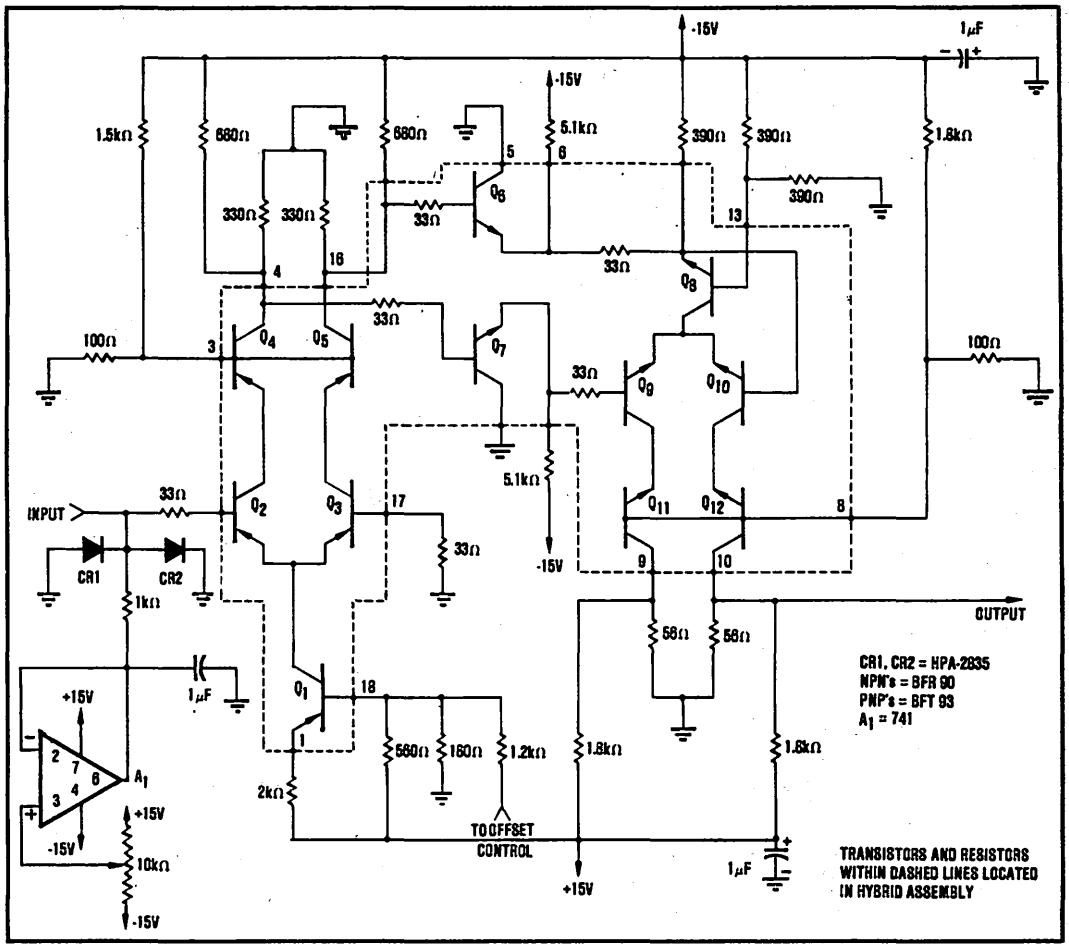


FIGURE 1. High Speed Limiting Amplfier.

amplifier is designed so that when the output is terminated in 50Ω the voltage swing will be 125mV. The 125mV that is observed is the final value of an effective 80V waveform. Since the gain of the amplifier was 40 and the input amplitude was 2V, a linear amplifier would produce an 80V output swing. Because the output waveform is clipped to the final 125mV, no trouble is experienced with the oscilloscope overloading.

Briefly, this amplifier operates in the following manner. The input signal is amplified by the input cascoded connection of transistors, Q_1 through Q_5. A pair of hot carrier diodes, CR_1 and CR_2, are used to clamp the input signal to reduce the settling time of the amplifier. Emitter followers, Q_6 and Q_7, are used to buffer the output of the first emitter-coupled amplifier to the output cascode of transistors, Q_8 through Q_{12}. In order to achieve a bandwidth of 130MHz, it is necessary to form a hybrid subassembly composed of all the transistors along with the 33Ω resistors that are found in the base of the transistors. The primary reason for doing this is to keep the emitter lead length down to a minimum. The inductance of wire is on the order of 60nH/inch so that if the amplifier were constructed using discrete components, it would be easy to accumulate as much as 0.5-inch of emitter lead length. In the amplifier shown, the emitter resistance of the two transistors is 10Ω and if the emitter lead length is 0.5-inch, the emitter inductance would be about 30nH. The pole, due to this effect, would be equal to

$$f = \frac{R_E}{2\pi L} = \frac{10}{2\pi\ 30 \times 10^{-9}} = 53\text{MHz}.$$

The amplifier has two poles of this type so the emitter parasitic effect would restrict the bandwidth to about 40MHz. An amplifier with a 40MHz bandwidth would have a settling time, to ±0.01% accuracy, of about 40nsec. This shows that hybrid construction techniques must be employed to perform a reasonably accurate measurement of the settling time of a 50nsec DAC. Figures 2 and 3 show the hybrid layout of this transistor array along with the layout of the entire amplifier.

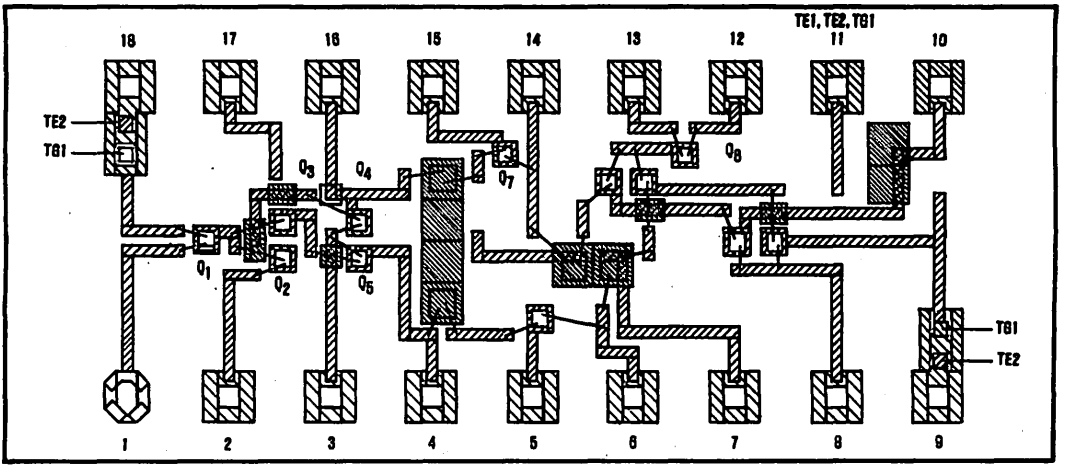


FIGURE 2. Layout of Hybrid Assembly for Wideband Amplifier.

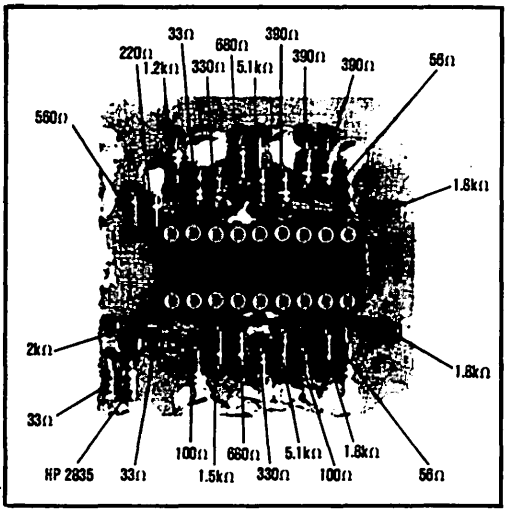


FIGURE 3. Layout of External Components for Wideband Amplifier.

Whether using this technique or any other method, when measuring settling time, it is important to use some independent means to determine the accuracy of the measurement. To determine the settling time of the amplifier, a diode switching network was used that had the same impedance level as the DAC to be measured. The assumption was that the settling time of the diode network was negligible so that the resulting response was that of the amplifier alone. Figure 4 is a schematic of the diode switching network and Figure 5 shows the transient or settling time response of the amplifier. These oscilloscope photos show the settling time to be 15nsec. When settling times as low as this are to be measured, it is recommended that a sampling oscilloscope be used. Sampling scopes typically have bandwidths that are greater than 1GHz and low capacitance inputs. In addition, sampling scopes exhibit lower settling times in

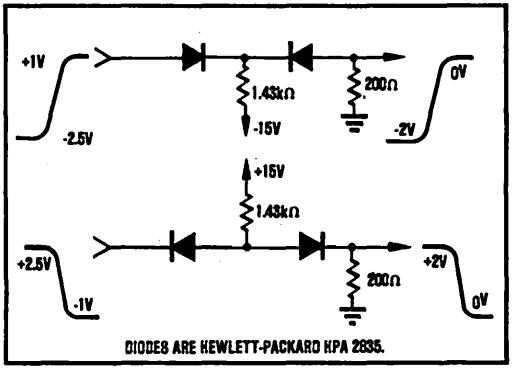


FIGURE 4. Networks used to Test Settling Time of High Speed Amplifier.

response to signals that would tend to overload a real-time oscilloscope. An approximate analysis of the amplifier driven by the diode network indicates a settling time of 13.6nsec which is close to the measured time of 15nsec. The analysis does not assume that any nonlinear effects are taking place. This is a good assumption because the amplifier, being emitter-coupled, is designed to avoid any saturation effects. Because of the high bias current in each stage, the time delay when either going into or coming out of cutoff is essentially negligible. It was experimentally determined that the amplifier has a bandwidth of 90MHz. The bandwidth of this amplifier is primarily determined by the relatively high output impedance of the DAC driving the first stage. The output stage, driven by the interstage emitter-follower has a very-high bandwidth due to the large F_T (frequency at which the current gain is one) of the transistors involved (about 4000MHz) and the fact that the load and source impedances are low, both being in the order of 50Ω.

The following analysis shows how the predicted settling time was determined. The voltage gain of the input stage is given by the expressions (this assumes that the collector time constant can be neglected).

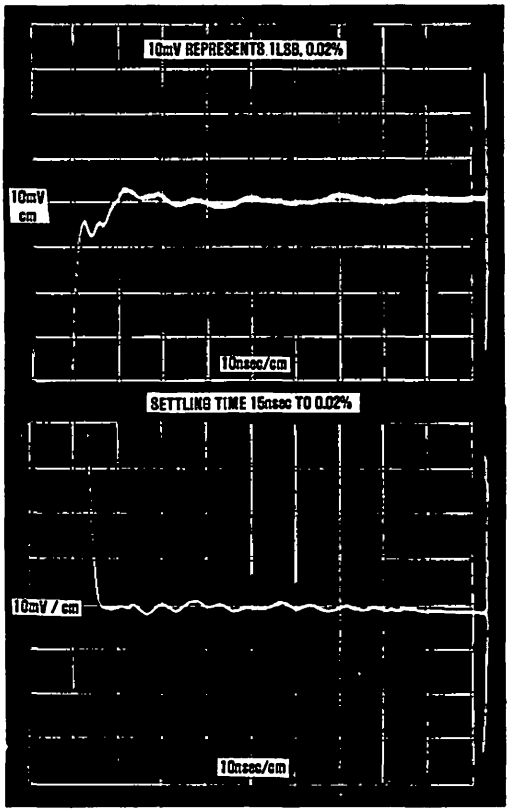


FIGURE 5. Settling Time Response of High Speed Amplifier.

1.
$$A(f) = \frac{\beta(f)\, R_L}{\beta(f)\, R_E + R_G}$$

where

$A(f)$ = the voltage gain as a function of frequency
R_L = collector load resistor
R_E = emitter resistance
R_G = source resistance

2. The transistor current gain is given by

$$\beta(f) = \frac{\beta(o)}{1 + j\frac{f}{f_T}}$$

where

$\beta(f)$ = the current gain as a function of frequency
$\beta(o)$ = the current gain at DC
f_T ≒ the frequency at which $|\beta(f)| = 1$

3. Substituting 2 into 1 and rearranging terms

$$A(f) = \frac{A(o)}{1 + j\,\dfrac{f\,\beta(o)\, R_G}{f_T(\beta(o)\, R_E + R_G)}}$$

4. The -3dB of the above expression is then given by

$$f\Big|_{3dB} = \frac{f_T(\beta(o)\, R_E + R_G)}{\beta(o)\, R_G}$$

For the amplifier shown in Figure 1

$f_T = 3000\text{MHz}$, $\beta(o) = 75$, $R_E = 5\Omega$, $R_G = 200\Omega$

and

$$f\Big|_{3dB} = \frac{f_T\ \beta(o)\, R_E + R_G}{\beta(o)\, R_G} = \frac{3000\ \frac{75(5) + 200}{75\ (200)}}{} = 115\text{MHz}$$

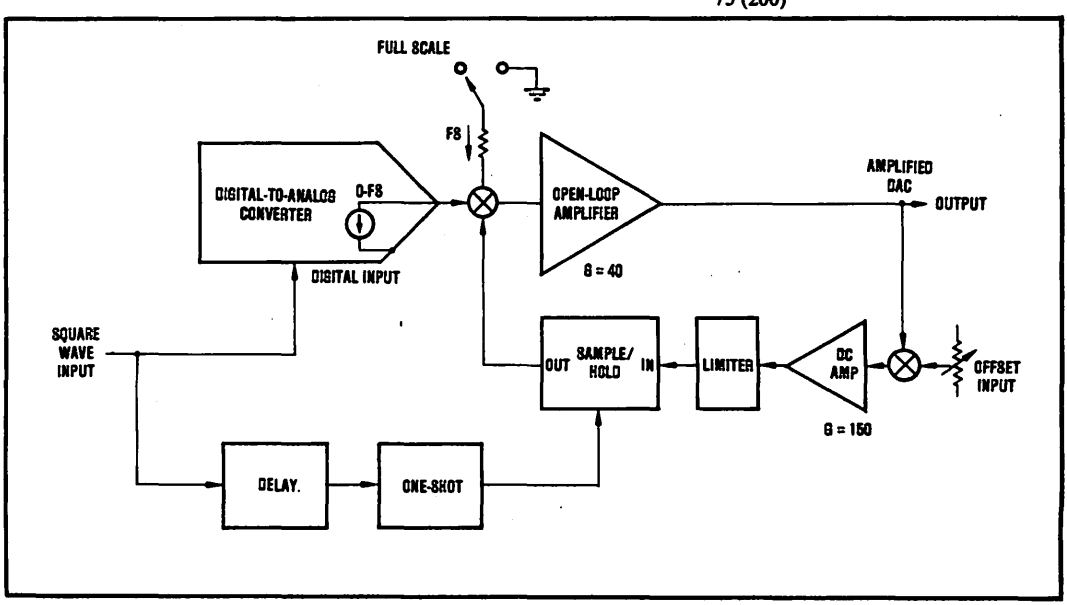


FIGURE 6. Block Diagram of System to Correct Offset of Open-Loop Amplifier when Measuring a Digital-to-Analog Converter.

115MHz corresponds to a time constant = $1/2\pi BW = 1/2\pi\ 115 \times 10^6 = 1.38$nsec. This settling time τ_S of this pole to ±0.01% is given by 9.3τ which is equal to 12.9nsec. The collector time constant τ_C is given by $\tau_C = R_L C_1$ where R_L is equal to the collector load resistor and C_1 is equal to the collector capacitor and $\tau_C = R_L C_1 = 235 \times 2 \times 10^{-12} = 0.47$nsec. Similarily, the settling time of the collector time constant is equal to 4.4nsec. Therefore, the settling time of the overall amplifier is equal to:

$$\tau \text{ overall} = \sqrt{\tau_S^2 + \tau_C^2} = \sqrt{(12.9)^2 + (4.4)^2} = 13.6\text{nsec}$$

which is in good agreement with the measured value of 15nsec considering the simplified analysis.

One of the shortcomings of employing this amplifier is the tendency of the offset to shift with time even after a sufficient warm-up period. This is due to the relatively high power dissipation of the input stage (7.5mW per input transistor) and the fact that the input stage has been designed with discrete transistors in hybrid fashion. More stable performance could be obtained if the input was a monolithic pair, but transistors with greater f_T are available only in discrete form. The tendency of the open-loop amplifier to drift with time can be corrected using feedback techniques.

Figure 6 is a block diagram of the system used to correct the offset of the open-loop amplifier. In this system, the offset at the output of the open-loop amplifier is considerably lowered by the DC amplifier and the feedback connection. The DC amplifier can be a low offset monolithic operational amplifier which will have excellent stability with time and requires little warm-up time. The gain of the DC amplifier is set at 150 to mask the offset of both the sample/hold and the open-loop amplifier. The sample/hold serves the purpose of selecting only that part of the output waveform that should be controlled for zero offset. If it is desired to observe the response time when the DAC is changing from zero to full scale, it is necessary to sum an equal and opposite full scale level at the input to the open-loop amplifier so, in effect, the output of the amplifier settles from a clipped positive extreme to zero. It is necessary to offset the input by a full scale level to keep the input signal within the dynamic capability of the open-loop amplifier. When the DAC settles from full scale to zero, it is not necessary to offset the input because the input is within the dynamic capability of the open-loop input. If the system is driven by a square wave, the output will tend to be at zero one-half of the time. The other half of the time, the output will either be at the positive or negative extreme of the open-loop amplifier. It is now easy to see why the sample/hold is necessary because output to be controlled is available only one-half of the time. Figure 7 shows a schematic of a production test fixture that is used to measure the settling time performance of the DAC63, a high speed DAC that is ECL-compatible.

In Figure 7 a square wave generator is formed from IC4 and the related circuitry and is set for a frequency of 135kHz to allow viewing of the settling time performance beyond just the immediate specification. The square wave oscillation is buffered by IC3, a quad ECL buffer. IC3 provides the oscilloscope synchronization pulse, the logic reference for the DAC being tested and it also drives IC1 and IC2. The logic signal is taken through switch contacts S2b from either pin 2 or pin 3 from IC3. The determination of which signal is selection depends of whether positive or negative settling is to be tested. The phase of the signal at pin 7 of IC3 is constant so the oscilloscope controls need not be altered when viewing positive or negative settling time. The logic signal is then sent to IC1 and IC2 before being applied to the device under test. A calibrate function is implemented by disabling bit 1 (MSB) through bit 11 leaving only bit 12 active. Since only bit 12 (LSB) is active, the weight of the LSB is determined independent of the gain of the amplifier. For convenience, the weight of an LSB is set for a 1cm oscilloscope deflection. After the digital signal is applied to the DAC under test, the output of the DAC is sent to the high speed open-loop amplifier previously described. When the phase of the logic input signal is selected, based upon whether positive or negative settling is to be viewed, it is necessary to apply a +10V reference level to pin 18 on the device under test. During the time when negative settling time is to be observed, the action of the +10V reference signal through the 1kΩ resistor, internal to the DAC63, provides a 10mA current that is just equal to the 10mA DAC current that is now being turned on. This is necessary to provide approximately a zero volt signal level to the input of the amplifier to stay within the dynamic range of the amplifier.

Amplifier A_1 generates the +10V reference which is applied to the device under test through contacts S2a. Switch contacts S2a and S2b are driven together so that the phase and offset of the signal will result in proper oscilloscope presentation. See Figure 8 which depicts the output of this test fixture. The synchronization output, which appears at connector J3 is used as a time reference for either the measurement of the positive or negative settling of the waveform under test.

The output of the device under test is then sent to the open-loop amplifier whose performance and operation have been previously described.

The output of the open-loop amplifier is then applied to amplifier A_3 before being sent to the sample/hold that is comprised of amplifier A_2 switch Q_2 and driver transistor Q_1. IC6 is a monostable which is used to supply the sampling signal to the sample/hold.

SETTLING TIME OF AN OPERATIONAL AMPLIFIER

Refer to Figure 9 for a block diagram of a circuit that measures the settling time of an operational amplifier in the inverting configuration. The false summing junction technique is commonly used because of its simplicity and effectiveness in performing the measurement. The false summing junction contains the same settling information as the actual summing junction. The actual summing junction is not used in order to avoid any extra loading that might alter the performance of the operational amplifier under test. Another important feature of this

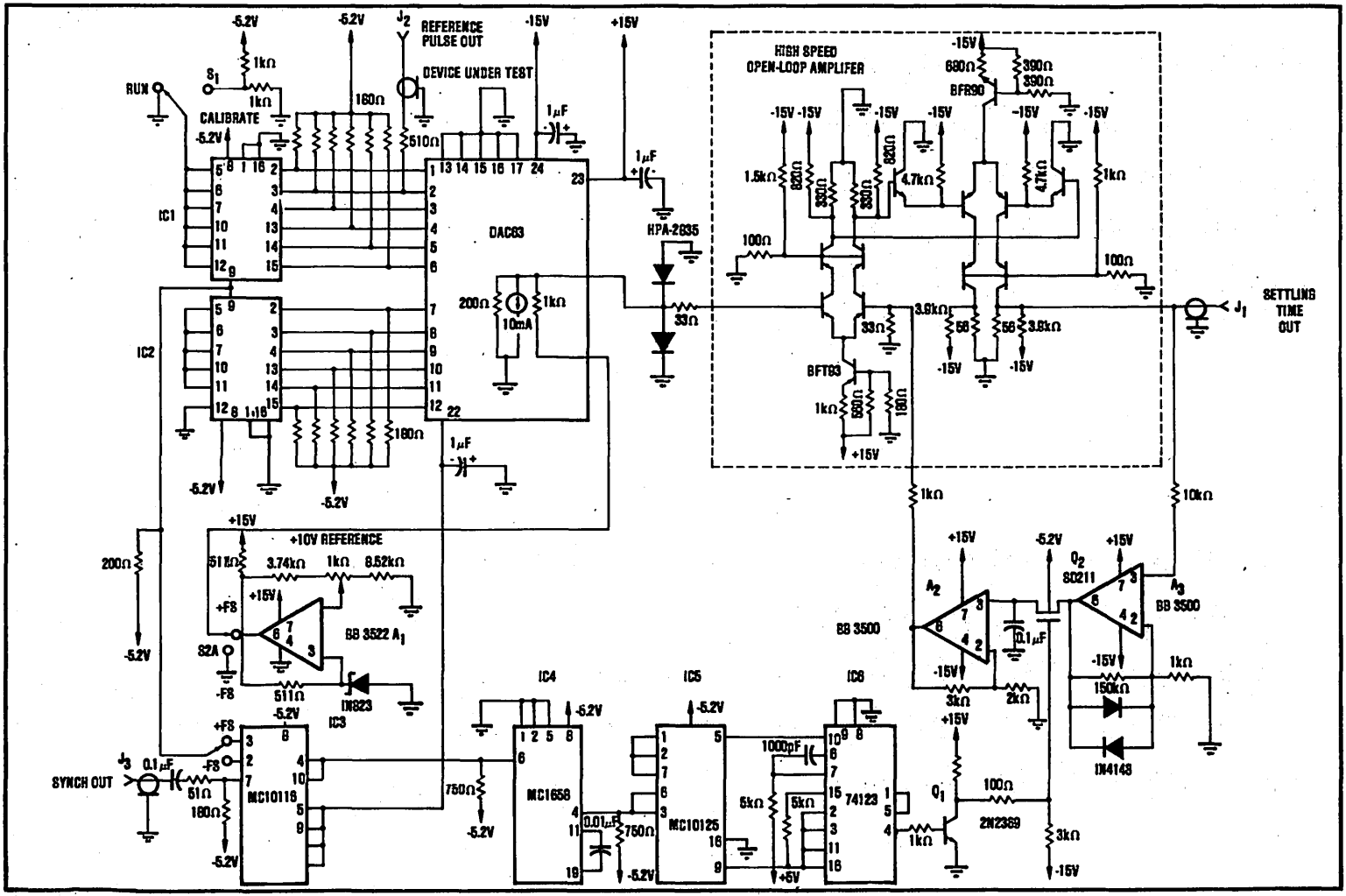


FIGURE 7. Settling Time Test Fixture for High Speed Digital-to-Analog Converter.

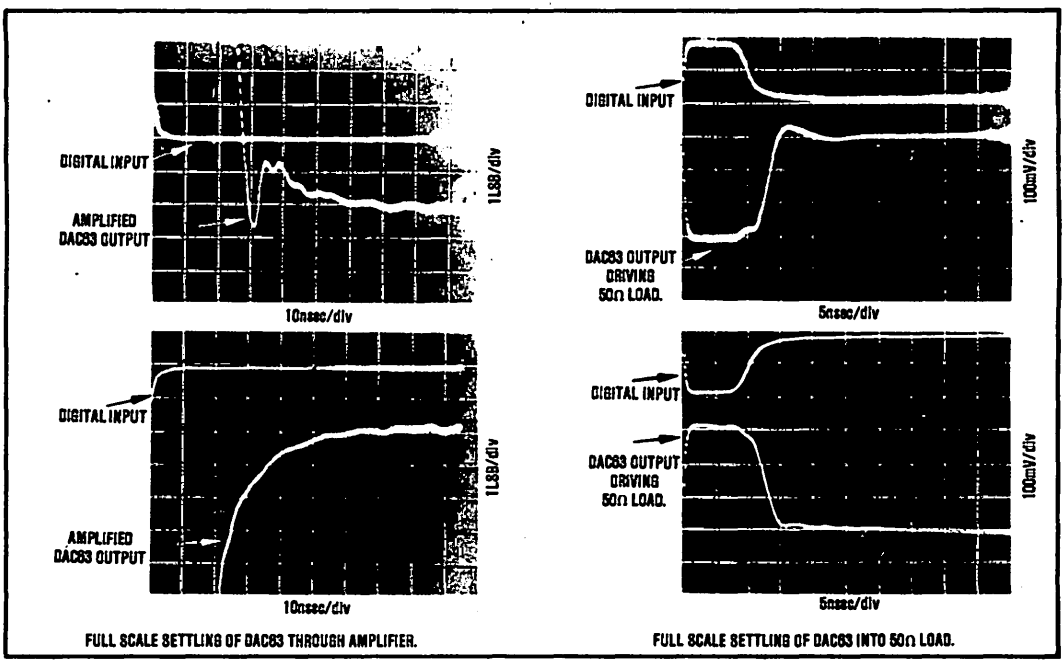


FIGURE 8. Output of Settling Time Fixture.

measurement technique is to correct for the effect of the waveform aberrations associated with the signal coming from the pulse generator. Very few, if any, commercial pulse generators have a flat top response that is adequate as a test signal if the op amp output is used directly for evaluation. Since the inverting configuration creates the opposite phase signal as the input, the waveform viewed at the false summing junction tends to be free of the effects of the input waveform inperfections.

In practice, it is relatively straightforward to implement this measurement for making settling time measurements down to about 250nsec with accuracies to±0.01%. This measurement does have some shortcomings when settling times much shorter than 250nsec to ±0.01% accuracy for 10V output changes need to be made. The difficulties that develop are two-fold. The typical oscilloscope probe has too much capacitance and this loads down even the false summing junction, leading to inaccuracy in the final measurement. The second difficulty is that fast changing waveform aberrations cause the summing junction to have to change so that the amplifier can follow the signal. The waveform at the actual summing, and henceforth at the false summing junction, can be relatively large due to the AC gain of the operational amplifier being relatively low at the frequency of the waveform inperfection. The solutions to these two problems are relatively straightforward.

First, to achieve maximum sensitivity, it is often necessary to use a direct-coupled 1:1 probe or a piece of cable when connecting to the oscilloscope. Under these circumstances, it is very easy to add 30pF of capacitance to the false summing point (1 foot of RG58 50Ω cable has 30pF of capacitance). Assuming that the feedback resistance R of the amplifier is 1kΩ and the capacitance load on the false summing junction is 30pF, an effective 15nsec time constant would exist at the false summing junction. For a waveform to settle to ±0.01% accuracy after being impressed upon a simple time constant, 9.2 time constants are required, therefore, it would take 138nsec for the false summing point to settle. If the anticipated settling time of the amplifier under test is 250nsec, the measured settling time would be in the vicinity of $\sqrt{(138)^2 + (250)^2} =$ 286nsec. Faced with this problem, one could either buy a commercial FET probe or use the circuit shown in Figure 9. The circuit shown in Figure 9 is, in effect, a FET probe

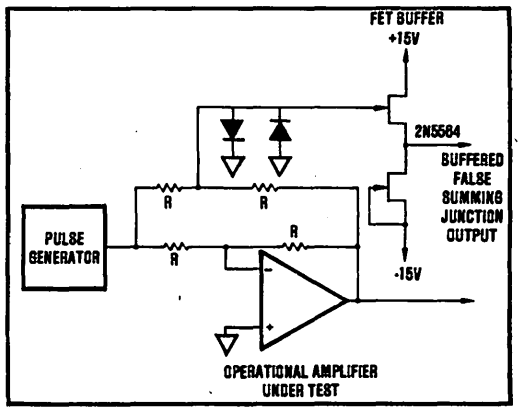


FIGURE 9. Block Diagram of the False Summing Junction Technique for Measuring the Settling Time of an Operational Amplifier.

but is less expensive and is often more convenient to use because the circuit is easy to build onto the breadboard or onto the test fixture that is used to evaluate the amplifier under test. The 2N5564 FET was chosen to buffer the false summing junction because the input capacitance is low, about 5pF, and the output impedance is approximately 50Ω. With the 50Ω output impedance, the cable length needed to drive the oscilloscope is not critical because the cable can be effectively back-matched.

The second problem that must be dealt with is that of obtaining an input signal with a clean flat-top response. The flat-top response of typical commercial pulse generators is no better than 1% of the signal amplitude being used as a test signal. The false summing technique will cancel low frequency effects but high frequency effects cannot be cancelled because of the transient response or phase response of the amplifier.

To illustrate this effect, assume that the signal used to evaluate the amplifier under test has a ripple component of frequency ω and an error amplitude of a. Assuming a 1-pole amplifier response, the approximate waveform that will exist at the summing junction is given by -

$$e(t) = 2\frac{V}{A(o)}\left(\frac{A(o)}{2}\epsilon^{\frac{-\omega o A(o)}{2}t} - 1\right) + \frac{a}{2}\left(\frac{\omega^2}{A(o)^2}\right)\sin\omega t$$

where ωo is equal to the -3dB bandwidth of the open-loop amplifier and A(o) is the open-loop gain of the amplifier. Figure 10 depicts the test waveform and shows more detail on the derivation of e(t). As an example of this effect, the following calculation demonstrates what happens when the test generator has a 5% ripple amplitude and a frequency of 1MHz. If the amplitude of the test signal is 10V, the ripple amplitude will be 0.5V. Note the term $\omega o A(o)/2$ corresponds to the-3dB bandwidth of the closed-loop amplifier which will be assumed to be 10MHz. Therefore, once the transient caused by the step function has died away, the remaining waveform is caused by the imperfect signal generator and the phase response of the amplifier. The amplitude of the signal at the summing junction is then

$$e(t) = \frac{a}{2}\left(\frac{f^2}{f\text{-}3dB^2}\right)\sin(\omega\tau)$$

or

$$e(t) = \frac{0.5}{2}(1^2/10^2)\sin(\omega\tau) = 2.5mV\sin(\omega\tau).$$

If the amplifier is specified to settle to ±0.01% of FS or to 1mV out of 10V, clearly a better signal generator must be found.

Figure 11 is a schematic of a pulse shaping circuit that is capable of supplying the clean flat-top response needed to effectively test high speed operational amplifiers.

This circuit is capable of producing the low ripple waveform required to evaluate an amplifier that settles to ±0.01% of full scale accuracy for a 10V step in 100nsec. Figure 11 also shows an entire production test fixture that Burr-Brown uses to evaluate the OPA600, a 100nsec settling operational amplifier.

Briefly, the circuit works in the following manner. IC1 is

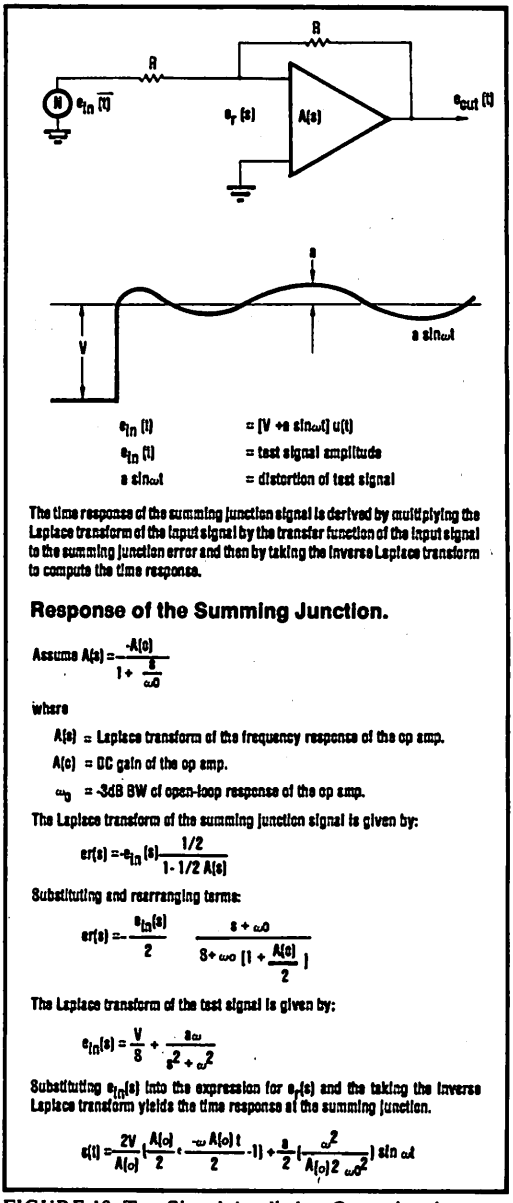


FIGURE 10. Test Signal Applied to Operational Amplifier Under Test.

a square-wave generator which is set for 500kHz. The TTL signal from IC1 is translated by Q_1 which, in turn, drives Q_2, a 2N2369. Q_2 is responsible for creating the well defined flat-top response as Q_2 is either driven into saturation or when Q_2 is cut off, the waveform is defined by diode, D_1, damping to the level established by the IN753 zener-diode. The signal is then buffered by the action of emitter followers Q_3, Q_4, and Q_5 before driving the device under test and the related circuitry. For reasons similar to why the DAC signal must be amplified for proper viewing, the signal at the false summing

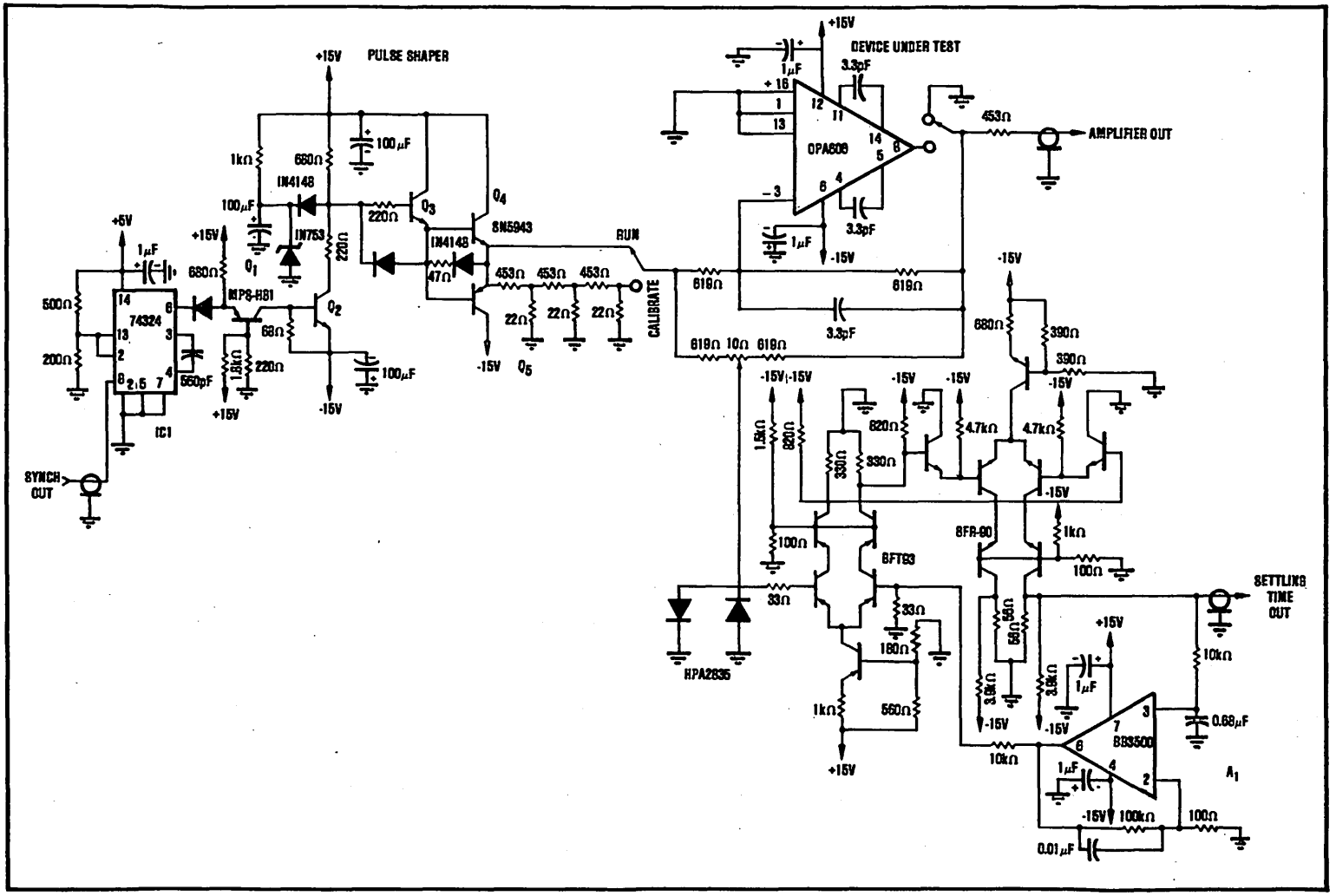


FIGURE 11. Settling Time Test Fixture for High Speed Operational Amplifier.

junction of the operational amplifier must be increased. Using the same wideband amplifier that was previously described, the false summing junction signal is amplified before being sent to an oscilloscope for viewing.

A_1 forms a low-pass filter with a gain of about 1000 and is used to correct for the high offset and drift associated with the wideband amplifier. It is not necessary to use a sample/hold to correct the offset of the wideband amplifier as was done for the DAC because the waveform at the false junction has an average value of zero. This test fixture has the useful feature of being able to calibrate the amplitude of the error signal. When placed in the calibrate mode, an attenuator is inserted at the output of the square-wave generator that reduces the amplitude of the test signal to 1/10,000 of its original value. 1/10,000 of the test signal corresponds to the amplitude of ±0.01% of the device under test, so a convenient means for checking the measurement is provided without having to know the value of the gain.

WAVEFORM DIGITIZER

A more powerful technique that can be employed to evaluate the settling time of a DAC or an amplifier is to digitize the waveform under test. Once the waveform is digitized, the waveform can be sent to a computer where software routines can be used to determine the performance of the device under test. Digitizing the waveform is superior to hardware-oriented instrumentation because of the versatility associated with a computer. The circuits and systems previously described were dedicated to evaluating only settling time. Different instrumentation would have to be developed if rise time, delay time, overshoot or some other AC parameter needed to be tested. By contrast, once the waveform has been digitized, any property of the waveform can be analyzed with the same hardware. Waveform digitization is not limited to testing DAC's and operational amplifiers, and the circuits that follow lend themselves to the evaluation of arbitrary waveforms. Before proceeding with a detailed description of the hardware used to digitize a waveform, a perspective on the proper sampling rate will be given. Choosing the proper sampling rate is important so that realistic hardware requirements are developed. As an example, consider the requirements of digitizing the response of a 12-bit DAC that settles to 1LSB in 50nsec for a full scale change. In the area of the waveform where the DAC is settling to its final value, the rate of change of the waveform is about 1mV/nsec. (See Figure 8 which shows the DAC63 settling to its final value.) Since this is a 12-bit DAC, 1LSB is equivalent to 0.5mV and if the waveform is to be digitized to the necessary accuracy, the sampling rate should be

$$T_S = \frac{\overline{V_E}}{(\frac{dv}{d_T})}$$

where dv/d_T is equal to the rate of change of the signal in the area of interest, T_S is equal to the sampling interval and V_E is equal to the allowable error signal. For the example in question,

$$T_S = \frac{V_E}{\frac{dv}{d_T}} = \frac{0.5mV}{\frac{1.0mV}{nsec}} = 0.5nsec$$

The leading edge of the DAC waveform shown in Figure 8 rises at the rate of 0.4V/nsec. When the rising edge of the waveform is sampled at 0.5nsec intervals, this part of the waveform can be resolved to 0.2V accuracy. Considering that it is a 2V waveform, resolving the rising edge to an amplitude of about 10% accuracy is probably adequate or if not, the sampling rate can be increased. If the expected settling time were to be 50nsec, data would be taken for a longer interval to assure that the device settles. If data was taken for 500nsec with 0.5nsec sample intervals, a record length of 1000 points to at least 12-bit accuracy would be required. This example illustrates an appropriate method for selecting the sample interval and record length for the measurement in question. Of course, as the performance requirements change, the measurement parameters can be suitably scaled.

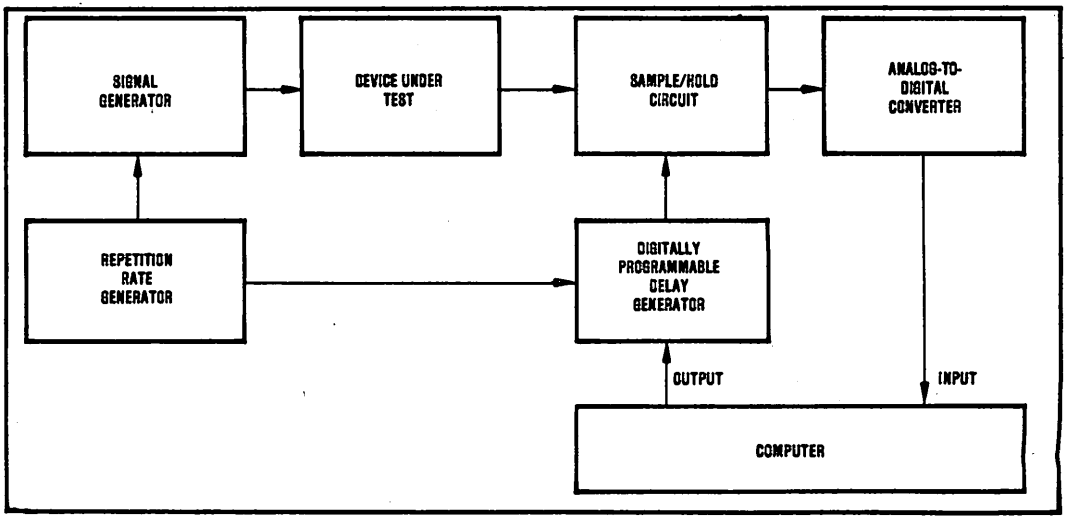


FIGURE 12. Block Diagram of a Digitizer.

Figure 12 shows a block diagram of a digitizer that can be used to record signals for many different measurement requirements. The digitizing works in the following way. The basic principal behind the digitizer is that when a waveform is synchronously sampled, the sampled value of the waveform will correspond to the phase difference between the sample pulse and the input waveform itself. At t = 0, the computer sets the programmable delay generator to start sampling at the beginning of the waveform. As the signal generator has been synchronized with the delay generator, the output of the sample/hold will be DC. The output of the analog-to-digital converter is then sent to the computer for recording. When a stable value has been recorded for a particular sample point, the delay is incremented and the process is repeated until the entire waveform has been digitized. Later it will be shown that the sample/hold circuit and the analog-to-digital converter can take on many different forms. The sample/hold could range from a conventional one to a sampled comparator while the ADC could be a digital voltmeter. Figure 13 demonstrates the waveforms of a hypothetical digitizer. Note how the digitizer responds very much like a sampling scope.

Figure 14 shows a detailed diagram of an actual digitizing system that can measure the performance of a high speed 12-bit digital-to-analog converter like the Burr-Brown DAC63.

The digitally-programmable delay is achieved by comparing the output of A_1, which is configured as a integrator, to the reference level which enters the other input to comparator IC3. The variable reference comes from DAC1 which gets its digital input from the comparator. Therefore, as the DAC input to the comparator increases in value, the comparator will generate a delayed leading edge that is controlled by a digital input. The delayed leading edge is then differentiated and formed into a 7nsec sampling pulse by IC2. The sample/hold function is created by IC1, a sampled comparator and A_2, an operational amplifier configured as an integrator. The comparator and integrator form a sample/hold in the following way. The comparator is a sampling type which means that the output responds only during the presence of a sampling pulse. Therefore, when the input to the comparator is in a state to allow the output to change state, the change of state will only occur at the time of the sampling pulse. This comparator has the additional feature of latching the result until the next sample pulse. The latched output is then integrated and fed back to the other input of the comparator. The integrator, in effect, forms a bang-bang servo and a stable condition of this loop is arrived at when the integrated output is above or below the amplitude of the sampled waveform 50% of the time. The integration time is selected so that the output of the integrator varies by a negligible amount between sample pulses. A differential integrator provides a convenient interface to the complementary output of the differential comparator. The output of the integrator, which is now DC, represents the value of the AC waveform at the point in time where it was sampled. This, in effect, forms a fast accurate sample/hold with an aperture time of about 100psec which is determined by the comparator IC1. Its dynamic performance is different from a conventional sample/hold in that it takes a long time to respond to signals that change rapidly. However, no dynamic error is made for this type of signal because the integrator eventually charges up to the correct value. While performance of this type may not be adequate for data acquisition systems, it generally poses no difficulty for measurement systems of this type.

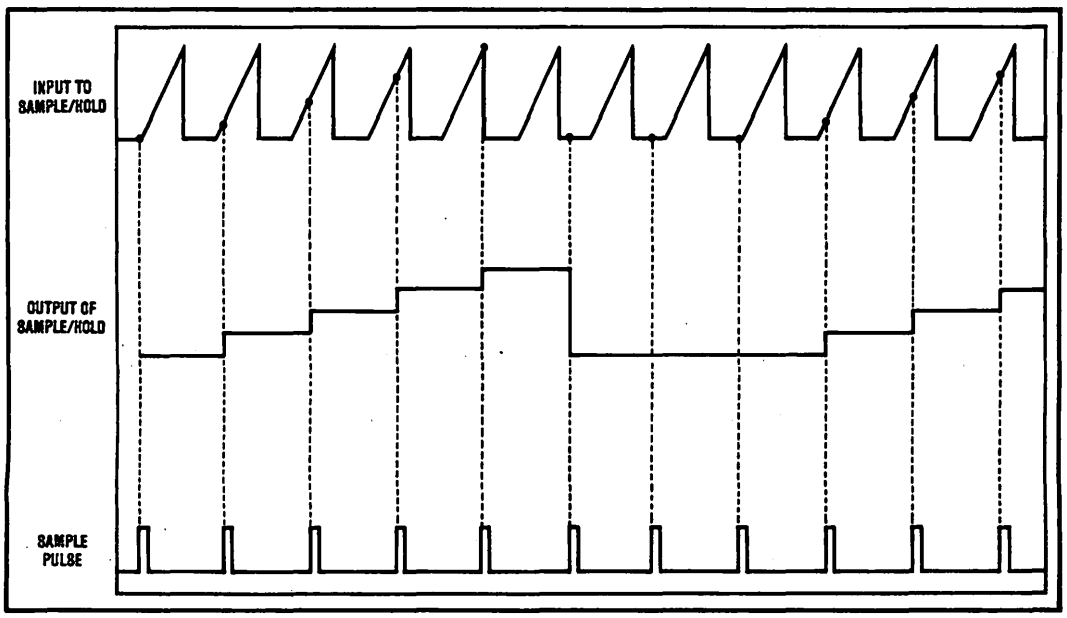


FIGURE 13. Response of Digitizer.

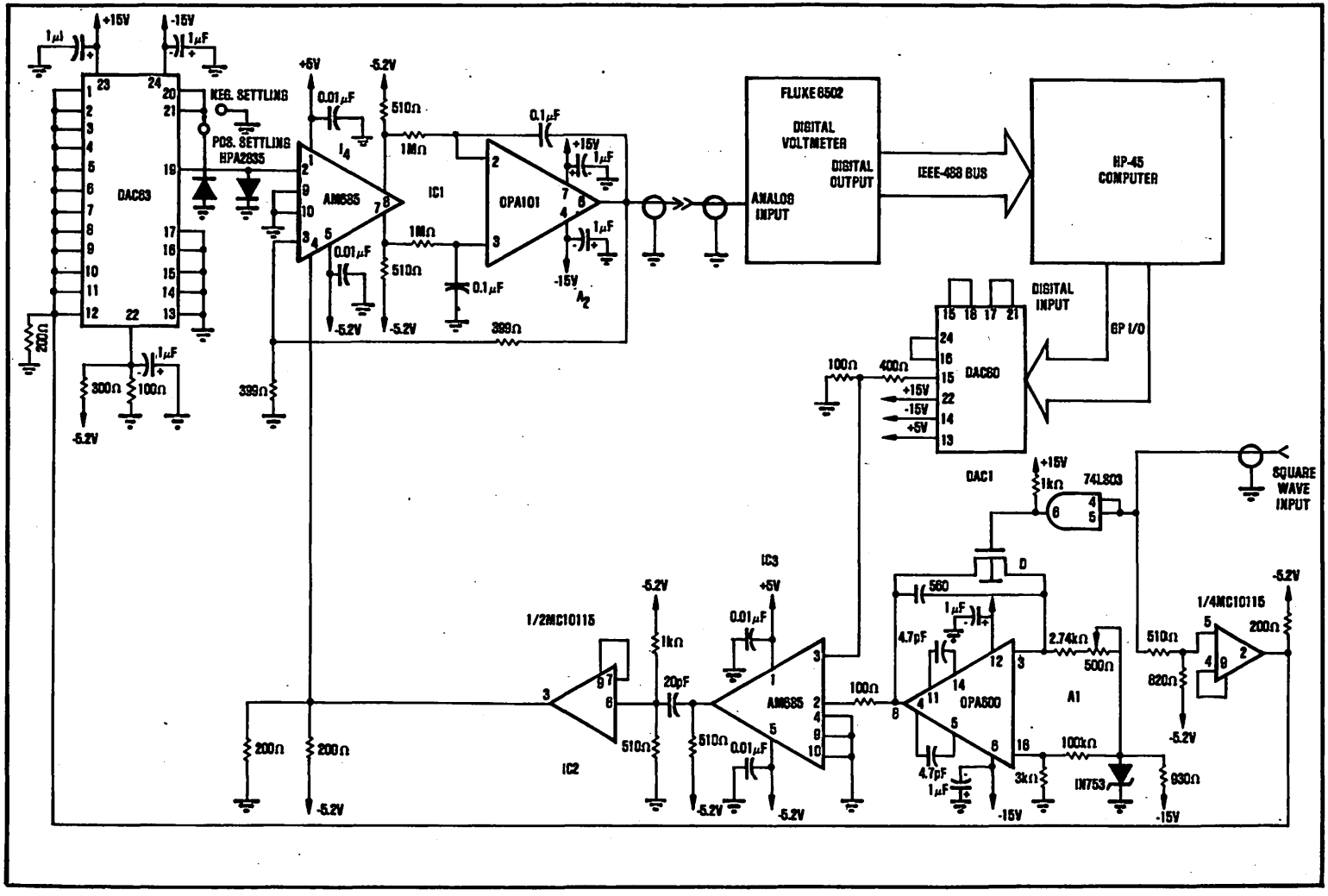


FIGURE 14. Computer Controlled Digitizer.

For the system shown here, the output of the integrator is sent to a FLUKE 8502 voltmeter for measurement. The voltmeter is connected to an HP45 through an IEEE-488 interface where the data is stored for further analysis. Once it has been detected that the output of the sample/hold is stable, the sample point is incremented to the next position. This process is repeated until the entire waveform has been recorded.

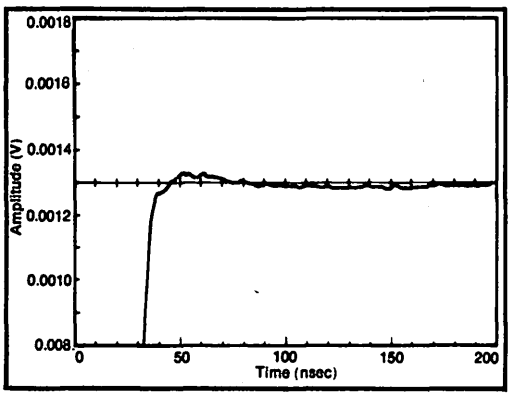


FIGURE 15. Settling Time of DAC63 Using Digitizing Measuring System.

Figure 15 shows one possible output of such a system that was used to evaluate the performance of a DAC63. A program was written which has displayed the data on an oscillograph type format to demonstrate the versatility of manipulating the data once it has been recorded. Once the data has been stored in memory, it could be analyzed in many different ways. Only a digitizing system of this type has this flexibility. The horizontal axis is in nanoseconds and the vertical is in volts.

ACCURACY OF MEASUREMENT

A problem when measuring settling time is determining the validity of the measurement.

The problem usually focuses on two portions of the measurement. First, what is the speed or the settling time of the measurement itself? Second, when a device settles to a stated accuracy in a given amount of time, would the waveform stay within the prescribed error ban if the measurement time were extended indefinitely?

Answers to both of these questions can be obtained conveniently with the computerized measurement system previously described. To determine the settling time of the measurement, a network of hot carrier diodes was used as a standard. It is believed that this is reasonable because the part of the waveform that is used as the standard is that part when the hot carrier diode is turned from on to off. Figure 4 illustrates the type of diode network that was used as a standard. When done in this manner there can be no possible thermal heating effects since the diode is turned off and since the impedance levels are low, the settling time of the diode network can be assumed to be negligible. Figure 16 shows the device under test and the diode network. The second part of this validation procedure is to compare the final value of the

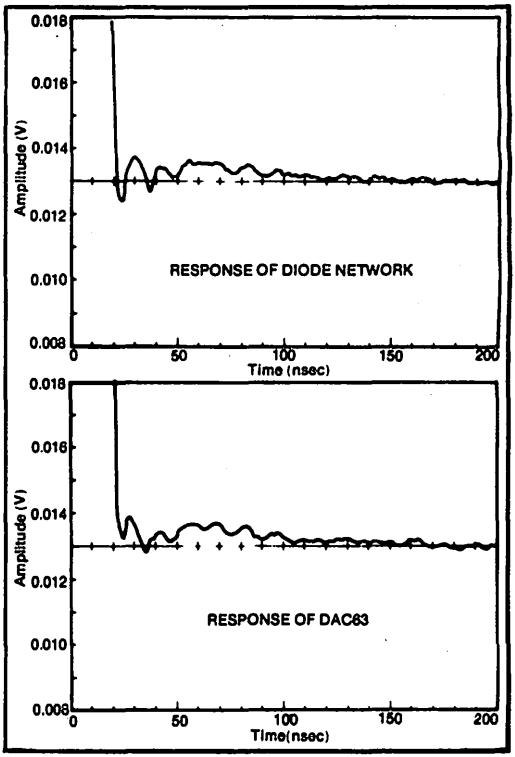


FIGURE 16. Comparison of the Device Under Test and a Standard Diode Network.

waveform under test under AC conditions, against the value when the device is left on continuously. The assumption is that when the diode is turned from on to off, the diode will not introduce any thermal effect and if there is any drift detected in the measurement, the drift is due to the instrumentation. When this experiment was performed, a difference of about 1mV was noted between the diode network evaluated under AC conditions and evaluated under DC conditions. When the DAC under test was compared against this standard, it was found that a similar difference was detected. Therefore, it can be assumed that the product was free from any long term settling effects. A measurement of the type just described would be difficult with anything but a computerized system because other hardware-oriented techniques are subject to greater drift and the results are more difficult to record for later comparisons. Figures 17 and 18 depict the results of this measurement.

Another possible application of this digitizing system is to correct the output waveform for the effects of imperfections associated with the input waveform. Measuring the settling time of a DAC or using the false summing junction of an operational amplifier doesn't present the problem, but measuring the settling time of a voltage follower would. A possible method of performing this measurement would be to digitize the input and output waveforms and using software techniques, determine when the output waveform tracked the input waveform.

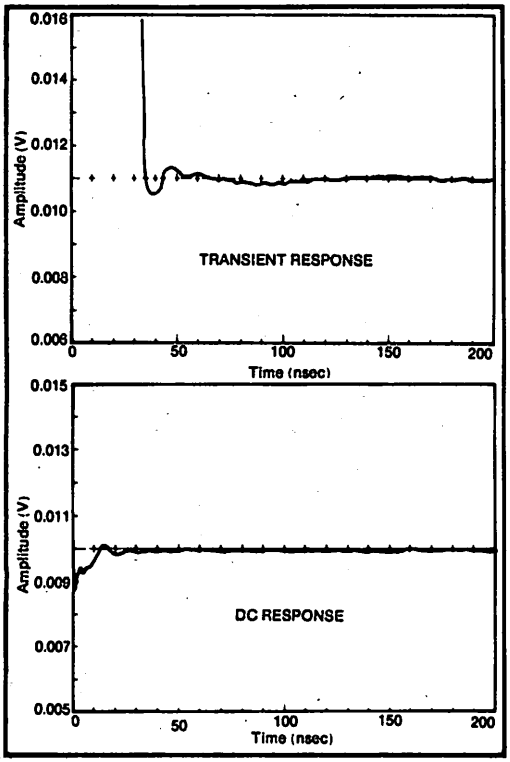


FIGURE 17. Comparison of Transient Response and DC Response of DAC Under Test.

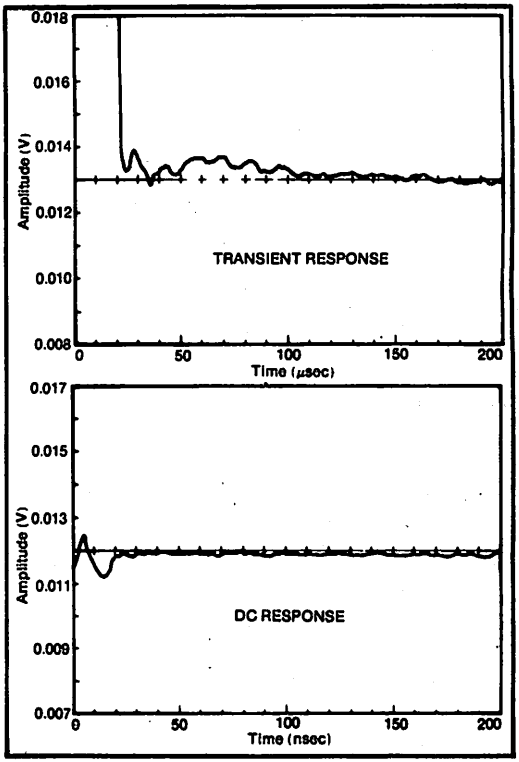


FIGURE 18. Comparison of Transient Response and DC Response of Diode Network.

SUMMARY

Numerous techniques ranging from oscilloscope measurements to a computerized digitizing system have been offered as solutions to the problem of measuring settling time. The measurements were described in a way to allow the user to determine which procedure is best suited for the application. The limitations of each measurement has been shown so that the user can determine the proper trade-off when assessing the degree of complexity necessary to perform the desired measurement.

STATIC AND DYNAMIC TESTING OF DIGITAL-TO-ANALOG CONVERTERS

This Application Note describes both static and dynamic testing of digital-to-analog converters.

STATIC TESTING

A static test is a test that requires a much longer time than the settling time of the DAC under test.

A testing time of greater than 100msec is typical because of the speed limitations of the digital voltmeter, the manual operation of taking data, or changing bit switches.

The DAC under test will be in the unipolar mode (output ranges from 0 to +10V), however the same test could be made in the bipolar mode (±10V output).

The following measurements will be performed:

1. Offset error
2. Full scale error (full scale error includes offset error)
3. Gain errror
4. Linearity error

Since static testing is a slow operation, and for a 12-bit DAC there are 4096 codes, a technique will be explored to avoid testing all 2^n digital codes.

TESTS USING A DIGITAL VOLTMETER

When testing a DAC with a digital voltmeter (DVM) particular care should be given to the linearity requirements of the DVM in conjunction with the number of bits the DAC uses. A good rule of thumb is that the DVM should be at least 10 times more accurate than the smallest DAC error to be measured, which is usually the linearity error specification of ±1/2 LSB. Table I shows the DVM requirements for accurate measuring within ±1/2 LSB linearity.

TABLE I. DAC Resolution Versus DVM Requirement.

DAC RESOLUTION	LSB 10V FSR	1/2OLSB	DVM REQUIREMENT	DVM RESOLUTION
8 BITS	39.0mV	19mV	4 DIGITS	1mV
9 BITS	19.5mV	10mV	4 DIGITS	1mV
10 BITS	9.8mV	05mV	5 DIGITS	0.1mV
11 BITS	4.9mV	024mV	5 DIGITS	0.1mV
12 BITS	2.4mV	012mV	5 DIGITS	0.1mV
13 BITS	1.22mV	006mV	6 DIGITS	001mV
14 BITS	0.61mV	003mV	6 DIGITS	001mV
15 BITS	0.30mV	0015mV	6 DIGITS	001mV

Since the linearity error of a DAC will usually be less than its gain error, the linearity error of a DVM is more critical than its scale factor error. From Table I we see that a 12-bit DAC requires at least a 5-digit DVM. A typical 5-digit DVM has a scale factor error of ±0.005% and a linearity error of ±1 digit. Since the linearity of the DVM is very critical, a trip to the calibration lab is recommended to verify that the DVM is linear to within ±1 digit (±100μV) on the +10V range. If tests are made with the DAC operating in the bipolar mode be sure the DVM has low symmetry error, that is, it reads the same for positive and negative input voltages. If the DVM is used on the 10V and the 1V range, the scale factor error of the 1V range must match the 10V range to within 100μV. If the scale factors do not match all measurements should be made on the 10V range only.

Next, the test circuit can be considered. Special precaution should be given to the wiring (see Figure 1),

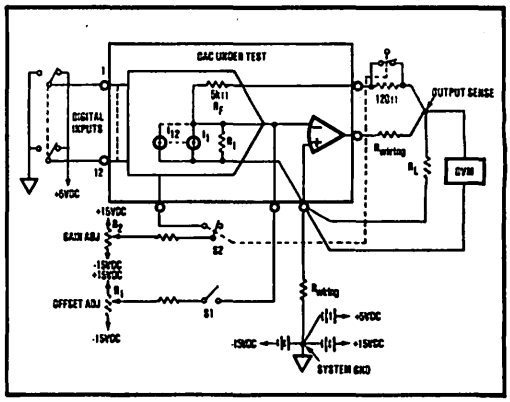


FIGURE 1. Static DAC Test Circuit.

connecting the DVM, the feedback resistor of the DAC, and any load impedance so that voltage drops caused by changing current in wiring resistance will not be misinterpreted as DAC errors. If a current output DAC is tested, add an external output operational amplifier. The adjustment potentiometers can be switched out of the circuit so that offset and full scale errors can be measured.

Before measuring any errors of a DAC, sufficient warm-up time should be allowed. Many converters have an internal temperature rise of 10°C or greater. If the temperature coefficient of the gain error is 20ppm/°C and the internal rise is 10°C, a change of 200ppm or 2.0mV on the +10.0V output will be experienced from the time power is supplied until converter output has stabilized.

Since a 5-digit DVM can resolve 0.1mV (10ppm), allow the temperature rise to reach 9.5°C so the DVM reading will be stable. For instance, if the internal power dissipation of a converter is 500mW the warm-up time can be from 5 to 15 minutes depending upon the type of package. An epoxy or glass package has a longer warm-up time than a ceramic or metal package; therefore, to make accurate measurements, allow the converter to warm-up or use high speed automatic test equipment which can measure any error before full scale output changes by 10ppm.

As mentioned previously, the plan is to devise a test that eliminates the need to test all 2^n digital codes. Table II shows a test plan to measure the offset, full-scale, and gain errors. Also, the linearity and differential linearity errors are measured at 15 evenly spaced points, namely 1/16, 1/8, 3/16 . . . . . 7/8, and 15/16 of the full scale output range. Taking data at these 15 points graphically illustrates the characteristics of converter errors as shown in Figure 2. The data recorded in the table was taken from a model DAC85. A 6-digit DVM was used for extra resolution.

The full scale voltage in step 5 was increased to 10.23750V. This gives an ideal bit weight starting at the LSB equal to 2.5mV, 5.0mV, 10mV. . . . 2.560V and finally 5.12V for the MSB. These numbers can be easily memorized and the error voltages can be quickly calculated by inspection. The full scale voltage can be boosted to 10.2375V by increasing R_F (with a resistor in series) or by increasing the reference voltage by 2.4%.

The linearity error and the differential linearity errors for the 15 evenly spaced output points are plotted in Figures 2a and 2b. Notice that the offset and gain errors have been nulled to zero.

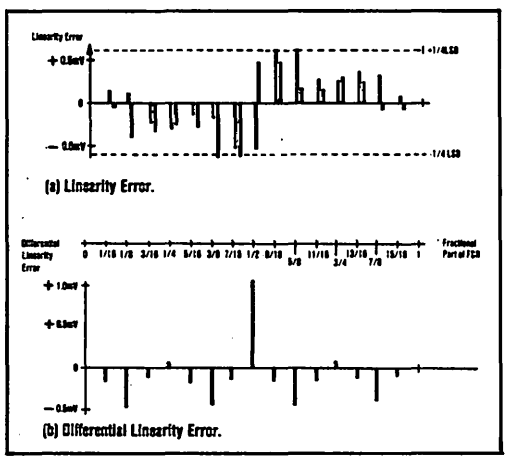


FIGURE 2. DAC85 Errors at 15 Evenly Spaced Carries.

An interesting fact is that the symmetry of the errors (linearity error at any binary word) will be equal in magnitude but opposite in sign to the one's complement of that code. A close examination of the data in Table II shows that this symmetry holds to within 80μV. This means that the converter has very little interaction (low superposition errors). This means that the weight of any bit or combination of bits that are turned on is toally independent of the on/off state of other bits.

This symmetry which produces repeating error patterns is true of all DAC's (provided superposition errors are low), however superposition errors do not need to be small for a converter to meet its linearity and differential linearity error specifications. In fact, bit interaction greater than 1/10LSB is very likely to occur in a 16-, 15-, or 14-bit DAC, and occurs in some 12-bit converters.

When bit interaction is less than 1/10LSB, it is possible to considerably shorten the tests of Table II. To determine the maximum linearity error, just do steps 3 and 5 to null the offset and gain errors and then test each individual bit as shown in steps 6 thru 13 and the second part of steps 14, 15, 17, and 21. Now take the sum of the positive errors to get the maximum positive linearity error. Next, take the sum of the negative errors to get the maximum negative linearity error. When we do this for the DAC85 data in Table II, we get a maximum linearity error of +0.63mV for the 100011111011 digital word and -0.69mV for one's complement (011100000100) of this digital word.

When superposition errors are small, the maximum differential linearity error (DLE) occurs at one of the digital code carries of the individual 12 bits. Instead of measuring the differential linearity errors they can be computed, to save test time, from the individual bit errors (ϵ), as shown below.

$$DLE_1 = \epsilon_1 - \sum_{2}^{12}\epsilon_i, \ldots, DLE_{12} = \epsilon_{12}. \qquad (1)$$

Now, what if superposition errors are not small? Unfortunately, there is no way to predict the input code where the maximum linearity error will occur. Therefore, it is necessary to test many code combinations, such as the tests shown in Table II, in order to approximate the worst case error. Bit interaction can be caused in many ways such as temperature gradients on a monolithic chip causing the magnitude of a bit output to be a function of the state of the other bit switches. A temperature gradient can cause the feedback resistor to appear to be nonlinear over the 0 to +10V output range (see Figure 9a). This apparent nonlinearity is due to variable power dissipation which can produce a 1°C to 2°C temperature gradient. This in turn changes the absolute value of the feedback resistor since it will have a temperature coefficient of between 50ppm and 300ppm/°C for a thin-film material and over 1000ppm/°C for a monolithic diffused resistor. Bit interaction can also be produced by varying voltage drops caused by changing current levels when critical portions of a circuit share the same metallization path such as on a monolithic chip, in a wire bond, the resistance of a socket, or the wiring resistance of a test circuit (see Figure 1).

Even though static testing with a DVM is a slow operation, it is a useful technique, especially when a new converter is being evaluated, for determining the peculiarities of the converter.

TABLE II. Measuring DAC Errors.

STEP	OPERATION	INPUT CODE	ACTUAL OUTPUT	IDEAL OUTPUT	ERROR mV	DIFF. LINEARITY ERROR mV	COMMENT
1	Offset Error	0000 0000 0000	+0.52mV	0.0	+0.52		S1, S2 Off
2	Full Scale Error	1111 1111 1111	9.9911	9.9976	-6.5		
3	Null Offset Error	0000 0000 0000	0.0	0.0	0.0		S1 On, Adj R1
4	Gain Error	1111 1111 1111	9.9908	9.9978	-7.0		
5	Null Gain Error	1111 1111 1111	10.2375	10.2376	0.0		S2 On Adj R2
6	Bit 12_A	0000 0000 0001	0.00250	0.0025	0		
7	Bit 11	0000 0000 0010	0.00500	0.0050	0		
8	Bit 10	0000 0000 0100	0.00998	0.0100	-0.02		Lower
9	Bit 9	0000 0000 1000	0.02001	0.0200	+0.01		Order
10	Bit 8	0000 0001 0000	0.0400	0.0400	0		Bit
11	Bit 7	0000 0010 0000	0.08004	0.0800	+0.04		Errors
12	Bit 6	0000 0100 0000	0.16005	0.1600	+0.05		
13	Bit 5	0000 1000 0000	0.32003	0.3200	+0.03		
14	1/16 FSR, Bit 4 Carry	0000 1111 1111 0001 0000 0000	0.63764 0.63998	0.6375 0.6400	+0.14 -0.02	-0.16	
15	1/8 FSR, Bit 3 Carry	0001 1111 1111 0010 0000 0000	1.27760 1.27961	1.2775 1.2800	+0.10 -0.39	-0.49	
16	3/16 FSR	0010 1111 1111 0011 0000 0000	1.91723 1.91962	1.9175 1.9200	-0.27 -0.38	-0.11	
17	1/4 FSR, Bit 2 Carry	0011 1111 1111 0100 0000 0000	2.55719 2.55974	2.5575 2.5600	-0.31 -0.26	+0.06	Linearity
18	5/16 FSR	0100 1111 1111 0101 0000 0000	3.19735 3.19970	3.1975 3.2000	-0.15 -0.30	-0.15	And
19	3/8 FSR	0101 1111 1111 0110 0000 0000	3.83730 3.83934	3.8375 3.8400	-0.20 -0.66	-0.46	Differential
20	7/16 FSR	0110 1111 1111 0111 0000 0000	4.47697 4.47936	4.4775 4.4800	-0.53 -0.64	-0.11	Linearity
21	1/2 FSR, Bit 1 Carry	0111 1111 1111 1000 0000 0000	5.11696 5.12049	5.1175 5.1200	-0.54 +0.49	+1.03	Errors
22	9/16 FSR	1000 1111 1111 1001 0000 0000	5.75814 5.76050	5.7575 5.7600	+0.64 +0.50	-0.14	at
23	5/8 FSR	1001 1111 1111 1010 0000 0000	6.39811 6.40014	6.3975 6.4000	+0.61 +0.14	-0.47	15 Evenly
24	11/16 FSR	1010 1111 1111 1011 0000 0000	7.03778 7.04015	7.0375 7.0400	+0.26 +0.15	-0.11	Spaced
25	3/4 FSR	1011 1111 1111 1100 0000 0000	7.67775 7.68029	7.6775 7.6800	+0.25 +0.29	+0.04	Code
26	13/16 FSR	1100 1111 1111 1101 0000 0000	8.31788 8.32027	8.3175 8.3200	+0.38 +0.27	-0.11	Carries
27	7/8 FSR	1101 1111 1111 1110 0000 0000	8.95784 8.95993	8.9575 8.9600	+0.34 +0.07	-0.41	
28	15/16 FSR	1110 1111 1111 1111 0000 0000	9.59753 9.59994	9.5975 9.6000	+0.03 -0.06	-0.09	

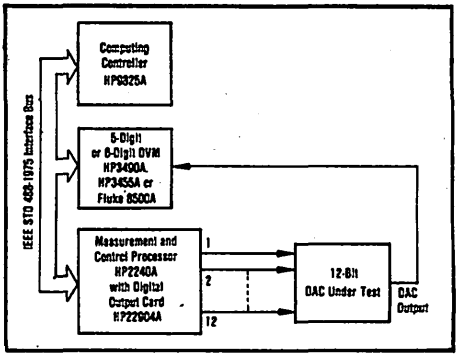


FIGURE 3. Automatic DAC Test Circuit Using a Computing Controller and a DVM.

AUTOMATIC TESTING WITH A DVM

Figure 3 illustrates one method of automating the manually performed tests described in the previous section. A computing controller directs the operation of both the DAC under test and the DVM via the IEEE Standard 488 Interface Bus. The computing controller can calculate and remove the effects of offset and gain errors so that adjustment potentiometers for the DAC are not required. This test system is easy to program with the high-level language of the computing controller. Of course, a microcomputer implementation is also possible but the high cost of developing assembly language software can be a disadvantage.

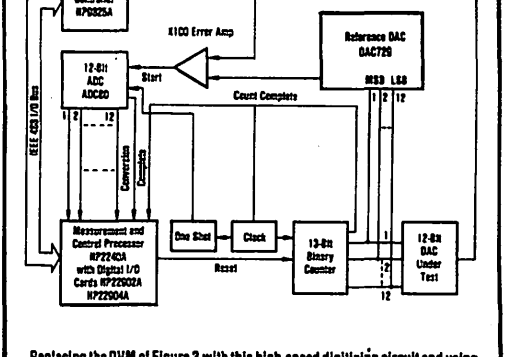
The speed of this system will be determined by the measurement speed of the DVM. At first glance, one might be inclined to assume that the speed limitation is simply the maximum number of readings per second of the DVM, which can range from 5 to 500 readings per second depending on the DVM used. However, the DAC output voltage will be updated between each reading of the DVM so that the maximum number of readings per second is determined by the internal settling time of the DVM to ±1 digit (±0.001% for a 5-digit DVM). Many manufacturers do not specify the settling time of their DVM so it must be determined experimentally. Typically, the settling time can range from 20msec to over 500msec for a step input change. Since testing all 2^n code combinations of a 12-bit DAC could take anywhere from one minute to several minutes depending on the speed of the DVM, short-cut methods such as in Table II may be required to increase the throughput rate.

DYNAMIC D/A CONVERTER TESTING

Since a DVM has a slow conversion speed, the circuits described in this section do not utilize a DVM. Most of the testers described will use a reference DAC and an oscilloscope to display the errors. Circuits to measure DAC output settling time are also included.

Fast-Computing Controller

Replacing the DVM of Figure 3 by the circuit of Figure 4 permits a decrease in each conversion period to 100μsec or less. The reference DAC should have a linearity error specification of ±0.0015% (±1/2LSB for a 15-bit DAC). The reference DAC and the X100 error amplifiers should have a combined settling time of less than 50μsec. To



Replacing the DVM of Figure 3 with this high-speed digitizing circuit and using the high-speed interrupt capability of the computing controller reduces the measurement period to less than 100μsec.

FIGURE 4. High Speed Digitizing Circuit.

prevent the error amplifier from saturating, the DAC under test must have offset and full scale errors of less than ±100mV. The 12-bit ADC80 will digitize the error signal in 25μsec to a resolution of ±1LSB or ±4.88mV. This provides a resolution of 4.88mV/100 or 50μV referred to the DAC output.

This system is capable of testing all 2^n codes of a 12-bit DAC and computing the offset, full scale, gain, linearity, and differential linearity errors in approximately 1sec, therefore, it is not necessary to wait for the converter to warm up before making measurements, unless the total error of the DAC is required. Total error (or absolute accuracy) is the worst case deviation from an ideal DAC output when the combined effects of offset, gain, and linearity errors are considered. Total error is an important parameter in applications where offset and gain adjustment potentiometers cannot be used.

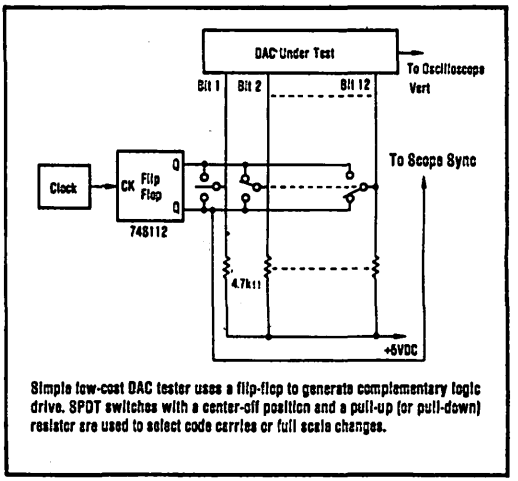
Differential Linearity Error

The low cost tester in Figure 5 will test a DAC for differential linearity error, monotonicity (an increasing output voltage for an increasing digital code), glitches, full-scale settling time when used in conjunction with one of the circuits in Figure 6, and will provide a clue about a converter's linearity error. Differential linearity error is an important parameter for many applications such as CRT graphic displays which require uniform spacing of the output voltages of a DAC.

The test sequence begins by testing the major carry at the MSB by selecting the code 100 · · · 000 with the bit switches. This circuit produces an alternating input code of 100 · · · 000 and 011 · · · 111 to the DAC so that all bits are changing states. To test the carry at bit 2, bit 1 switch is placed in the center off position and bit 2 switch is turned on. This procedure is repeated for each bit. The DAC output is AC coupled to an oscilloscope to observe the deviation from an ideal 1LSB change. If the DAC has a differential linearity specification of ±1/2 LSB, then the DAC output step will increase anywhere from 1/2LSB to 3/2LSB when the digital code increases by one binary count.

One can also test glitches (switching transients) to determine their amplitude and settling time. Glitches, which are caused by unequal turn-on and turn-off times of the internal switching circuits of the DAC, will be worse at a digital code carry, usually the MSB. Since digital data skew can also cause glitches, a Schottky TTL flip-flop is used in Figure 5 to minimize the data skew.

Testing differential linearity error is very convenient in that it requires no accurate measurement standards. In a sense the DAC under test is its own measurement standard since each bit is compared to the sum of the lower order bits. But what conclusions about the linearity error of the DAC can be reached? This test does give an indication of the linearity error of a DAC, but unfortunately, it does not give the actual linearity error nor does it set a bound on the linearity error. It is possible to compute the linearity error by using the equations of (1) in reverse starting at the LSB since $DLE_{12} = \epsilon_{12}$. This method, however, is not too accurate because of the acccumulation of errors resulting from "eye-balling" the differential linearity errors from the oscilloscope.



Simple low-cost DAC tester uses a flip-flop to generate complementary logic drive. SPDT switches with a center-off position and a pull-up (or pull-down) resistor are used to select code carries or full scale changes.

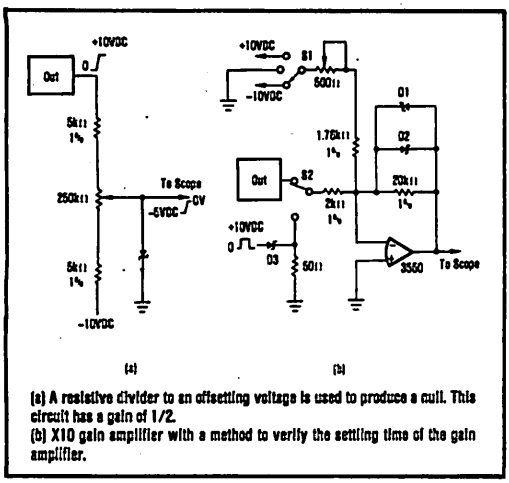
FIGURE 5. Low Cost DAC Tester.

It can be shown that the linearity error of a DAC will suffer if the sign of the differential linearity errors alternate starting at the MSB. For example, a DAC with differential linearity errors $DLE_1 = +1/2LSB$, $DLE_2 = -1/2LSB$, and $DLE_3 = +1/2LSB$ will automatically have greater than ±1/2LSB linearity error even if the other code carries have zero differential linearity errors. Therefore, we can conclude the following: if the differential linearity errors at the code carries are small (less than ±1/4LSB, with at most only two carries as large as ±1/2LSB provided their signs do not alternate), then the converter's linearity error will be less than ±1 2LSB. These comments assume, of course, that superposition errors are small.

Full-Scale Settling Time

An attempt to measure full scale settling time can be a tricky proposition since we are attempting to resolve the DAC output settling to within ±1/2LSB (±1.2mV for a 12-bit DAC) of the final value of a 10V step change. Measuring the DAC output directly is impractical as most oscilloscopes have a terrible overload recovery time, which could be confused for the settling time of the DAC. Therefore, a circuit such as shown in Figure 6a is required that provides clamping and a level shifting bias arrangement to shift the full scale DAC output signal close to ground potential. Even with the Schottky diodes clamping the oscilloscope input at ±0.5V, some scopes will overload on their 2mV/division or even their 5mV/division input sensitivity. If this is the case, some amplification as in Figure 6b will be necessary so that the scope can be operated at 10mV or 20mV/division, which usually cures the overload problem.

Now we must be sure that the settling time of the X10 amplifier in Figure 6b is small compared with the settling time of the DAC. The settling time of the amplifier can be



(a) A resistive divider to an offsetting voltage is used to produce a null. This circuit has a gain of 1/2.
(b) X10 gain amplifier with a method to verify the settling time of the gain amplifier.

FIGURE 6. Circuits for Measuring Settling Time.

tested by switching S1 to the ground position and S2 to the external pulse generator position. Applying a +10V pulse will clamp the amplifier output at -0.5V. When the input pulse returns to zero, D3 will zero-bias and the amplifier output should settle to ±1/2LSB (±6mV for testing a 12-bit DAC and an amplifier gain of 10) in less than 1μsec provided the amplifier does not have a second-order long term settling time problem. If we approximate the combined settling time of the X10 gain amplifier as the square root of the sum of the squares, we find that the error caused by the settling time of the amplifier is small enough to ignore when the settling time of the DAC is greater than 2μsec.

Automatic Linearity Tester

Test circuits that rapidly determine if a DAC meets its important specifications can be a real time saver especially when a large number of converters must be tested. The circuit in Figure 7 automatically tests linearity error as well as offset and gain errors. In the first two time intervals of the test sequence the offset and gain errors are removed by the two integrate/hold amplifiers in a servo loop which automatically adjusts the offset and full scale outputs of the reference DAC to agree with the DAC under test. Next, the falling edge of the second one-shot starts an oscillator which clocks both successive approximation registers (SAR_1 and SAR_2) in parallel.

The multiplexer selects SAR_1 which functions as a shift register to sequence through the bits of both DAC's. The output of the X10 error amplifier drives a comparator to provide input data so that SAR_1, will store the bits which have positive error. After each bit has been examined, the multiplier selects SAR_2 and the exclusive-OR complements the digital word. This complemented digital word turns on the bits that have negative error so that the worst case negative linearity error is displayed. Finally the exclusive-OR allows the output of SAR_2 to pass straight through so that the worst case positive linearity error is displayed.

It is also possible to display the offset and the full scale errors of the DAC under test. Simply turn off the two integrators by opening switches S1 and S2 so that the offset and gain errors are no longer nulled during the first two time intervals. To display gain error, turn on the auto zero integrator so that the offset error is removed from the full scale error. An alternate method of determining the offset and gain errors is to measure the output voltage of each integrator as this voltage is directly proportional to the error.

Full Dynamic Test

When the superposition errors of a DAC are not small due to one of the reasons discussed in "Tests Using a DVM", the short-cut methods for measuring linearity error such as in Figure 7 do not work. If a high speed measurement circuit is available which can display each bit error, then testing all 2^n code combinations is a good alternative.

Figure 8 shows a simple implementation of this type tester. The binary counter has n + 1 stages to implement a binary count from 0 to 2^n - 1 and to reset the counters at the end of the count. The reference DAC and the X10 error amplifier must have combined settling times to ±1/10LSB of less than 10μsec as the system clock must operate at 20kHz to have a flicker-free display. For a 12-bit converter, a complete cycle takes 50μsec × 4096 counts or approximately 200msec. The output of the nth counter stage is also displayed on the scope to indicate the mid-scale transition point. Offset and gain adjustment potentiometers are provided to zero the end points of the error display.

This tester works well for 8-, 9-, and 10-bit converters. For a 12-bit DAC, the 4096 segments that are displayed on a CRT are spaced so close together that the switching transients create a wide band of noise so that it is difficult to tell if the converter meets its specification, especially when the linearity error is near the ±1/2LSB limit. One way around this problem if we assume that the errors contributed by the last four bits of the DAC are small, is to inhibit these bits with the AND gates shown in Figure 8. This reduces the binary count to 256 and also gives each count 16 times longer for the glitches to settle out.

Other improvements that can be made to this tester are automatic offset and gain error nulling, a sample hold deglitcher to remove the glitches at the error output and a GO/NO GO window comparator to test the linearity error at each binary count.

The oscilloscope photographs in Figure 9 show two different 12-bit DAC functions. The first converter has superposition errors (in addition to the errors created by the individual bit errors) due to self-heating of its feedback resistor causing the DAC to appear nonlinear. A simple method to determine if the feedback resistor is at fault is to substitute a low TCR resistor for the internal feedback resistor of the DAC and see if the nonlinearity disappears. Figure 9b demonstrates the symmetrical error patterns that are produced when a DAC has low superposition errors (see Figure 2).

Figure 9a is a good example to show the effect of specifying linearity error as the maximum deviation from a best straight-line fit rather than a straight line through the end points. It is apparent for this example that a linearity error specification of ±1/2LSB is easier to meet when the best straight-line method is used. Since Figure 9b has symmetrical error patterns, a straight line through the end points is the same as a best straight-line fit.

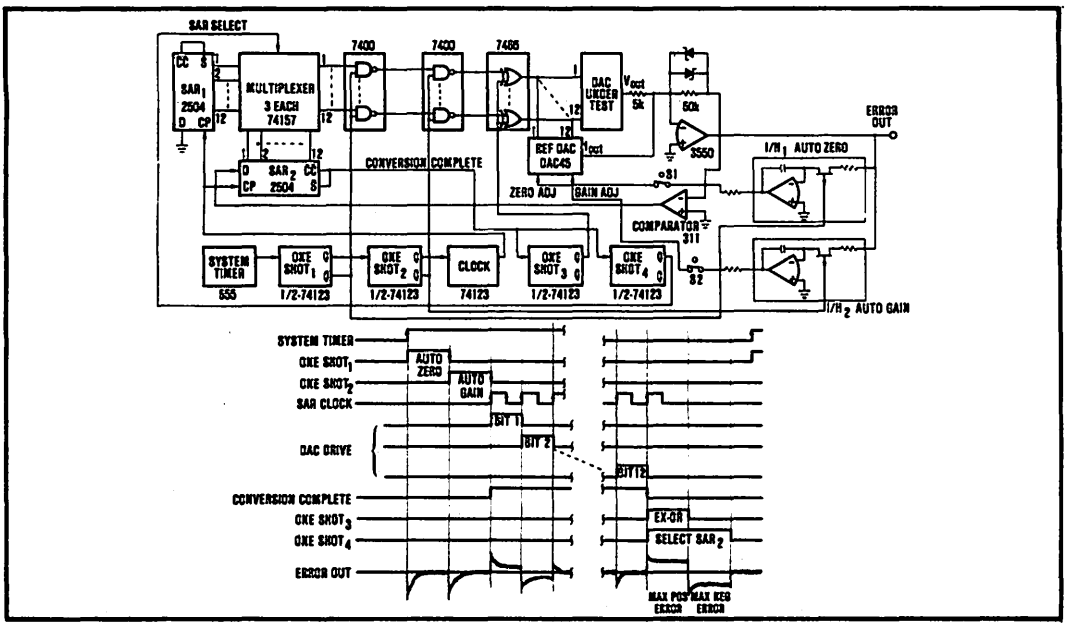


FIGURE 7. Automatic Linearity Tester.

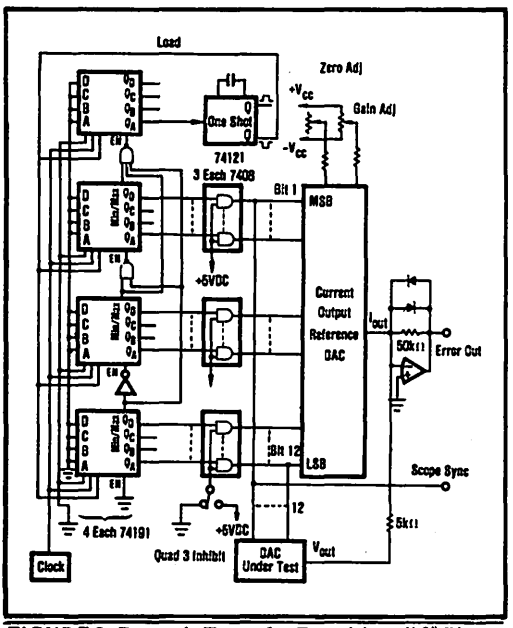
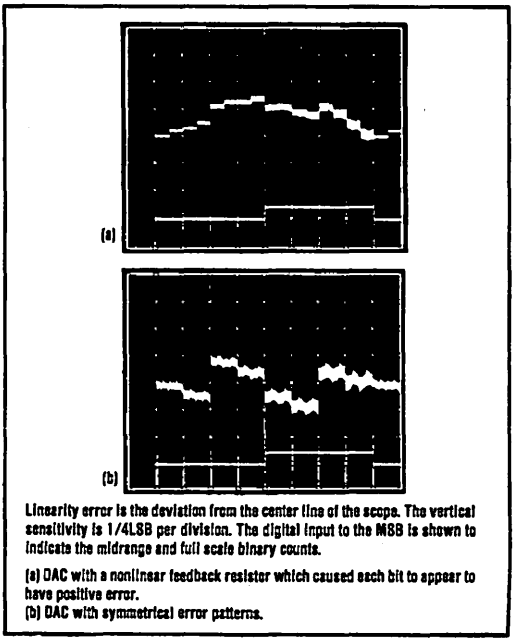


FIGURE 8. Dynamic Tester for Exercising all 2^n Binary Codes.



Linearity error is the deviation from the center line of the scope. The vertical sensitivity is 1/4LSB per division. The digital input to the MSB is shown to indicate the midrange and full scale binary counts.

(a) DAC with a nonlinear feedback resistor which caused each bit to appear to have positive error.
(b) DAC with symmetrical error patterns.

FIGURE 9. Superposition and Symmetrical Errors.

TESTING OF ANALOG-TO-DIGITAL CONVERTERS

The test methods and test circuits that are described herein are mostly suitable for converters that have conversion times of less than 100μsec, such as the successive approximation converter. These dynamic testers are not adaptable for integrating converters which have conversion rates in the tens or hundreds of milliseconds and display a converter's error on an oscilloscope. Before actual test methods are described, some of the characteristics of an analog-to-digital converter (ADC) should be covered. The transfer functions are shown in Figures 2 and 3 apply in particular to the successive approximation converter and the counter converter which employ a DAC and a comparator in a feedback loop with control logic.

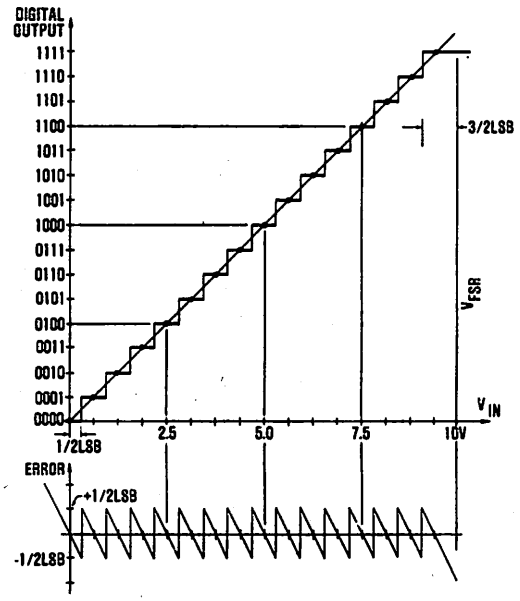


FIGURE 1. Transfer Function and Error Plot for an Ideal 4-bit ADC.

Figure 1 shows the transfer function of an ideal 4-bit ADC. Each step of the transfer function is a uniform 1LSB wide. If the first output code transition (code change from 0000 to 0001) is adjusted to occur at an input voltage of $\pm$1/2LSB and the last transition (1110 to 1111) to occur at -3/2LSB below the full-scale range voltage (FSR), then the center of each step will occur at the same voltage as the output of an ideal 4-bit DAC. These ideal DAC output points are shown by the dots at the center of each step in Figure 1.

As can be seen by Figure 1 these +5V inputs between $\pm$1/2LSB ($\pm$0.312V) will produce the output code of 1000, or in other words, if a converter had an output code of 1000 there is a $\pm$0.312V ($\pm$1/2LSB) uncertainty that the input is exactly 5V. This uncertainty of $\pm$1/2LSB is called the quantizing error which is inherent of all ADC's. When an ADC has a linearity error specification of $\pm$1/2LSB the total uncertainty increases to $\pm$1LSB — the total sum of the quantizing error plus the linearity error.

Linearity error can be defined as the amount the input voltage must deviate from the theoretical transfer function when offset and gain errors have been removed. If the DAC that is used in an ADC is nonlinear, the step size will deviate from the ideal 1LSB step size and the

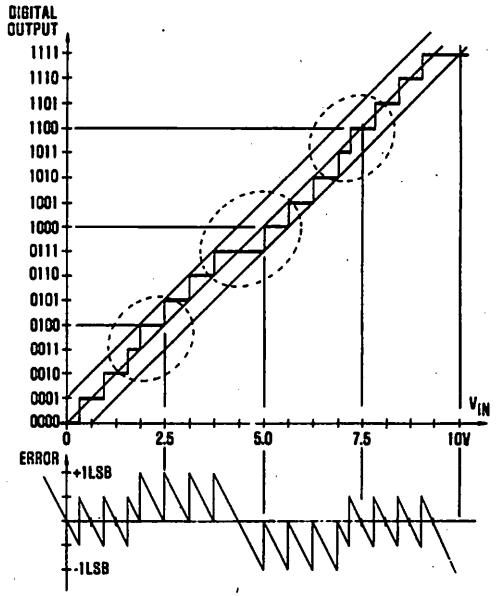


FIGURE 2. Transfer Function and Error Plot for an ADC which Contains a DAC with Individual Bit Error of $\epsilon_1 = +1/2$LSB, $\epsilon_2 = -1/2$LSB, $\epsilon_3 = 0$, and $\epsilon_4 = 0$.

transition voltages will shift from the ideal transition voltage. The maximum linearity error of an ADC can be determined by finding the worst case deviation from the ideal transition voltage and the differential linearity error can be found by finding the step size with the largest deviation from the ideal 1LSB step size. Another method used by some manufacturers for measuring linearity error is to compute the difference between the actual and the ideal center of each step on the average of several steps.

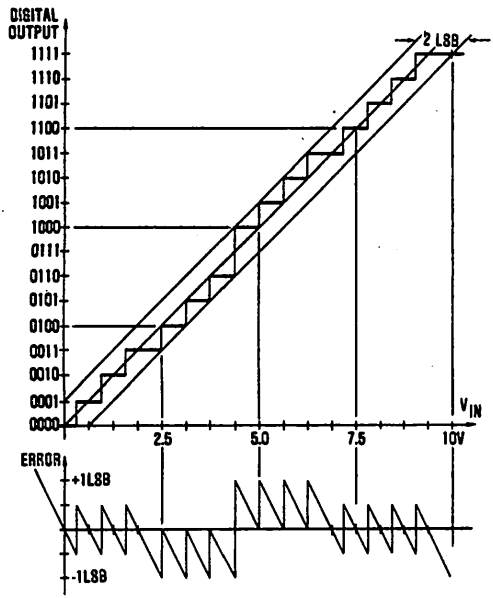


FIGURE 3. Transfer Function and Error Plot for an ADC which Contains a DAC with Individual Bit Errors of $\epsilon_1 = -1/2LSB$, $\epsilon_2 = +1/2LSB$, $\epsilon_3 = 0$, and $\epsilon_4 = 0$.

The transfer function in Figure 2 is produced by an ADC with an internal DAC having individual bit error of $\epsilon_1 = +1/2LSB$, $\epsilon_2 = -1/2LSB$, $\epsilon_3 = 0$, and $\epsilon_4 = 0$. The worst case differential linearity error of +1LSB occurs at the code 0111 and the transition voltages are shifted -1/2LSB at four codes below the midrange input voltage and +1/2LSB at four codes above midrange.

When the bit errors of the internal DAC have the opposite sign, namely $\epsilon_1 = -1/2LSB$, $\epsilon_2 = +1/2LSB$, $\epsilon_3 = 0$, and $\epsilon_4 = 0$, the transfer function of Figure 3 is produced. Notice the missing code at 0111 (DLE = -1LSB) and that the transition voltages are shifted in the opposite direction. Both of these examples demonstrate that the worst case differential linearity error is bounded by two times the linearity error. The reverse of this statement is not true.

The dotted areas of Figure 2 demonstrate that changes in differential linearity errors and hence, changes in the linearity errors, take place at the code carriers. Since the "real action" takes place at the code carries, we can avoid testing all 2^n steps of an ADC by examining the errors at the carrier. For example, at the MSB carry we must measure the transition voltages from 0110 to 0111 and from 0111 to 1000 in order to compute the differential linearity and the linearity errors. This technique is the basis for the tests in Table I.

In actual practice, the internal DAC must have better than ±1/2LSB linearity error because of the dynamic nature of the conversion process. If sufficient time is not allowed for the DAC and the internal comparator to fully settle (and usually this is the case to minimize the conversion time) the transition voltages will be shifted an additional amount. Now superposition errors are no longer small and the ADC should be tested at several code carriers to find the worst case errors. It can be shown that the shifts caused by dynamic errors will show up at the major code carriers, and, therefore, code transitions both above and below a major code transition point should be measured. To fully characterize the major carry at MSB, for example, one should measure the 0110→ 0111→ 1000→ 1001 transition voltages. Table I outlines this test method.

MANUAL TEST WITH DVM

Figure 4 shows a simple test circuit for manually testing an ADC. Manual testing can be used for any type ADC from very-fast parallel encoders to very-slow integrating converters.

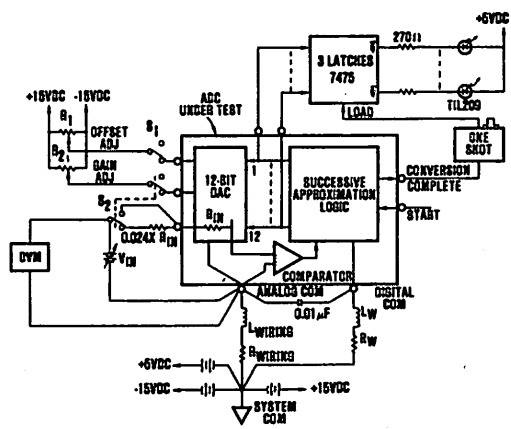


FIGURE 4. Manual ADC Test Circuit with DC Input Voltages, a DVM to Monitor the Input Voltage, and a LED Digital Code Display.

The input is a variable DC power supply and the digital output word is displayed by a bank of LED indicators. Because of the dynamic nature of the conversion process, proper wiring precautions are extremely important due to current pulses flowing through the wiring resistances and inductances. To minimize possible noise and/or hysteresis at the transition voltages of the ADC, the recommended layout procedures which are given in most manufacturer's data sheets should be closely followed. These procedures usually include proper supply bypassing the wiring, and, in some cases, use of a bypass

capacitor. The capacitor is connected between the analog and digital commons to turn differential signals into common-mode signals to prevent digital noise from feeding through the DAC to the comparator.

The test procedures involve varying the DC input voltage with the ADC continually converting until the appropriate LED indicators flicker with approximately a 50 percent duty cycle between the digital codes on either side of a transition voltage.

Table I outlines the test procedure to measure offset, full-scale, gain, linearity, and differential linearity errors. For a successive approximation ADC we must measure the transition voltage above and below the code of interest since the transition voltage can be shifted due to

TABLE I. Measuring ADC Transition Voltages.

STEP	OPERATION	CODE TRANSITIONS	IDEAL INPUT	ACTUAL INPUT	ERROR	DIFF LIN ERROR	COMMENT
1	OFFSET ERROR	0000 0000 0000 0000 0000 0001	+1.22mV		e_o		S1, S2 OFF
2	FULL SCALE ERROR	1111 1111 1110 1111 1111 1111	+9.9964V		e_{FS}		$e_{GAIN} = e_{FS} - e_o$
3	NULL OFFSET ERROR	0000 0000 0000 0000 0000 0001	+2.5mV	+2.5mV	0		S1 ON, ADJ R1
4	NULL GAIN ERROR	1111 1111 1110 1111 1111 1111	+10.2375V	+10.2375V	0		S2 ON, ADJ R2
5	BIT 11 CARRIES	0000 0000 0001 0000 0000 0010 0000 0000 0011	5.0mV 7.5mV		e_A e_B	$e_A - e_B$	
6	BIT 10 CARRIES	0000 0000 0010 0000 0000 0011 0000 0000 0100 0000 0000 0101	7.5mV 10.0mV 12.5mV		e_C e_D e_E	$e_C - e_D$ $e_D - e_E$	ERRORS AT THE LOWER ORDER BITS
7	BIT 9	0000 0000 0110 0000 0000 0111 0000 0000 1000 0000 0000 1001	17.5mV 20.0mV 22.5mV				
	⋮			⋮			
13	BIT 3 CARRIES 1/8 FSR	0001 1111 1110 0001 1111 1111 0010 0000 0000 0010 0000 0001	1.2775V 1.2800 1.2825				LINEARITY AND DIFFERENTIAL LINEARITY ERROR AT 7 EVENLY SPACED CODE CARRIES
14	BIT 2 CARRIES 1/4 FSR	0011 1111 1110 0011 1111 1111 0100 0000 0000 0100 0000 0001	2.5575 2.5600 2.5625				
15	3/8 FSR	0101 1111 1110 0101 1111 1111 0110 0000 0000 0110 0000 0001	3.8375 3.8400 3.8425				
16	BIT 1 CARRIES 1/2 FSR	0111 1111 1110 0111 1111 1111 1000 0000 0000 1000 0000 0001	5.1175 5.1200 5.1225				
17	5/8 FSR	1001 1111 1110 1001 1111 1111 1010 0000 0000 1010 0000 0001	6.3975 6.4000 6.4025				
18	3/4 FSR	1011 1111 1110 1011 1111 1111 1100 0000 0000 1100 0000 0001	7.6775 7.6800 7.6825				
19	7/8 FSR	1101 1111 1110 1101 1111 1111 1110 0000 0000 1110 0000 0001	8.9575 8.9600 8.9625				

the dynamic errors of the conversion process in addition to shifts caused by the linearity errors of the internal DAC. The full-scale voltage has been increased to 10.2375V by adding a series resistance (Figure 4) to the input, which is 0.024 x R_{in}. This makes the ideal bit weights with 1LSB equal to 2.5mV, 5.0mV, 10mV...2.560V and finally 5.12V for the MSB; also the transfer function has deliberately been shifted by +1/2LSB when the offset adjustment is performed in step 3. Now the ideal transition voltages will occur at exactly the same voltage as the output voltages of an ideal 12-bit DAC.

Notice in step 2 of Table I that the gain is calculated, instead of being measured, by substracting the offset error from the full-scale error. In order to save space in Table I, part of the steps have been omitted and only 7 evenly spaced carry points are shown. In actual practice 15, 31, or even 63 evenly spaced code carries should be measured if the ADC being tested has excessive superposition errors.

It should be apparent that testing an ADC manually will be a very time-consuming process, perhaps by a factor of 10 over testing a DAC, due to the increased number of data points required and because the input voltage must be slowly varied to find the transition voltages.

To speed up this manual adjustment process of finding transition voltages, a servo loop can be used to automatically adjust the input voltage. Yet another scheme would employ, for example, a computer-controlled DAC to gradually increase the input voltage to the ADC under test by a fractional part of an LSB and note the input voltage when a code transition occurs.

Instead of measuring transition voltages, another test method is sometimes used. The ideal center voltage of each step is applied to the input of the ADC and the resultant output code is compared to the ideal output

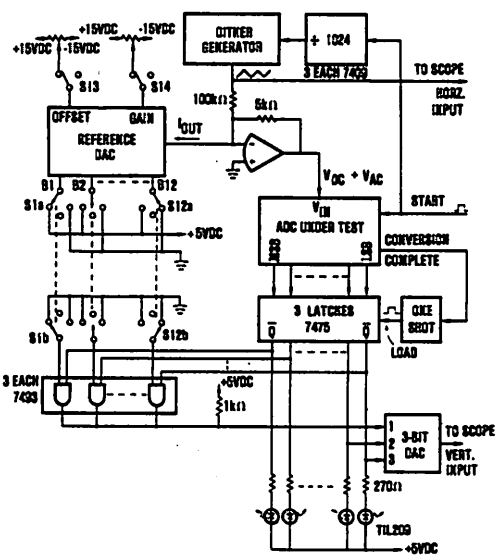


FIGURE 5. Dynamic Transfer Function Test Circuit.

code. If the maximum linearity error of the ADC is ±1/2LSB, the resultant output code will always be within ±1 count. This test gives an indication of the quality of an ADC, but is does not uncover some of the possible anomalies of the converter's transfer function. After studying the examples in Figures 2 and 3, it should be apparent that a converter can pass a ±1 count test and still exhibit the following anomalies: greater than ±1/2LSB linearity error, missing codes, nonmonotonicity, hysteresis, and noisy transitions. Examples of these anomalies are given in the next section.

DYNAMIC TRANSFER FUNCTION TESTER

The test circuit shown in Figure 5 can rapidly display an eight-code segment of the transfer function of an ADC. All of the tests of Table I that were done manually can now be quickly performed. In addition, much more information is available concerning the quality of the ADC under test than is provided by the tests of Table I. For example, one can readily spot a noisy transition, alternations between codes, hysteresis, missing codes, and nonmonotonicity in addition to offset, gain, linearity, and differential linearity errors. In other words, the transfer function displayed on an oscilloscope provides an almost totally complete picture of the characteristics of the ADC.

The input voltage to the ADC in Figure 5 is a triangle waveform superimposed on a DC voltage from a reference DAC. The rate of change of the triangle waveform is small enough during each conversion period of the ADC so that a sample/hold circuit ahead of the ADC is not required. The triangle waveform should be synchronized to the start convert command of the ADC to prevent any jitter in the scope display. A good figure is 1024 conversions per cycle of the triangle waveform.

This tester works on the principle that the lower order bits have repeating binary code patterns as shown in Figure 6 (a). If the last two bits of an ADC are connected to a 2-bit DAC, the output of the DAC will generate the repeating four-level staircase waveform shown in Figure 6 (b). Unfortunately, all of the repeating staircase waveforms look alike so it is possible to confuse which staircase represents the specific "code carry of interest."

An improvement is shown in Figure 6 (c) which serves to identify the "code carry of interest." The MSB of a 3-bit DAC is connected to the appropriate bit output line of the ADC (bit 2 for this example). The result as shown in Figure 6 (c) is a shifted staircase with eight levels instead of only four levels when bit 2 becomes true at 1/4 of full scale (bit 2 also becomes true at 3/4 of full scale). The open collector AND gates and the center-off DPDT bit switches of Figure 5 are used to implement this shifting feature which is activated when a bit switch corresponding to a specific "code carry of interest" is placed in the center-off position.

Before testing an ADC, the oscilloscope should be calibrated so that the beam position (when the inputs are shorted) is at the position shown by the dot in Figure 6 (d) and both the vertical and horizontal gains are adjusted to equal 1LSB per division. With the scope calibrated, an

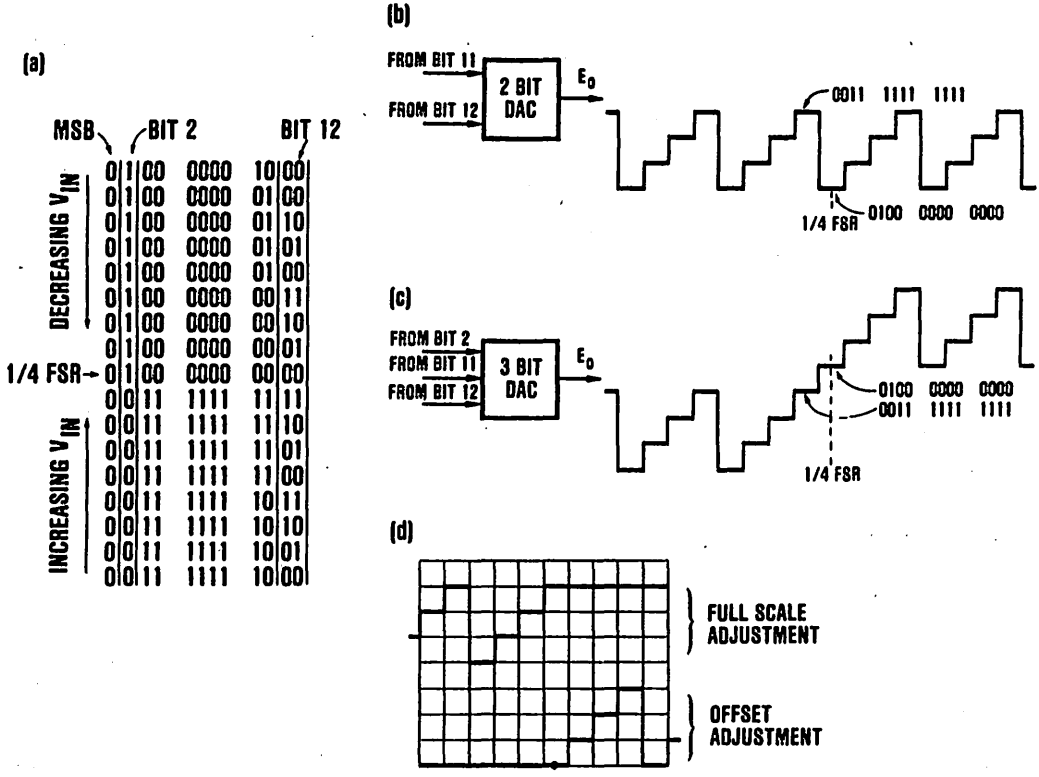


FIGURE 6. Basis for the Dynamic Transfer Function Tester of Figure 5. (a) Repeating binary codes in the last two bits of an ADC output code for an input dither voltage at 1/4 of the full-scale range voltage. (b) Staircase waveform from a 2-bit DAC. (c) Shifted staircase waveform when the MSB of a 3-bit DAC is connected to the appropriate output of the ADC. (d) Offset and full-scale adjustments prior to examining the ADC transfer function.

ideal transfer function will be positioned on the graticule lines of the oscilloscope as shown in Figure 7 (a).

To measure linearity error, the end points of the transfer function are adjusted with the offset and gain adjustment potentiometers to the positions shown in Figure 6 (d). The transfer function at the "code carry of interest" is selected by the bit switches and the linearity error is measured as the deviation from the ideal transition voltages. Differential linearity error is the deviation from the ideal 1LSB step size. To measure gain error, the gain adjustment potentiometer is removed by opening switch S14 and the deviation of the full-scale transition point from the ideal (Figure 6 (d)) is noted. In the same manner, offset error is measured by removing the offset adjustment with switch S13.

Several examples of 12-bit ADC transfer functions are shown in Figure 7 to demonstrate the effects of hysteresis, a missing code, noise, and alternations.

DYNAMIC ERROR PLOT

The test circuit shown in Figure 8 differs from the previous test circuits since a full n-bit DAC (instead of a 3-bit DAC) is used to reconstruct the analog input signal. This DAC should be at least ten times more linear than the ADC under test since an error amplifier is used to accurately create the difference between the input signal to the ADC and the output signal from the DAC. The output of the error amplifier will be the sum of the converter's inherent ±1/2LSB quantizing error and its linearity error (for example, see the error plots of Figures 2 and 3). Differential linearity errors show up in an error plot as the deviation from an ideal 1LSB change in the ramp portion of each sawtooth waveform. Any phase shift between the input signal to the ADC and the delayed output signal of the DAC will produce an additional error term in the error plot, namely, an undesirable small-amplitude sine wave. Therefore, the frequency of the input signal must be low enough to minimize this undesirable signal.

Figure 8 (a) shows the error plot of an 8-bit ADC near the zero crossing of the input signal. The linearity and the differential linearity errors are very apparent. Figure 8 (b) illustrates the error plot at the peak of the sine-wave input. Notice the reversal of the sawtooth waveform

when the slope of the input signal changes sign.

Broad-band noise in the error output limits this test to 8-bit converters. To test greater than 10 bits will require high-pass filtering of the error signal and a reduction of the frequency of the input signal. Now a storage scope or a strip chart recorder will be required to record the error plot.

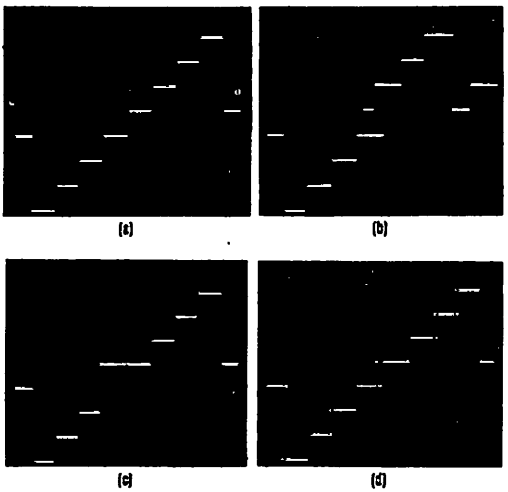


FIGURE 7. ADC Transfer Function Characteristics for a 12-bit Converter. (a) Near-perfect transfer function. (b) Hysteresis at the MSB code carry. Note the missing code 100...000 for V_{in} increasing, but when V_{in} decreases the code is not missing. (c) Near-perfect transfer function except for the missing code 011...111. (d) Noise and alternations (code reversals) near the transition voltages.

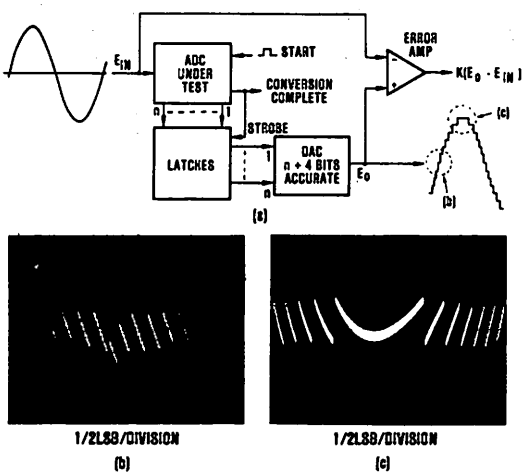


FIGURE 8. ADC Test Circuit. (a) Comparing E_{IN} and the ADC output which is converted back to an analog voltage with an accurate DAC. (b) Error at $E_{in} = 0$. (c) Error at plus full-scale input.

TEST CIRCUIT FOR HIGH-SPEED CONVERTERS

Figure 9 shows a circuit for testing high-speed converters with typically less than 10μsec conversion times. These high-speed converters will most likely use the successive approximation or the parallel-type conversion schemes. A unique feature of this tester is the full dynamic exercise given the ADC under test by digitizing the input waveform at points which are slightly greater than 180° out of phase. If alternate conversions are held in a latch the output DAC will produce a low-frequency duplicate of the input waveform. Since the input waveform will be changing more than a fractional part of an LSB during each conversion period, a good quality sample/hold is required to "freeze" the input to the ADC.

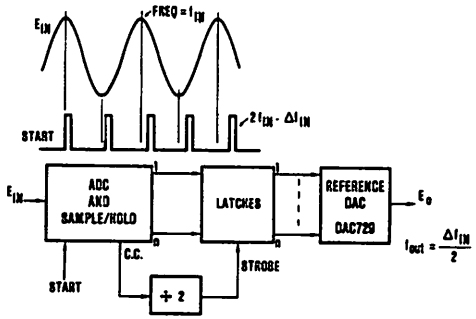


FIGURE 9. Test Circuit for a High-Speed ADC.

An example will best illustrate the maximum possible frequencies for the input and output waveforms. Consider a high-speed 12-bit ADC which has a conversion time (including the sample/hold acquisition time) of 1μsec. The output DAC will be updated every 2μsec as the latches are strobed at the completion of alternate conversions. Since it is desirable to test all 4096 output codes, the maximum output frequency will be 1/(4096 x 2μsec) or 122Hz. The maximum input frequency, since two samples per period are being taken, will be 500kHz. If the output signal is high-pass filtered, then the quality of the output waveform, which is a measure of the combined performance of the sample/hold and the ADC, can be measured with a harmonic distortion analyzer or a spectrum analyzer.

CONCLUSION

Several methods for testing ADC's and DAC's have been presented along with some of the unique properties of converters in an effort to broaden the perspective of the converter user. Obviously, test methods for many other converter parameters could have been included, but only the more commonly required tests have been covered.

Using the ideas discussed in this paper, the reader should be able to implement a test system best suited to his application.

OP AMP IMPROVES V/F CONVERTER'S INPUT

By adding an op amp to a V/F converter, you can combine the highly linear A/D-conversion capability of the converter and the high-impedance differential input of an instrumentation amplifier (IA). This approach eliminates the separate IA that is often required for preamplification and rejection of common-mode noise.

You connect the op amp to the input integrator of a charge-balance type of V/F converter (Figure 1). This combination leaves two high-impedance inputs, which impress their difference signal across the integrator's input resistor R_1. You choose that resistor value to set the V/F converter's gain as though it were an IA (For the VFC320 V/F converter shown, set the resistor value to produce 0.25mA for a full-scale differential input.). Then, choose the desired output pulse width (C_1 value) and the integrator output swing (C_2 value). For the component values shown, a 1V differential input will produce a 10kHz full-scale output. The relation is

$$F_O = (E_2 - E_1/(7.5R_1C_1).$$

A common-mode voltage will create no signal current in R_1, but it will shift the integrator's output, causing a change in trip-time for the following comparator. One V/F-converter cycle removes most of this timing error, however, because the integrator capacitor absorbs the common-mode voltage, and feedback via the reset current source restores the integrator's output. Moreover, during gain calibration the linear portion of the common-mode error disappears; only the nonlinear portion (approximately 10%) contributes to the overall nonlinearity. For this circuit, gain nonlinearity is 0.03% typical.

AC common-mode signals affect the timing of every V/F-converter cycle, but the net effect is 0, provided that the count period (for reading the V/F converter) is long compared to the period of the common-mode signal.

Because this technique increases the integrator's gain, it also increases the output offset and the gain nonlinearity. Gain nonlinearity, for example, increases according to (approximately) the V/F converter's normal 10V full-scale input range divided by the new full-scale value. Further, you are limited by the V/F converter's common-mode rejection capability (60dB) and common-mode range (−10 to 1V). To increase the common-mode range (to −5V to 10V), connect the op amp output to the V/F converter's common return (Figure 2). This connection also shifts the output pulses' zero level, so you may have to add the level-translating transistor Q_1.

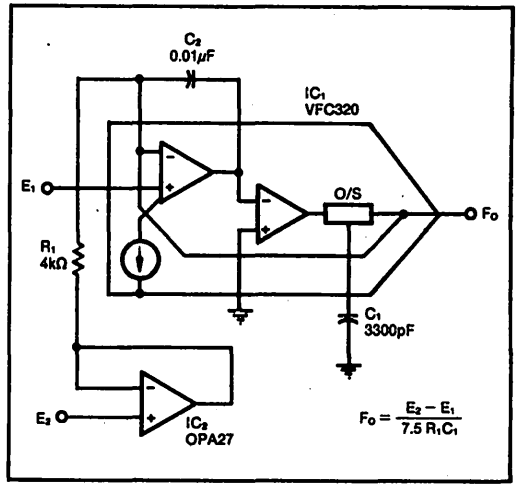


FIGURE 1. Adding an op amp (IC_2) provides a V/F converter (IC_1) with preamplification and high-impedance differential inputs.

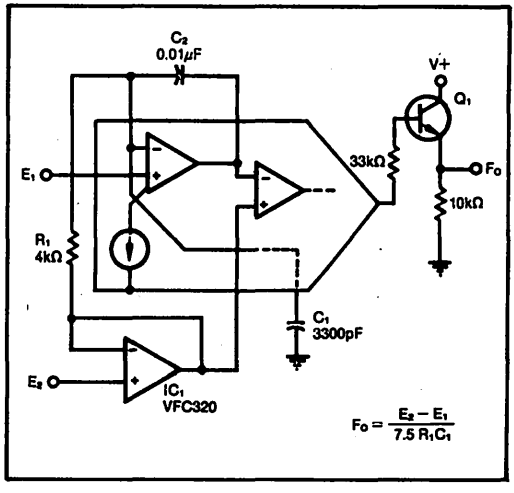


FIGURE 2. The connection here extendes the common-mode voltage range from −10 to 1V to −5 to 10V.

THROUGH CONTINUOUS INTEGRATION, V/F CONVERTER RAISES ACCURACY OF CUMULATIVE MEASUREMENTS

For systems demanding concise, fast cumulative measurements, a clocked voltage-to-frequency chip does the trick. Constantly integrating and multiplying, it delivers a product instantly.

In instrumentation and process control, many physical measurements—energy consumption, exposure to light, mechanical work—dictate cumulative operations. Individual readings must be summed or integrated either by numerical methods (using a microprocessor or computer) or by electronic integration.

The attributes of voltage-to-frequency converters, particularly charge-balancing devices, make them ideal candidates for cumulative measurements. The converters integrate an analog input by storing a charge in an integrating capacitor (Figure 1). When sufficient charge accumulates, a comparator trips, the charge drains from the capacitor during a reset period, and a one-shot generates an output pulse. Using a digital counter to tally successive pulses moves the integration process from the analog to the digital domain. Although the frequency output of a V/F converter is usually measured by counting its output for a fixed period of time, if the counter is never reset, the resulting measurement is an infinite or continuous integration. In such cases, the V/F converter doubles as an analog-to-digital (A/D) converter.

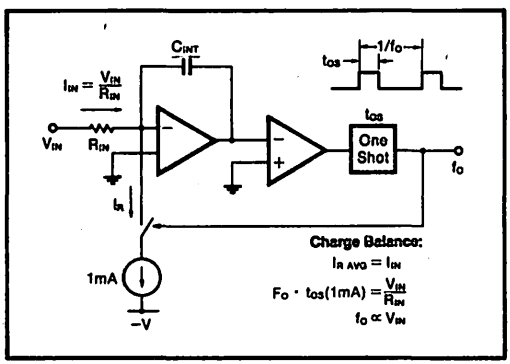


FIGURE 1. Each output pulse of the VFC100 voltage-to-frequency converter represents the receipt of a fixed quantity of charge at the integrator input. The integrating op amp integrates the applied voltage with respect to time. Counting the output pulses allows the integration to be carried out indefinitely in the digital domain.

Because of continuous integration, V/F converters sport distinct advantages over conventional A/D converters. For instance, successive-approximation A/D converters are inherently sampling devices. They can handle cumulative measurements with reasonable accuracy only by making frequent conversions and subsequent mathematical summations—two software-intensive requirements. Dual-slope converters integrate the input voltage only for a portion of the conversion cycle, typically 30% to 40%; thus they, too, may fall short in accuracy. Dual-slope devices that add an autozeroing cycle (so-called quad-slope types) integrate the input voltage for an even smaller percentage of the total conversion time. A V/F converter, however, provides that unique continuous integration when coupled with a digital counter.

The VFC100 charge-balancing V/F converter, which adapts well to cumulative measurements and also replaces several discrete logic and analog devices, conserves engineering design time and troubleshooting efforts.

The transfer function of the device:

$$f_{OUT} = \frac{V_{IN}}{20} \cdot f_{CLOCK}$$

makes circuit design straightforward by eliminating dependency on the critical one-shot capacitors, as required in previous V/F designs. Moreover, the transfer function provides an elegant means of multiplication. By making the converter's clock frequency depend on some variable, the chip's output is proportional to the product of the input voltage and the variable. The chip's continuous integration, combined with multiplication of two input variables, comes in handy for measuring power consumption and mechanical work. The design considerations posed by cumulative measurements move to the fore in a stationary bicycle—a fairly pedestrian application that nevertheless touches all facets of design. The principles it illustrates can easily extend to more prosaic, if not more productive, pursuits.

The total energy expended (for example, watt-hours or calories) is figured by integrating the product of rotational speed and torque. That product is the power developed, and the time integral of power is work.

A HANDLE ON TORQUE

On the stationary bicycle, brake friction, combined with the wheel's rotation, imposes a force on the brake assembly (Figure 2); a strain gauge measures the force by

sensing the opposing amount of force required to restrain the brake. The torque equals the force divided by the radius at which it is applied.

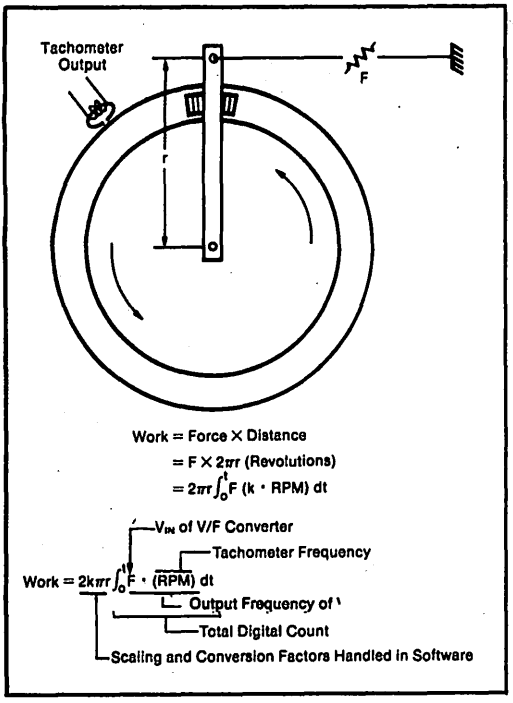


FIGURE 2. Instruments on the stationary bicycle measure the work done. The force required to restrain the brake assembly (which would otherwise be free to rotate with the wheel) is multiplied by the radius of the force, yielding the applied torque. The time integral of torque times speed is mechanical work.

The strain gauge is composed of a thin-film resistor pair; mechanical stress causes one resistor's value to rise while the other's falls. The gauge teams with two fixed precision resistors to form a bridge (Figure 3).

Gain drift is minimized by exciting the bridge from the V/F converter's internal 5V reference. Any residual drift on the reference voltage affects the converter's transfer function and the bridge output in an equal and opposite manner, reducing conversion drift to about 10ppm/°C. Resistor R_1 supplies approximately 7mA of the 10mA for the bridge; the 5V reference output supplies the remaining 3mA. Any initial imbalance in the bridge dominates all other voltage offsets in the system and must be adjusted—here, with R_5.

With the brake exerting a full-scale force of 20 lb on the strain gauge, the bridge puts out a mere 5mV and thus needs amplification. A precision instrumentation amplifier also rejects the bridge's 2.5V common-mode output voltage. Furthermore, its internal tracking resistors preserve gain accuracy. Since the gain is pin-programmed for 1000, a full-scale bridge output yields a 5V input to the V/F converter—a figure well within the device's 10V maximum linear input, yet with room to spare for overrange force peaks.

A PRERECORDED MESSAGE

Rotational velocity is sensed by a magnetic tape fastened to the circumference of the wheel and on which a steady tone has been recorded. A magnetic head positioned near the wheel senses a frequency that is proportional to the wheel's speed. The signal, approximately 20mVp-p, is applied to comparator A_1 to create logic-level pulses. A small amount of hysteresis, supplied by resistors R_6 and R_8, rejects noise and prevents multiple triggering. To further enhance the ability of comparator A_1 to trigger on small signals without producing double pulses or oscillations, R_7 and C_2 momentarily contribute additional hysteresis after an output transition.

The analog and digital worlds meet at the V/F converter. As with an A/D converter, the grounding procedures at this critical interface ultimately determine the system's accuracy. Special internal circuit techniques isolate digital and analog signals to achieve a linearity typically 0.01% at 100kHz (full scale). Since improper grounding can compromise the internal signal isolation, analog and digital ground lines should be separated near sensitive analog input circuitry.

SPLITTING GROUND

The meaning of "separate grounds" is often vague, since analog and digital grounds are rarely truly separate. Most often, "separate" means that the analog and digital ground buses join at only one point and only at a point where interaction is minimal (Figure 3 again). In this case, the two grounds separate at the connector of the analog input and V/F circuit board.

The system's analog ground runs to the appropriate contact on the V/F converter and the associated power-supply bypassing capacitors. The analog ground line continues to the common side of the bridge sensor, since the 5V V_{REF} output that excites the bridge is set relative to analog ground. The V/F converter's high-input-impedance ground reference connects directly to the output ground references of the instrumentation amplifier. The arrangement avoids the ground-drop errors caused by varying currents in the instrumentation amplifier's output reference pin or the voltage drops caused by bridge excitation current.

Digital ground lines pair up closely with lines carrying an opposing return current. For instance, the output of the VF converter, F_{OUT}, runs parallel to the digital ground return line. Fast-changing digital currents flowing in this loop are thus denied a large antenna that might radiate interference. Similarly, the rpm sensing circuitry and its output are given a separate ground return line to avoid radiation. The clock coming from A_1 serves as the input to the VF chip and does not require a similar return current path, since its input impedance is very high and the currents are very low.

The chip's transfer function produces accurate multiplication—provided the integrator amplifier operates in a linear fashion. If the integrator's output voltage swing is too large and saturates, accuracy drops. With a constant clock frequency (as is the case in most applications), the

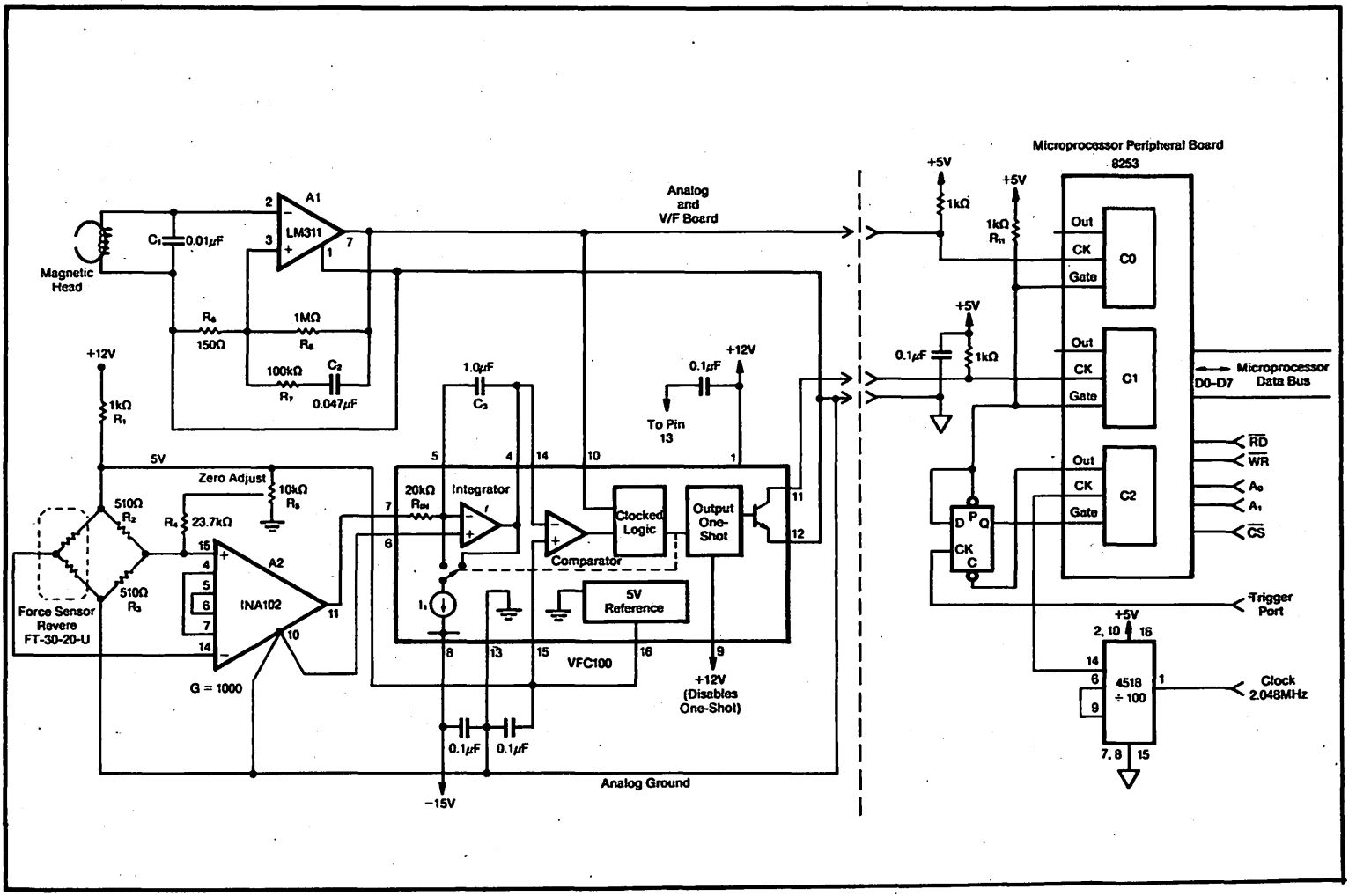


FIGURE 3. The output from the comparator, which reads the rotational speed of the wheel, serves as the clock input to the V/F converter. The strain gauge output, fed through an instrumentation amplifier, is then applied to the V/F converter. Counter outputs are applied to a microprocessor to produce—under program control—the power, torque, and rpm developed.

integrator voltage swing remains nearly constant over the full input range of 0 to 10V. In this multiplying circuit, however, it varies inversely with changes in the clock frequency.

The limit for accurate multiplication is set by the lowest expected clock frequency, since the largest integrator voltage swing arises at that frequency. As a result, the integrating capacitor must be large enough to keep the integrator amplifier's output swing linear. The special design of the high-speed integrator op amp limits its output swing to approximately 0 to $V_S - 2V$.

The integrator voltage swing centers on the 5V offset voltage applied to the noninverting comparator input, leaving a positive or negative integration range of 5V. The maximum integration time equals the time required for the reference reset current (1mA) to charge the integrating capacitor to 5V:

$$T = (1\mu F/1mA) \cdot 5V = 5ms$$

Thus for accurate multiplication, the clock frequency from the rpm sensor must be greater than $(5ms)^{-1}$, or 200Hz.

Usually, there is a value of the crank rotation speed below which accurate multiplication is not required. In this instance, a 200Hz clock frequency corresponds to a very slow crank rotation of 5rpm. Even though chances are that no significant time would be spent at or below that rate, it is important that designers should keep in mind the type of errors that occur in passing through this region.

The limited integrator voltage range causes the V/F converter to behave as if a minimum, 200Hz clock frequency were present. Therefore any positive offset evident at the input to the V/F converter when no force is being applied to the strain gauge is multiplied by a constant 5rpm. That offset error can be reduced by using a larger value for the integrating capacitor, together with accurate trimming of the bridge offset voltage. A small negative offset, set with R_2, ensures that no output pulses are generated at zero torque and zero rpm.

The accurcy of the total conversion, including multiplication, depends on the highest clock frequency entering the converter. Second-order effects cause the transfer-function gain to change slightly as clock frequency varies, producing small errors in the multiplication. For clock frequencies below 100kHz, gain typically varies less than 0.1%, leading to very accurate multiplication when compared to transconductance-type multipliers.

A 16-bit counter-timer, actually an 8253 microprocessor peripheral, digitally counts the device's output. Its three internal counters serve separate purposes: CT_0 counts pulses from the rotation sensor's comparator, A_1; CT_1 counts the V/F converter's output pulses. Finally, CT_2 counts the microprocessor clock frequency for a timer, enabling the updated information to be displayed at one-second intervals. The cumulative counts gathered by CT_0 and CT_1 represent revolutions and work, respectively.

The 8253 counter-timer peripheral chip ties directly to a Z80 data bus, and its I/O ports are addressed by a chip-select signal and two bits from address decoding logic. A BASIC program reads the counters and processes a conversion (Figure 4). Since the counters are not reset, any reading of them yields the cumulative work done to that point in time. Those readings update a bar-graph display on the computer. In order to keep that display updated at uniform time intervals, the BASIC program, which is dedicated to that task alone, takes readings every second. The processor, however, which in other applications may be busy with supervisory functions, is not required to poll the counters regularly. All readings of the counters will show the cumulative result at that time.

TEMPORARY ASSIGNMENT

The 16-bit counters are read in a two-byte sequence (lines 80 and 90) that assigns separate temporary variables to each byte for conversion into a single 16-bit number. Since the 8253 is a down counter, the sense of the count is reversed before further processing, and the counters are never reset to zero, as would be done with frequency counting.

At the end of their 16-bit maximum count, CT_0 and CT_1 roll over and continue counting. A rollover occurs approximately every 26 revolutions of the wheel for CT_0 and is detected in software by comparing consecutive counter readings. When detected, 65,535 is added to the appropriate count variable (lines 120 and 130). The rotation counter must be read at least every 26 revolutions to avoid missing multiple rollovers of the counter, with the maximum count limited only by software.

OTHER USES FOR CUMULATIVE MULTIPLICATION

The instrumentation shown is an example of a general class of cumulative measurements which require the multiplication of two variables. The heat transfer measurement in Figure 5a shows another situation requiring multiplication of two variables. The heat transfer rate of a thermal system can be measured by multiplying the mass flow rate by the input-output temperature differential. Cumulative heat transfer is determined by counting the output pulses of the V/F converter.

Figure 5b shows another example requiring the multiplication of rate and torque to determine mechanical work of a DC motor. Torque is measured by sensing the current in the motor (torque is directly proportional to the current in a DC motor). Torque and speed are multiplied in the V/F converter and cumulative output pulses indicate total mechanical work.

When two input variables are expressed as a voltage, it may be more convenient to perform multiplication in an analog multiplier such as the model MPY634. It is possible, however, to convert the second variable to a frequency with a second V/F converter (Figure 5c). The unique attributes of the V/F conversion and counting scheme may provide advantages in some systems.

```
10 ' ERG.BAS  -- Z-80 MBASIC --  COUNTER CONTROL PROGRAM  9-23-85
30    GOSUB 480     ' INIT. 8253 PERIPHERIAL AND VARIABLES
40    GOSUB 740     ' INIT. SCREEN FOR BAR DISPLAYS
50  GOTO 70         ' SKIP TIMEOUT FIRST TIME THRU
60 WAIT C2,128,0  ' WAIT FOR 1 SEC TIMEOUT IN C2
70 Z%=INP(TP)      ' TRIGGER 1 SEC TIMER WITH DUMMY PORT READ
80   LB0=INP(C0) : UB0=INP(C0)  ' READ C0 LOWER BYTE, UPPER BYTE
90   LB1=INP(C1) : UB1=INP(C1)  ' READ C1 LOWER BYTE, UPPER BYTE
100 K0=HI-256*UB0-LB0  ' CONVERT COUNTER 0 DATA TO DECIMAL UP COUNT
110 K1=HI-256*UB1-LB1  ' CONVERT COUNTER 1 DATA TO DECIMAL UP COUNT
120   IF K01>K0 THEN K01=K01-HI  '  CHECK FOR ROLLOVER: SUBTRACT 64K
130   IF K11>K1 THEN K11=K11-HI  '  CHECK FOR ROLLOVER: SUBTRACT 64K
140 K0T=K0T+K0-K01  '  ADD TO RUNNING REVOLUTION TOTAL
150 K1T=K1T+K1-K11  '  ADD TO RUNNING WORK TOTAL
160 IF J<>0 THEN 180  ' TEST FOR FIRST TIME THRU
170    K0T=0 : K1T=0  ' ZERO TOTALS ON FIRST PASS
180 J=J+1          ' INCREMENT SECOND COUNTER
200    REVS=INT(K0T/2510)    '  CALC. TOTAL REVOLUTIONS
210    RPM=600*(K0-K01)/2510 '  CALC. CURRENT RPM
240     GOSUB 650      '  GO DRAW RPM BAR GRAPH DISPLAY
260  K01=K0           ' SAVE COUNTER VALUE FOR OVERFLOW TEST
280    WRK=.000217*K1T            '  CALC. CUMULATIVE WORK
290    PWR=3600*.000217*(K1-K11)  '  CALC. POWER FROM DELTA WORK
320   GOSUB 650         '  GO DRAW BAR GRAPH OF POWER
340 TORQ=9.55*PWR/RPM  ' CALC TORQUE FROM POWER AND RPM
370   GOSUB 650         '  GO DRAW TORQUE BAR GRAPH
390    K11=K1           '  SAVE COUNTER VALUE FOR ROLLOVER TEST
470 GOTO 60    '    ******  END OF MAIN LOOP  ******
480 '      SET UP AND INITIALIZE 8253 COUNTER PERIPHERAL
490   C0=&O320 : C1=&O321 : C2=&O322 : TP=&O330 : HI=65535!
500   OUT &O323,146     ' SET COUNTER 2, LO BYTE, MODE 1, BINARY
510   OUT C2,0          ' LOWER BYTE
520   OUT &O323,162     ' SET COUNTER 2, HI BYTE, MODE 1, BINARY
530   OUT C2,80         ' UPPER BYTE 80*256=20480
540   OUT &O323,48      ' SET COUNTER 0, SEQ R/W, MODE 0, BINARY
550   OUT C0,255 : OUT C0,255      ' MUST A LOAD COUNTER
560   OUT &O323,112     ' SET COUNTER 1, SEQ R/W, MODE 0, BINARY
570   OUT C1,255 : OUT C1,255      ' MUST A LOAD COUNTER
580   RETURN    '  END COUNTER SET UP AND INITIALIZATION
```

FIGURE 4. A BASIC program, shown in simplified form, reads the contents of three counters and creates a readout for a microprocessor display. The calculated results are converted into a bar graph, providing an analog output of the measurement results.

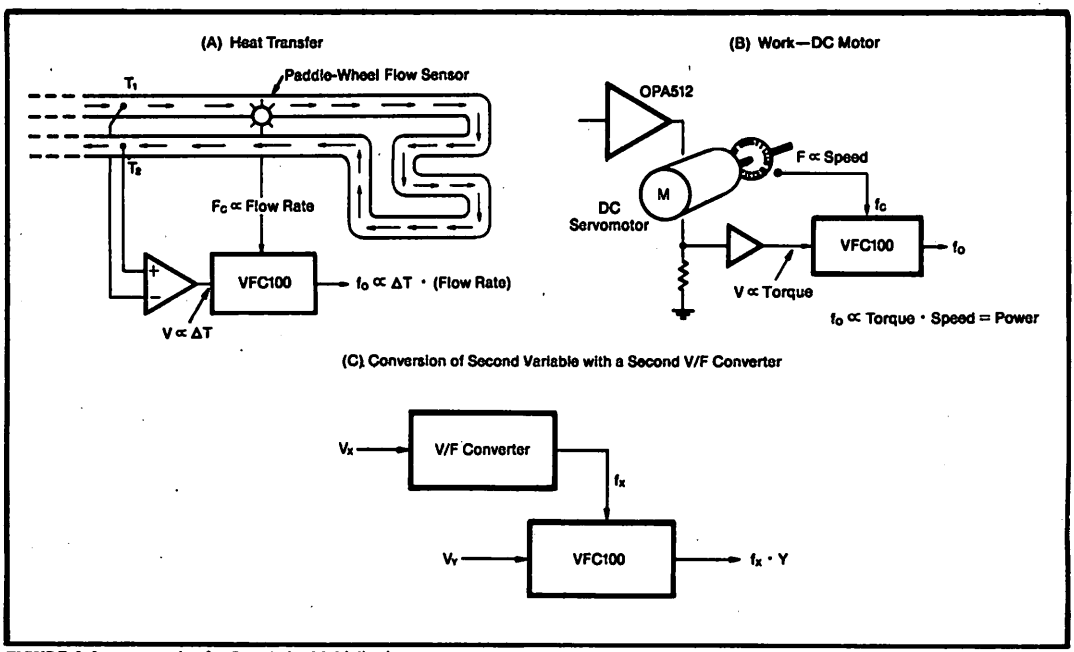


FIGURE 5. Instrumentation for Cumulative Multiplication.

VOLTAGE-TO-FREQUENCY CONVERTERS OFFER USEFUL OPTIONS IN A/D CONVERSION

Specialized Counting Techniques Achieve Improved Speed and Resolution

Voltage-to-frequency converters (VFCs) provide unique characteristics when used as analog-to-digital (A/D) converters. Their excellent accuracy, linearity, and integrating input characteristics often provide performance attributes unattainable with other converter types. By using efficient frequency counting techniques, familiar speed/accuracy trade-offs can be averted.

Since an analog quantity represented as a frequency is inherently a serial data stream, it is easily handled in large multichannel systems. Frequency information can be transmitted over long lines with excellent noise immunity using low cost digital line transmitters and receivers. Voltage isolation can be accomplished with low cost optical couplers or transformers without loss in accuracy. Many channels of frequency data can be efficiently steered to one counter circuit using simple digital gating, avoiding expensive analog multiplexing circuitry.

Like a dual-slope A/D converter, the VFC possesses a true integrating input. While a successive approximation A/D converter takes a "snapshot" in time, making it susceptible to noise peaks, the VFC's input is constantly integrating, smoothing the effects of noise or varying input signals. When system requirements suggest the VFC as an appropriate choice, a frequency measurement technique must also be chosen which meets the conversion speed requirements. While it is clearly not a "fast" converter, conversion speed of a VFC system can be optimized by using efficient counting techniques.

The frequency counting scheme shown in Figure 1 is the most commonly used technique for converting the output of a VFC to a numerical quantity. A gate time is created by dividing a reference frequency down to a suitable period, T. The output pulses of the VFC are simply accumulated during the time the gate signal is high. If T is equal to one second, for instance, the output count M is equal to the VFC frequency. Other gate periods (often 0.1 seconds, 10 seconds . . . etc.) are conveniently scaled by a decimal point shift or a simple multiplying factor. The reset circuitry which must be used to clear the counter before the next gate period occurs is not shown in this simplified diagram.

Since the gate period is not synchronized to the VFC output pulses, there is a potential counting inaccuracy of plus or minus one count on M. This is easily seen by imagining a sliding window of width T along the VFC output waveform. Counting the rising edges which are seen in that period, you can see how, depending on the VFC frequency, a ± one count error can occur.

The resolution which can be achieved by this method is related to the gate period, T, times the full-scale frequency of the VFC. This is equal to the number of counts, M, at full scale. Many applications require rela-

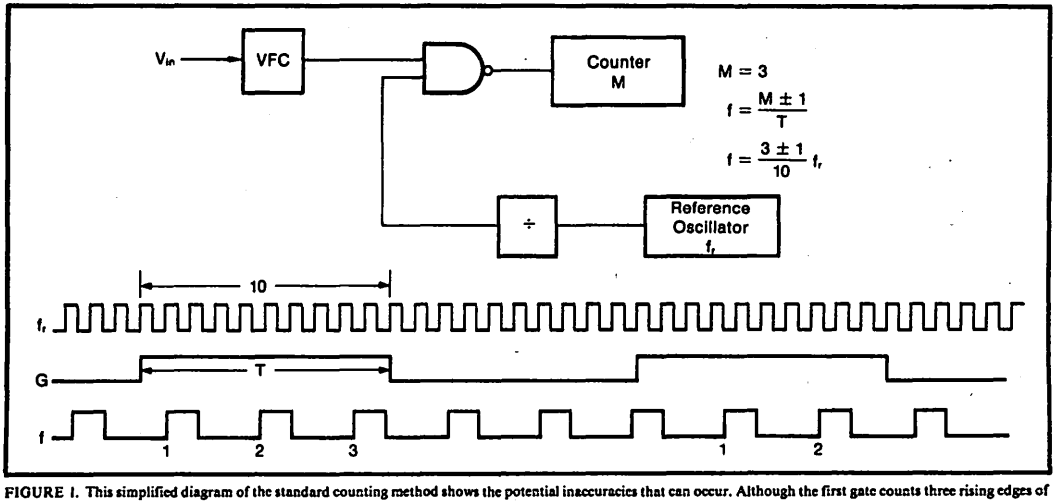


FIGURE 1. This simplified diagram of the standard counting method shows the potential inaccuracies that can occur. Although the first gate counts three rising edges of the VFC output frequency, f, the second gate period counts only two.

tively fast conversions (short gate periods) with high resolution. This can only be accomplished by the use of a high full-scale frequency. This is an effective solution in many cases, but since VFC linearity degrades at high operating frequency, this often limits the available accuracy.

The ratiometric counting technique shown in Figure 2 (sometimes called reciprocal counting) eliminates this tradeoff. By counting N counts of a high speed clock which occur during an exact integer M counts of the VFC, an accurate ratio of the unknown VFC frequency to the reference (f_r) is determined.

This is accomplished by using a D flip-flop clocked with the VFC output. A new, synchronized gate period is created which is an exact number of VFC pulses in duration. In contrast to the standard counting approach which has a plus or minus one count error on M, the synchronized gate precisely counts an integer number of VFC pulses. During the same synchronized gate period, high speed clock pulses are counted. Since these high speed clock pulses are not synchronized with the gate, this count has a plus or minus one count error. High resolution is achieved by making the reference oscillator a high frequency so the N count is a large number. The one count error can then be made to have a small effect on the result.

The additional resolution of this counting technique means that for a given conversion speed, the VFC can now be operated at a low frequency where its linearity and temperature drift are excellent. Again, reset and control circuitry have not been shown to clearly illustrate the fundamentals of the technique.

The resulting two counts (M and N) are divided to achieve the result of an individual conversion. This can be done in a host processor or microcontroller along with the offsetting and scaling that often must be performed.

An example of A/D system design is shown in Figure 3. It uses a VFC320 to convert a 0 to 10V input into a 2kHz to 10kHz output by offsetting the VFC input with a reference voltage. The 10V reference sets a constant input current through R3 + R4 which is added to the signal input current through R1 + R2. Since the synchronized gate awaits complete cycles of the VFC to achieve an exact count, a very-low VFC frequency would cause the synchronized gate period to be excessively long. The offset at the VFC input allows 2kHz (corresponding to 0V input) to be counted during the desired conversion time.

All counter functions are provided by a type 8254 counter/timer peripheral component which interfaces to many popular microprocessor systems. It contains three 16-bit counters which can be programmed for a variety of functions. Counter C2 provides the timing necessary to generate the gate signal "G". A rising logic edge at the Convert input initiates the conversion cycle. This causes FF1 to latch "high". Counter C2 is programmed and loaded to count 50,000 clock pulses (3MHz clock), then reset FF1. This creates a 16.66ms (1/60s) gate period at "G".

FF2 synchronizes the gate signal "G" to an integer number of VFC pulses, creating the synchronized gate "SG". Counter C0 tallies the exact number (M) of VFC pulses, while C1 simultaneously counts N high speed clock pulses.

Conversion to a digital result is completed by reading the contents of counters C0 and C1 by the microprocessor. The VFC frequency is computed in software as the ratio of M and N times the clock frequency. The proper choice of counter modes programmed in the setup of the 8254

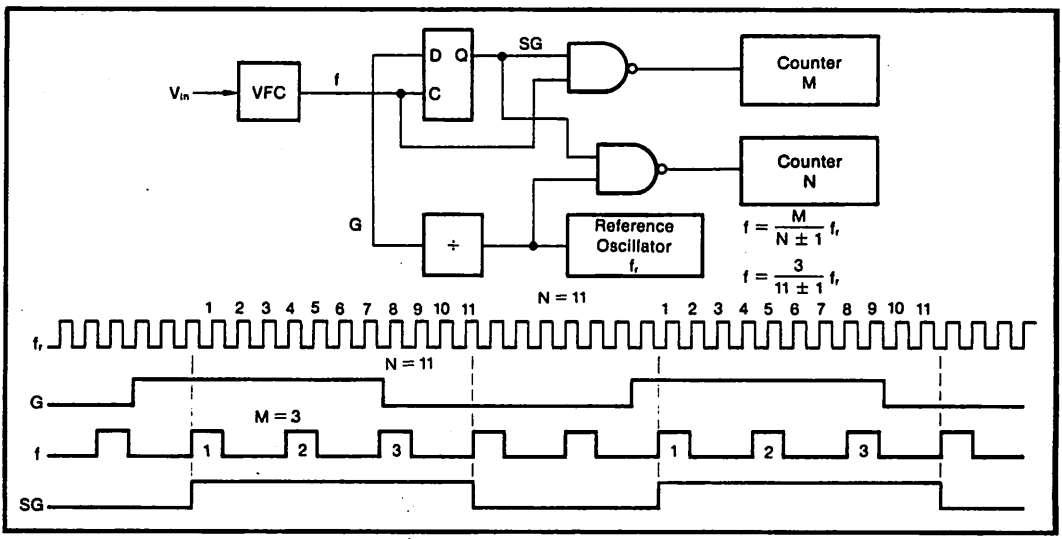


FIGURE 2. The ratiometric counting scheme in this simplified diagram synchronizes a gate period to the unknown input frequency from the VFC. The synchronized gate is then used to count the high frequency reference. The ratio of the exact count of M VFC pulses and the reference count, N, provide a more accurate measure of the unknown frequency.

peripheral allows counters C0 and C1 to be automatically reset at the initiation of the next conversion cycle. The Convert command can be created by hardware timing or other peripheral hardware can be used to initiate the conversion process with software control.

The seemingly odd gate period time of 16.7msec has a definite purpose. Since the integration period of the VFC is equal to the counting period, an interfering signal can be rejected by counting for one period (or an integer number of periods) of the interfering signal. Line frequency noise (60Hz) can thus be rejected by counting for 1/60sec or 16.7msec. Figure 4 shows the noise rejection of an A/D converter with an integrating (counting) period of T as a function of frequency. Using a gate period of 16.7msec, the deep nulls in the response curve align with the fundamental and all harmonics of 60Hz. The shorter gate periods feasible with ratiometric counting make the precise choice of the gate period important if good line frequency rejection is to be achieved. With long gate times the line frequency noise is far down the attenuation slope where reasonable noise integration is achieved without great concern as to the precise gate period.

Since the actual counting period is determined by the synchronized gate, SG, actual gate times will depend on the input VFC frequency and how the pulses randomly align with the gate. Worst case, however, occurs at low input voltage where the maximum deviation of the synchronized gate time from desired 16.7msec is equal to one period of the VFC at 2kHz or 0.5msec. Even this worst-case deviation from the ideal gate period still yields 30dB rejection of 60Hz and its harmonics.

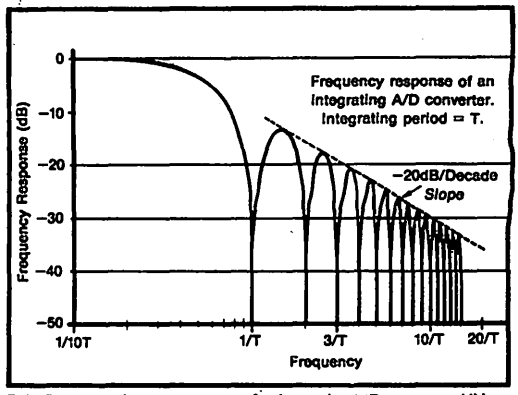


FIGURE 4. The frequency response of an integrating A/D converter exhibits a comb filter response. The deep nulls in the response are very useful for rejecting a known interfering signal and its harmonics.

In this example, conversion data is updated every 33.4msec, yet the counter resolution is one part in 50,000. Using standard counting, it would take several seconds to achieve the same resolution.

Figure 5 summarizes the speed/accuracy tradeoffs between the two counting techniques. With standard counting, the gate time is shortened as the VFC full-scale frequency is increased. This makes the number of counts at full scale consistent with the linearity achievable at that frequency. A low full scale is chosen for ratio counting where VFC linearity is excellent.

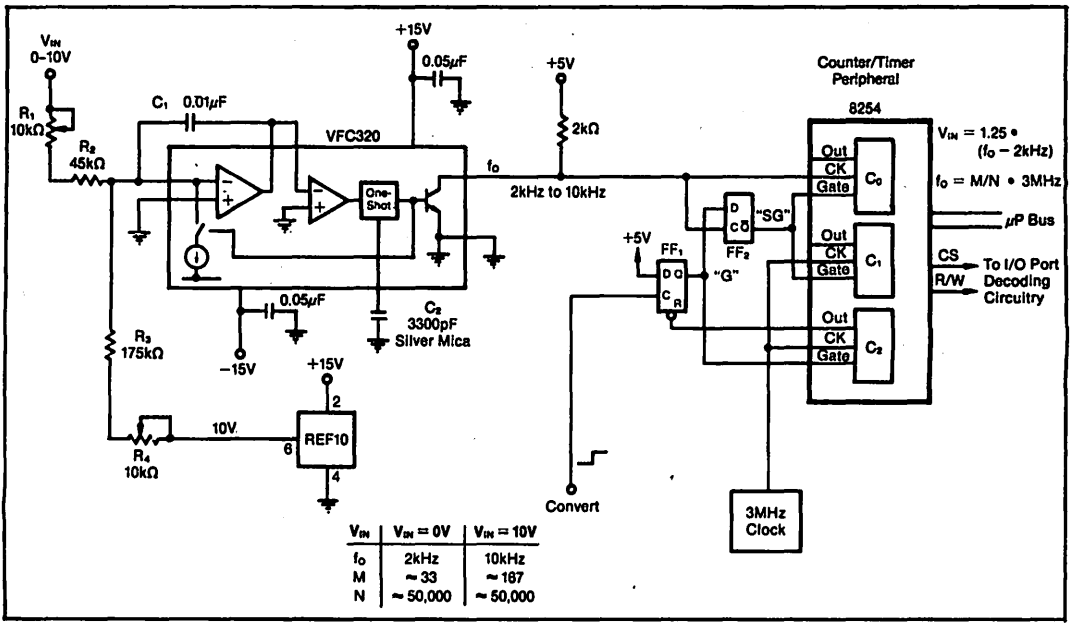


FIGURE 3. The VFC input is offset in this practical example so that low scale inputs can be converted in short times. Note that the N count always remains near 50,000 over the full input range while the M count ranges from 33 to 167.

VFC320 And VFC62 Performance				
Frequency Full Scale	Linearity (%)	Approximate Achievable Resolution [bits]	Conversion Time	Comments
STANDARD COUNTING				
10kHz	0.005	14	1.64sec	Accurate but slow.
100kHz	0.03	11	20.48msec	Fair accuracy and speed.
1MHz	0.2	9	512μsec	Fast, not too accurate.
RATIOMETRIC COUNTING				
10kHz	0.005	14	20msec	Fast and accurate.

FIGURE 5. Full accuracy capabilities are possible with either standard counting or ratiometric counting techniques, but ratio counting holds a large speed advantage. Standard counting should be considered, however, when an application would benefit from a longer counting integration period which tends to average broad-band noise.

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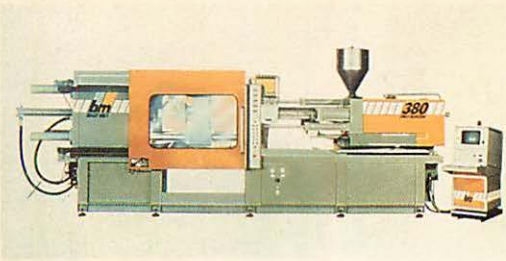

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